7.1 A 0.0056mm² All-Digital MDLL Using Edge Re-Extraction, Dual-Ring VCOs and a 0.3mW Block-Sharing Frequency Tracking Loop Achieving 292fs$_{rms}$ Jitter and -249dB FOM

Shiheng Yang[1], Jun Yin[1], Pui-In Mak[1], Rui P. Martins[1,2]

[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

Multiplying delay-locked loops (MDLL) and injection-locked clock multipliers (ILCM) have shown improved jitter performance in recent years [1-5], but their PLL-based frequency-tracking loops (FTLs) for securing performance against frequency and PVT variations are area and power hungry. In [1], the frequency (F_{OUT}) is tracked by a replica-delay cell of the VCO, such that the intrinsic phase information is preserved under reference injection (REF-INJ). Regrettably an analog FTL is susceptible to noise and mismatch from the charge pump, demanding more area (loop filter: 0.01mm²) and power (charge pump: 0.8mW) to limit the in-band jitter deterioration.

For the digital FTLs, using double REF-INJ and pulse-width comparison [2] can track F_{OUT} while expanding the REF-INJ bandwidth. Yet, two extra blocks (digital-to-analog and time-to-voltage converters: 0.015mm²) consume significant area for calibrating the duty-cycle mismatch and comparator offset, which otherwise could cause deterministic error. In [3], the deterministic error is resolved by calculating the period's error rate, but this entails the use of a 3.5mW algorithm for in-situ time-domain mismatch detection. In [4], a pulse-gating method skips the REF-INJ periodically every 8 REF cycles, such that the jitter can be accumulated for phase-error comparison. The main expense is a reduced F_{REF} in terms of the REF-INJ bandwidth (12.5%) and FTL bandwidth (78.5%).

The presented all-digital MDLL (Fig. 7.1.1) features edge re-extraction, dual-ring VCOs and a low-power (0.3mW) block-sharing FTL. Together, they improve the jitter performance (292fs$_{rms}$ at 3GHz) and stabilize it (<9% variation) against voltage, temperature and frequency changes, while requiring less area (0.0056mm²) and power (1.45mW) than recent art [1-5].

In our MDLL, the FTL incorporates a frequency selector for frequency coarse tuning (Fig. 7.1.1) and tracks for $(FCW-1)\times T_0+T_1=T_{REF}$, where FCW is the frequency command word; T_0, T_1 and T_{REF} are the periods of free-running, REF-INJ and REF, respectively. The edge extractor and time-interval comparator are used for frequency fine tuning to achieve $T_0=T_1$. The edge extractor is reused to extract the specific OUT edges from E_1 and E_2 containing the information of T_1 and T_0. For frequency fine tuning, the time-interval comparator directly detects the difference (ΔT) between T_0 and T_1. The coarse tuning and fine tuning loops run automatically in the background to accomplish frequency locking ($T_{REF}=FCW\times T_0$), even under a large frequency disturbance >F_{REF}, while [2,3] do not.

Figure 7.1.2 details the calibration steps at FCW=4. The digitally controlled delay line (DCDL)'s offset calibration is realized by: i) extracting the 1st and 2nd edges via the edge extractor controlled by SEL_{REF}, such that T_0 is not affected by REF-INJ ($t^{1st}-t^{2nd}=T_0$); ii) sending the 1st edge via the DCDL to delay it by T_{DCDL}, and comparing it with the 2nd edge via a bang-bang phase detector (BBPD); and, iii) returning the BBPD's decision to adjust the DCDL until $T_{DCDL}=T_0$.

Next, the fine-tuning calibration is enabled to compare T_0 and T_1 in 3 steps: i) extract the 3rd and 4th edges by $SEL_{(FCW-2)^{th}}$ sharing from the counter output; ii) delay the 3rd edge by T_0 via the DCDL, and compare it with the 4th edge via the same BBPD ($t^{3rd}-t^{4th}=T_1$); and, iii) send the decision to the fine-tuning path to adjust F_{OUT}. After F_{OUT} is finely tuned, the DCDL offset calibration will execute for the subsequent T_{REF} to work for $T_{DCDL}=T_0$.

The above two calibration steps run separately in each T_{REF} to continuously track F_{OUT}, while sharing the same blocks. When $T_0=T_1$, ΔT is nullified and F_{OUT} is driven to $FCW\times F_{REF}$. The overall time-domain calibration of the DCDL has a wide timing window (200-810ps) and a fine resolution (K_{DCDL} of 0.35ps/LSB) to ensure a wide F_{OUT} coverage (1.6-3.2GHz). The area (0.0015mm²) is 10× more efficient than its voltage-domain counterpart in [3] (0.015mm²). The edge extractor and the BBPD are reused for T_0 and T_1 to avoid offset and mismatch caused by the DFF and BBPD.

Figure 7.1.3 (upper-left) depicts the seamless frequency-tuning scheme. It features coarse tuning (B<13:11>) directly applied to the VCO's switched varactor banks, and moderate (MSB<10:6>) and fine (LSB<5:0>) tuning are applied as the varactor's control voltage through the DAC. The voltage step of one MSB (~25mV) is around half of the voltage range of the whole LSB band. Once the LSB is full (<111111>), the MSB will increment, and the LSB is set to the middle (<100000>). This undertaking not only improves the linearity and monotonicity, but also avoids the unwanted voltage step (≈25mV with 50% overlapping) that otherwise could cause frequency fluctuation (4MHz) when all LSB bits are fully switched on/off. The DAC (Fig. 7.1.3, upper-right) is implemented by 2 banks of coarse-fine current steering: MSB (LSB) for coarse (fine) control, and is 20× more area efficient (0.001mm²) than the unit-element-based tuning in [3] (0.02mm²). The DAC for VCO tuning has a fine resolution ($K_{DAC\text{-}VCO}$=120kHz/LSB) to match with the K_{DCDL},

$$K_{DAC-VCO} = K_{DCDL}\times\frac{(F_{OUT})^2}{FCW}$$

Small $K_{DAC\text{-}VCO}$ and K_{DCDL} are essential to reduce the reference spur (e.g. -65dBc at 1.8GHz and FCW=9),

$$\text{REF. Spur}|K_{DAC-VCO} \approx 20\log\left(\frac{K_{DAC-VCO}}{F_{REF}}\right)$$

and

$$\text{REF. Spur}|K_{DCDL} \approx 20\log\left(\frac{FCW\times K_{DCDL}}{T_{REF}}\right)$$

while the VCO's phase noise further aids to randomize the reference spur.

The dual-ring VCOs (Fig. 7.1.3, lower-left) are based on the REF-INJ MDLL with different sizes, covering two bands with overlap: 1.55-2.47GHz and 2.35-3.35GHz. A replica cell is inserted before the MUX to match the slopes between the injection signals and the outputs of the ring VCO. The pseudo-differential delay cells are implemented using inverters coupled in a feed-forward manner, with the varactors loading for frequency tuning. F_{OUT} is tuned by the varactor to preserve a constant jitter performance over the tuning range. Instead of tuning V_{DD} [2, 4] or current [1], which suffer from a degraded phase noise at low frequency (since the carrier power decreases faster than the noise power), the SEL for the multiplexer is controlled directly by REF, generating a pulse like an ILCM. This technique solves the bottleneck of a timing issue in the conventional MDLLs [2, 3] that utilize the output signal via a frequency divider. The SEL's window size (T_{SEL}) for REF-INJ is properly controlled, otherwise the deterministic error (glitch) from an oversize (undersize) window will disturb the OUT period.

With the proposed block-sharing FTL, the MDLL occupies 0.0056mm² in 28nm CMOS. It consumes 1.45mW at 0.8V over a 1.55-to-3.35GHz range (VCO: 1.15mW, FTL: 0.3mW). With a 200MHz $F_{REF,}$ the phase noise at 3.0GHz exhibits an integrated jitter (10kHz to 40MHz) improvement from 463 to 292fs$_{rms}$ when the FTL is enabled, and the result is dominated by the BBPD's and REF's noise (Fig. 7.1.4). The reference spur is -44dBc dominated by the reference power coupling in the I/O, and can be improved by upsizing the reference buffer. For the robustness of the MDLL, the worst variation of the integrated jitter is <9% against V_{DD} (0.74-0.9V), temperature (-40-120°C) and frequency (1.6-3.2GHz), as shown in Fig. 7.1.5.

Benchmarking with the recent ring-VCO-based MDLLs and ILCMs [1-5] in Fig. 7.1.6, this work shows improved area efficiency (>4.2×) and FoM_r (>2dB). The FTL's power (0.3mW) is the lowest reported. The experimental setup and die photo are shown in Fig. 7.1.7.

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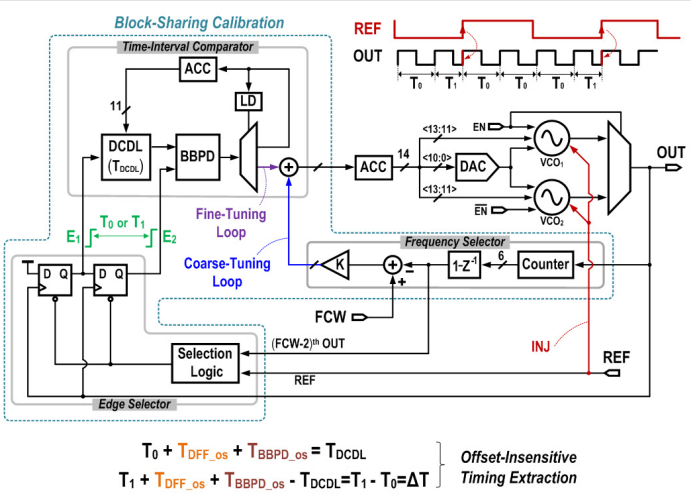


Figure 7.1.1: Proposed all-digital MDLL with a block-sharing FTL for better area and power efficiency. Edge re-extraction equalizes the periods T_0 and T_1 of OUT, being immune to the timing offset in the DFF (T_{DFF_os}) and BBPD (T_{BBPD_os}).

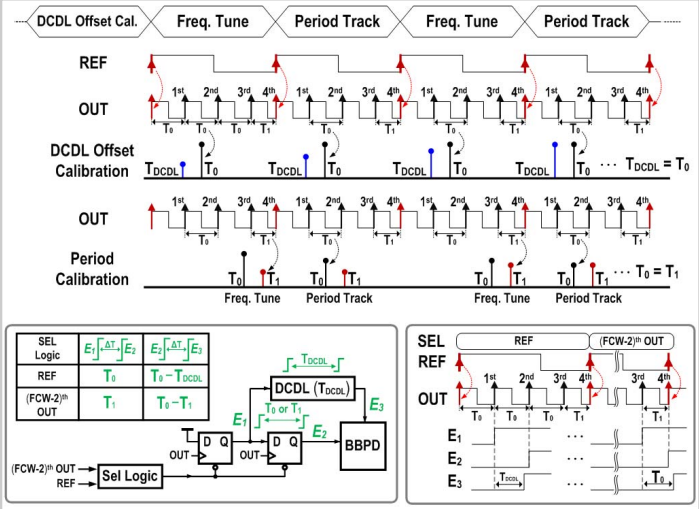


Figure 7.1.2: Timing diagram of the FTL with block sharing in each calibration step. Reusing the same DFF and BBPD logic not only cancels the timing offset and path mismatch, but also saves area and power. FCW=4.

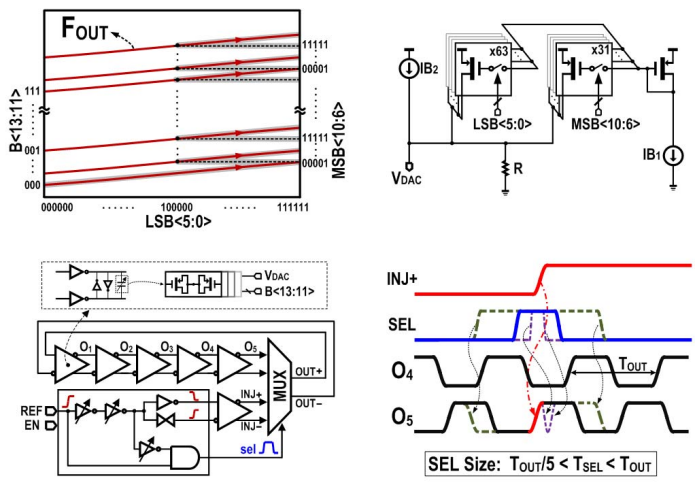


Figure 7.1.3: Upper: F_{OUT} tuning for seamless decoding and coarse-fine DAC block to optimize area and linearity; Lower: ring-VCO with direct REF-INJ to avoid the divider time constraint and SEL size effect to OUT.

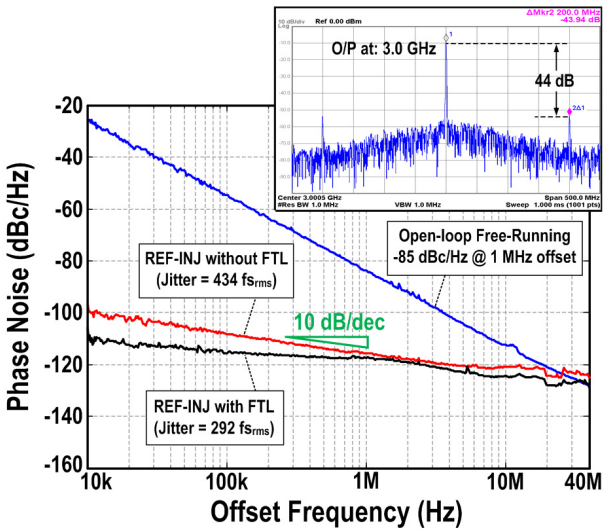


Figure 7.1.4: Measured phase noise: free-running ring-VCO, MDLL with and without the FTL. REF=200MHz and output at 3.0GHz.

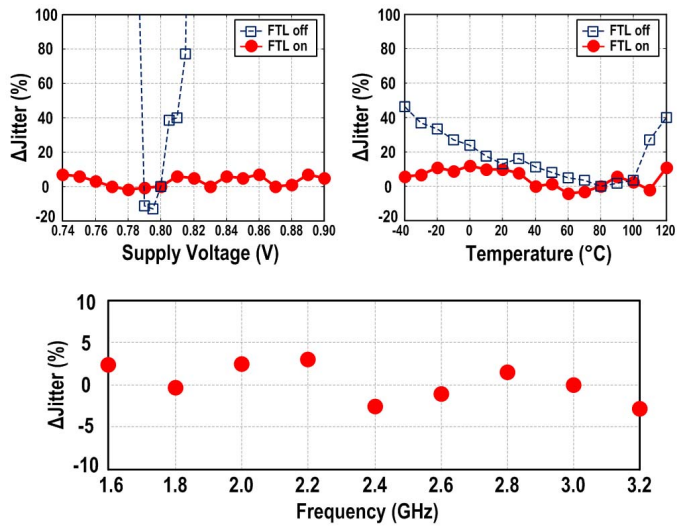


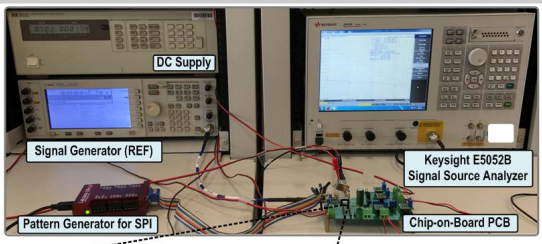
Figure 7.1.5: Measured RMS-jitter variation: <9% against supply voltage and temperature, and <5% versus frequency. REF=200MHz and output at 3.0GHz.

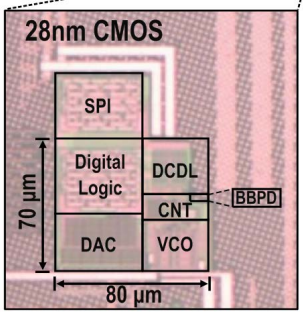
	This Work	[5] ISSCC'17	[4] ISSCC'17	[3] ISSCC'16	[2] ISSCC'16	[1] ISSCC'16
Technology (nm)	28	65	65	65	28	65
Architecture	Ring-MDLL	Ring-ILCM	Ring-ILCM	Ring-MDLL	Ring-MDLL	Ring-ILCM
Calibration Method	**Edge Re-extraction & Block-Sharing**	Synthesizable Symmetric PD Cancellation	Pulse Gating & 2x REF	Error-Rate Calculation	PWC & Double Injection	Replica Delay Cell
Supply Voltage V_{DD} (V)	0.8	1.2	0.9-1.1	1.2	N/A	1.1
Freq. Range (GHz)	1.55 to 3.35 (73.5%)	0.52 to 1.15 (75.4%)	2.5-5.75 [3] (78.8%)	0.2 to 1.45 (151.5%)	2.4	0.96 to 1.44 (40%)
Output Freq. (GHz)	3.0	0.9	5.0	1.4	2.4	1.2
Ref Freq. (MHz)	200	150	125	87.5	75	120
Multiply Ratio	15	6	40	16	32	10
Ref. Spur (dBc)	-44	N/A	-45	-45	-51.4	-53
Output Integrated Jitter ($p_{S_{rms}}$)	**0.292 (10k-40MHz)**	0.42 (10k-10MHz)	0.34 (10k-40MHz)	2.8 (10k-10MHz)	0.7 (1k-40MHz)	0.185 (10k-40MHz)
Total Power (mW)	**1.45**	3.8	5.3	8	1.51	9.5
FTL Power (mW)	**0.3**	2.9	2.0	3.5	0.43	4.75
FoM[1] (dB)	**-249.1**	-241.7	-242.4	-225	-241.3	-244.9
FoM$_T$ [2](dB)	**-249.1**	-242.9	-244.4	-228.6	-245.6	-247.1
Active Area (mm²)	**0.0056**	0.062	0.09	0.054	0.024	0.06

1: $\text{FoM} = 10\log\left[\left(\frac{\sigma_{rms}}{1\,\text{sec}}\right)^2 \cdot \frac{\text{Power}}{1\,\text{mW}}\right]$ 2: $\text{FoM}_T = 10\log\left[\left(\frac{\sigma_{rms}}{1\,\text{sec}}\right)^2 \cdot \frac{\text{Power}}{1\,\text{mW}} \cdot \frac{F_{REF}}{200\,\text{MHz}}\right]$, normalized to $F_{REF} = 200$ MHz

3: V_{DD} tuning included.

Figure 7.1.6: Comparison with the recent integer-N MDLLs and ILCMs.





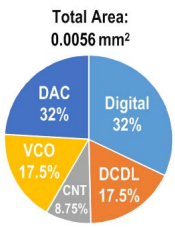


Figure 7.1.7: Experimental setup, chip photo and breakdown of total area.

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