A 13-bit 60MS/s Split Pipelined ADC with Background Gain and Mismatch Error Calibration

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Abstract— **This paper proposes acomprehensive background gain and mismatch error calibration technique for split ADC, without injecting any test signal. By employing a comparator threshold random selection method the input/output transfer characteristics of each split ADC channel is different. Based on Least Mean Square (LMS) adaptation the interstage gain error and capacitor mismatch error are corrected. All the estimations and corrections are performed in the digital domain, resulting in slight modifications of the analog circuit. The proposed calibration technique is applied on a 13-bit 60MS/s pipelined ADC. Fabricated in a 90nm CMOS process, the ADC achieves 70.8dB SNDR while consuming 63.8mW. The FoM is 377fJ/step at DC and 452 fJ/step at Nyquist.**

I. INTRODUCTION

The most popular architecture from the family of Nyquist Analog to Digital Converters (ADCs) is the pipelined ADC, which is used in many applications due to its high linearity and high resolution. However, for higher resolution above 12-bit, pipelined ADCs are very sensitive to interstage amplification and sub-DAC errors. The amplification error derives mostly from the insufficient DC gain of the opamp, and the sub-DAC error from the capacitor mismatch. In nanometer technology, these errors can hardly be avoided. On the other hand, digital circuits are quite efficient when the technology shrinks down. As a result, the digital calibration technique attracts attention since it allows the design effort to be transferred from the analog to the digital part.

Among different digital background calibration techniques, the split ADC concept takes advantages of the fast convergence speed when compared with dither injection techniques [1], [2] and low overhead analog circuit area, as well as power consumption when an analogy is made with auxiliary ADC calibration techniques [3]. In a split ADC, the main channel of the architecture is split into two half channels. Each half channel has full speed and full resolution but half capacitance and half power when related to the main channel. The outputs of each half ADC are added together to obtain the final output and the noise level is kept the same as before. The difference between two half

ADCs is used to drive the LMS engine for finding the correction parameters. Therefore, for the calibration to work the output difference can not be zero until each half channel has been fully calibrated. The design of two totally different structures as the half ADCs is relatively straightforward but the design effort increases significantly. Previously, only the residue transfer curves were modified in the first pipeline stage to allow the calibration to be applied on it while the backend is left identical and uncalibrated [4]. However, the second and third stages still contribute with severe errors, thus degrading the ADC performance. In this paper, a comparator threshold random selection technique is proposed and applied on the backend stages, while keeping backend identical, which allow their residue transfer curves uncoupled and hence the calibration can be extended to any pipeline stages. The calibration targets the errors in the inter-stage gain, the sub-DAC, as well as the sampling skew. With the calibration enabled in the first three stages the SNDR is enhanced from 42dB to 70.8dB.

II. TRANSITION POIINTS ANALYSIS

In a split ADC architecture (typical example shown in Fig. 1), the difference between each channel is used to drive the LMS loop. The calibration fails when the two channels generate equal but wrong decisions, which happens when the two channels have the same transition locations along their transfer characteristics.
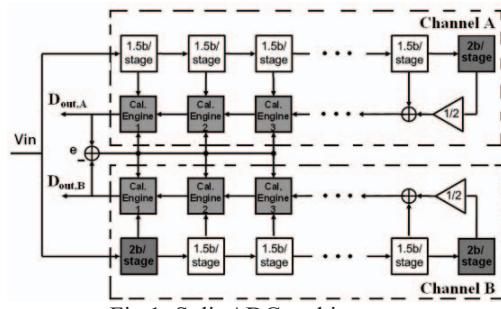

Fig.1: Split ADC architecture

For simplicity of the analysis, let us consider the first stage of channel A composed by a conventional 3-level 1.5-bit/stage MDAC (in our work the actual implementation with 7-level 2.8b) while the first stage of channel B employs

a 4-level MDAC (actual with 8-level) topology. Thus, the transition points of the residue in the first stage of channel A are $\pm 1/8V_{ref}$, and of channel B are $\{0, \pm 1/4\}V_{ref}$, being clear that the transition points are different, as well as the input/output characteristics. With a conventional 1.5b/stage architecture applied in the backend ADC Fig.2 plots the ADC transfer characteristics considering only the non-idealities in the 1st and 2nd stage.
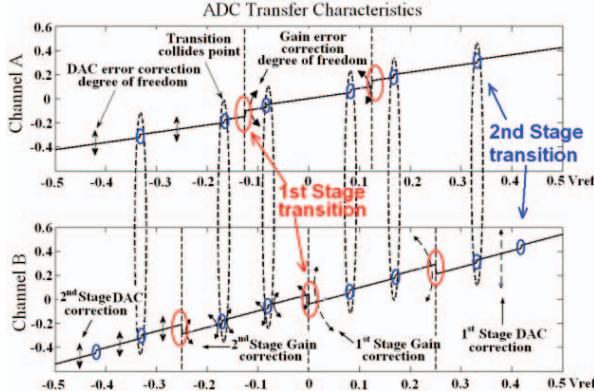

Fig.2: Traditional ADC Characteristics of two channels

From Fig. 2, it is found that the residue transition in 2nd stage points may still collide. The calibration of the gain error relies on changing the slope of each residue segment. Then, the gain error calibration adds one degree of freedom allowing each residue segment to rotate. On the other hand, as discussed in [4], the sub-DAC error is represented by the shifting, up or down, of each residue segment. The calibration adds or subtracts the shifted amount back to each residue segment linearizing the whole ADC transfer curve. However, the addition of a certain amount to each segment allows another degree of freedom by shifting up or down. Since the 2nd stage transition points are identical in both channels with the two degrees of freedom mentioned, it becomes evident that the whole ADC transfer curves for both channels can collide, even if they are not linearized, because the transition points of the residue in the two curves collide.

III. COMPARATOR THRESHOLD RANDOM SELECTION

To overcome this problem the residue transition points of the backend stages need to be differentiated in order to calibrate the errors starting from 2nd stages. This can be achieved by employing in the 2nd stages, 1.5b in channel A and 2b in channel B, but this will significantly increase the design efforts. In this paper a comparator threshold random selection technique is proposed to avoid the problem while keeping the design of the two backend channels identical. For example, in the channel A of the 2nd stage a positive offset V_{os} is intentionally added, while the same amplitude but with opposite polarity offset $-V_{os}$ is added in channel B of the 2nd stage. The polarity of the injected offset is controlled by a pseudo random sequence to avoid the inherited comparator offset canceling the additional added offset. With this dithering method the 2nd stage transition

points will be separated, as shown in Fig.3. The implementation of the dithering is realized by randomly selecting the reference voltage of the comparators shown in Fig.4. During phase 1, the dithered threshold voltage is sampled on the capacitor C_s, during phase 2, the input signal is applied on the bottom plate of C_s and the comparator makes the decision. The resistor string has more resolution to realize the dithering but the power and area remains the same. When applying the dithering, all the comparators in channel A share the same PN signal while those in channel B are controlled by $\overline{PN}$.

Theoretically, the dithering approach can be applied in every stage of the split pipelined ADC leading all stages too be identical (including the 1st), thus greatly simplifying the design. Here, it will be applied starting from the 2nd stage since the 1st stage dither occupies the over-range margin where the aperture error should also be accommodated in the S/H-less architecture. The dithering is realized by randomly selecting the threshold voltages of the comparators shown in Fig.4. Since the sub-ADC error is easily tolerated by the redundancy in the pipelined ADC the dithering method implies a very small penalty in the overall pipelined ADC operation.
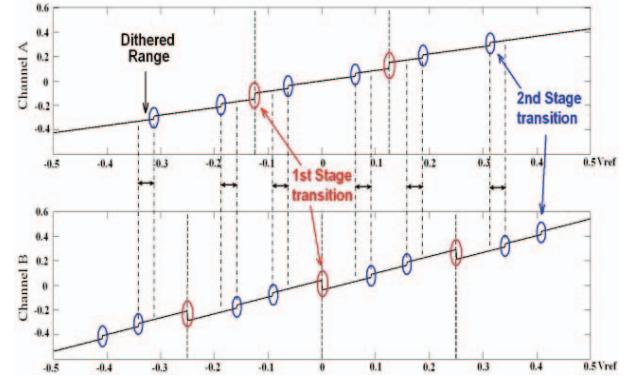

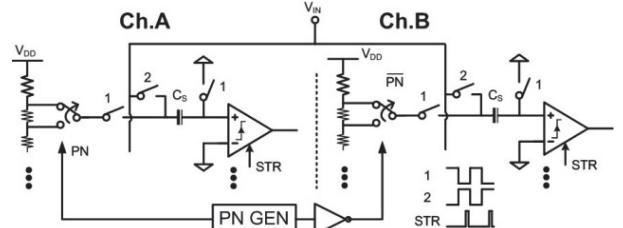Fig.3: Proposed Dithered ADC Characteristics

Fig.4: Dithered comparator circuit diagram

IV. CALIBRATION ALGORITHM

For brevity, a simplified ADC model with only the first stage calibration scheme is shown in Fig.5(a), while subsequent stages are grouped together as a backend ADC. With a similar theory and generality the calibration can be applied to any of the pipeline stages.

A. Gain error calibration

The inter-stage amplification error arises mainly from the insufficient open loop gain of the opamp which is the

dominating error source in pipelined ADCs. Practically, the gain stage can be modeled as a linear function $V_{res}=GV_x$. As shown in Fig.5(b) the calibration relies on implementing a digital inverse function which recovers D_{BK}, the digital representation of V_{res}, to D_x, the digital representation of V_x. The digital inverse is also modeled as a linear function $D_x=b_1D_{BK}$, where b_1 is the gain error coefficient. Thus, without taking the other calibrations into account, the digital output is $(D_1+b_1D_{BK})$. The corresponding difference between the outputs of the two halves of the ADCs is,

$$e = (D_{1A} - D_{1B}) + b_{1A}D_{BK,A} - b_{1B}D_{BK,B} \quad (1)$$

where the subscripts A or B indicate the quantities in channel A and channel B, respectively. As a result, the gradient of the gain error coefficient can be found and the LMS adaptation equation is deduced as,

$$\nabla b_{1A} = \partial e / \partial b_{1A} = D_{BK,A} \quad (2)$$

$$b_{1A}[n+1] = b_{1A}[n] + \mu \cdot e[n] \cdot D_{BK,A}[n] \quad (3)$$

B. DAC error calibration

The DAC error in a pipelined ADC is mostly due to the capacitor mismatch, and it moves the residue segment up or down randomly. To calibrate the DAC error the shifted amount should be added back according to the residue segment. The DAC calibration scheme is shown in Fig.5(c). Supposing that the correction amount is $\varepsilon_{DAC,j}$ for each residue segment, the digital output is $(D_1+D_x+\varepsilon_{DAC,j})$, and the corresponding output difference is,

$$e = D_{1A} - D_{1B} + D_{xA} - D_{xB} + \varepsilon_{DAC,A,j} - \varepsilon_{DAC,B,k} \quad (4)$$

where j={1…7} and k={1…8} are the indicators of the residue segment of the first stage in Ch.A and Ch.B, respectively. The gradient and the corresponding update formula can be deduced as follows,

$$\nabla \varepsilon_{DAC,j} = \partial e / \partial \varepsilon_{DAC,j} = 1 \quad (5)$$

$$\varepsilon_{DAC,j}[n+1] = \varepsilon_{DAC,j}[n] + \mu \cdot e[n] \quad (6)$$

It would also be important to note that the DAC error is a relative error, and for a pipeline stage with j levels the DAC calibration only requires (j-1) correction parameters.
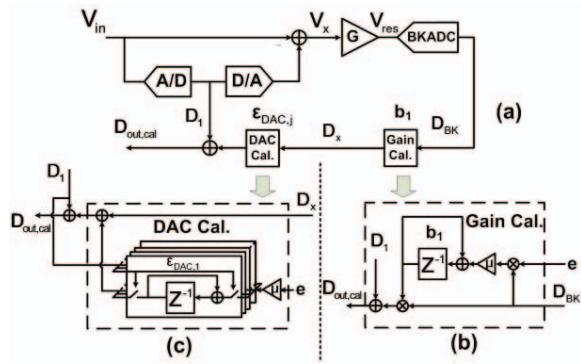

Fig.5: (a) Simplified ADC model, (b) Inter-stage gain error calibration diagram, (c) Sub-DAC error calibration diagram.

V. CIRCUIT IMPLEMENTATION

To verify the validity of the calibration technique a 13-bit split pipelined ADC is implemented with a supply of 1.2V. The architecture is similar to the one presented in Fig.1: each half ADC has 6 stages, in which the first stages of the Ch.A and the Ch.B use 7-level and 8-level structures and the backend uses a conventional 2.8b/stage with the last stage of a 3-bit flash. The calibration is applied in the first 3 stages with the distribution shown in Table 1. Fig.6 shows the MDAC circuit of the first stage. A flip-around topology is chosen and the reference voltage is directly obtained from vdd and gnd. The additional capacitor C_5, which is the only analog modification, injects a DC shift, thus resulting in the required 8-level residue curve. The comparator dithering is applied in the 2nd and 3rd stages. The dither amplitude is 75mV that occupies ¼ of the over range margin, and the redundancy still accommodates 56mV of the sub-ADC error. To save power consumption the capacitors and opamp are scaled down by a ratio of 4:2:1:1:1 in the pipelined ADC. The opamp is designed with a traditional single-stage folded-cascode topology with a DC gain of 42dB and consuming 6mW. Scaled versions of similar opamps are used in the following stages. In addition, the timing skew in the first stage is also calibrated using a fractional delay filter [3].
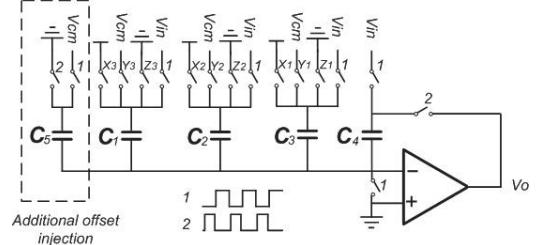

Fig.6: MDAC circuit used in the 1st stage (in Channel A/B, without/with C_5).

	1st stage	2nd stage	3rd stage	backend
Gain	Y	Y	Y	N
DAC	Y	Y	N	N
Timing	Y	N	N	N

Table 1: Calibration distribution.

VI. MEASUREMENT RESULTS

The chip micrograph of the prototype ADC is shown in Fig.7 with a core area of 0.93mm^2. Fabricated in 90nm CMOS process with the supply of 1.2V, the ADC is running at the sampling frequency of 60MS/s consuming 63.8mW of power, including all the reference voltage resistor strings, clock generator and digital power. During measurement, the digital codes of the first 3 stages and the backend codes are taken from a logic analyzer and then fed into the calibration model. Since there is no interaction between the output codes and the analog circuit, the calibration algorithm is implemented off-chip without any loss of generality. To test the reliability and the robustness a total of 20 chips were measured, with the performances shown in Fig.8. Fig.9 shows the INL plot, with an improvement from 50.8/-55.3LSB to 1.59/-1.49LSB, w/o or with calibration,

respectively, while the DNL is improved from 1.18/-1LSB to 0.96/-0.92LSB. On the other hand, Fig.10 depicts the FFT of the output near Nyquist frequency. Fig.11 shows the ADC performance at different input frequencies. The SNDR is improved from 42dB to 70.8dB at f_{in}=2MHz, from 41.2dB to 69.2dB at f_{in}=27MHz, respectively. The single split channels can also achieve 69.5 and 68.9dB SNDR at DC and Nyq. frequencies. Fig.12 exhibits the ADC performance at different sampling frequencies. The calibration is successfully attained in 10^5 samples or equivalent to 1.67ms at 60MS/s. The whole ADC has an FoM of 377/452fJ/conv.-step@DC/Nyq.. Table 2 shows the comparison between this work and the state-of-the-arts with background gain calibration and SNDR>65dB.

	[5] ISSCC '13	[6] ISSCC '10	[7] ISSCC '11	[8] CICC '11	[9] ASSCC '11	This work
Process (nm)	180	500	180	65	180	90
Resol.	14	18	16	12	14	13
fs (MS/s)	60	12.5	80	150	200	60
Power (mW)	68	105	100	48	460	63.8
SNDR @DC	76.9	88	77.6	67.5	68.5	70.7
SNDR @Nyq.	73.3	80	75	55	65.7	69.2
Area (mm²)	1.43	6	9.9	0.78	22	0.93
FOM @DC	198	410	202	166	1062	377
FOM @Nyq.	300	1025	273	698	1471	452

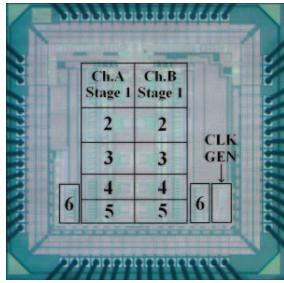Table 2: Comparison of this work with prior state-of-the-art.
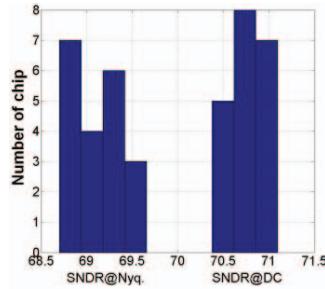

Fig.7: Chip micrograph of the prototype ADC.

Fig.8: Various Chip performances.

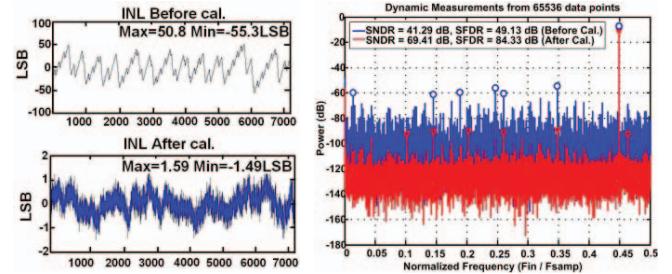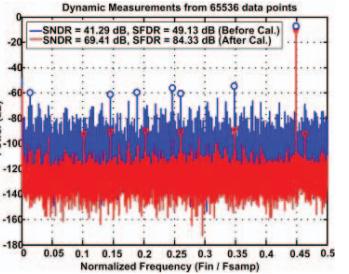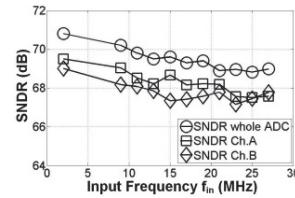
Fig.9: INL plots.

Fig.10 Output FFT spectrum

Fig.11: Performance sweep vs. input frequency f_{in}.
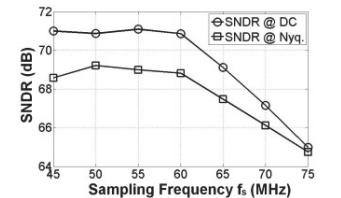
Fig.12: Performance sweep vs. sampling frequency f_s.

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