A Dual-Loop Digital LDO Regulator with Asynchronous-Flash Binary Coarse Tuning

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***Abstract*—This paper presents a dual-loop digital low-dropout regulator (DLDO) with asynchronous-flash (AF) binary coarse tuning for fast transient response. In steady state, the DLDO operates with a unary-weighted low power fine-tune loop to improve the regulation accuracy. Besides, a freeze mode is also employed to further reduce the power budget and to eliminate the limit cycle oscillation phenomenon. When a load-transient is detected, the proposed AF bidirectional shift register will direct the binary-weighted power switches for coarse and fast tuning. The prototype is fabricated in a 28nm bulk CMOS process. With V_{IN}=0.5V and 50mV dropout, the AF-DLDO can deliver 33mA output current and consume only 10.5μA quiescent current. We measured 102mV voltage undershoot for a 30mA/20ns load step, showing a 0.11ps FOM.**

Keywords*—Digital low-dropout regulator; LDO; asynchronous flash; coarse tuning, power management.

I. INTRODUCTION

Fully-integrated power management unit (PMU) provides point-of-load power supplies to various voltage domains for system-on-a-chip (SoC). Low-dropout regulators (LDOs) are widely employed for their fast-transient response and power supply rejection capabilities and small area overheads, compared to the switching mode power converters [1].

In recent years, bidirectional shift register (SR) based digital LDO (DLDO) becomes a popular research topic for its near-threshold voltage (NTV) operation and feasible process scalability [2]-[6]. As a result, DLDOs have emerged as a good candidate to fit in the low-power SoC applications. However, the DLDO response time and recovery time highly depend on its clock frequency. In the baseline design [2], it takes several clock cycles for the DLDO to react during a load transient. Therefore, either a large loading capacitor (large silicon area) or a high frequency clock (large quiescent current), or both, are commonly needed to satisfy urgent load requirements.

To miniaturize C_L and obtain full integration, some state-of-the-art designs introduced several possible solutions. The work from [7] proposed a multi-bit digital proportional-integration (PI) controller with event-driven scheme to shorten the loop latency, and thus reduce the output capacitance to 100pF. However, it only offers a driving capability of 3.3mA, and consumes 8μA to 258μA operation current due to the multi-bit digital signal processing. Further, [8] employed a SAR-like architecture to obtain 15.1ns fast-transient, but it may have

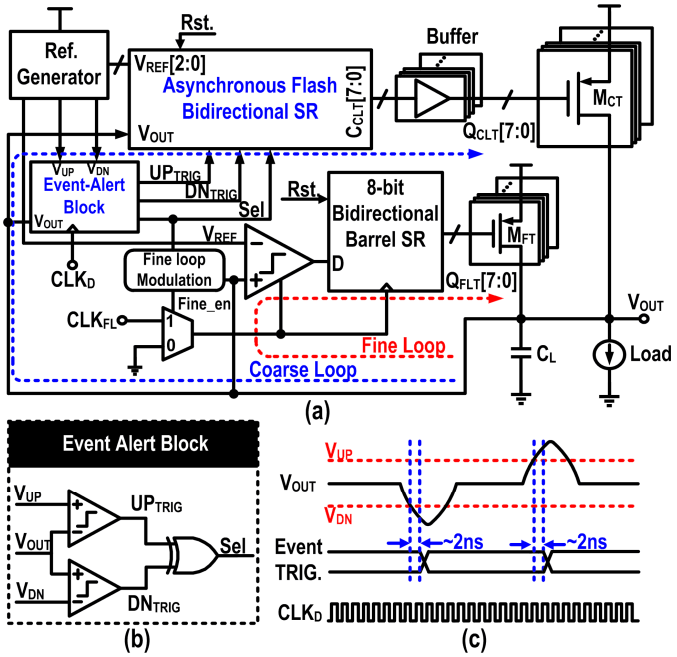

Fig.1. (a) Overall architecture of the proposed AF-DLDO; (b) the event alert block implementation; and (c) the event trigger timing diagram.

large transition glitches in the dynamic period. And, [9] shows a good example to alleviate the power-speed-area tradeoff with the help of an analog-assisted (AA) loop. But the effectiveness of the AA loop is proportional to the turned-on switches, reducing the transient performance in light load conditions. On the other hand, [10] is the first work that adopted an asynchronous logics DLDO. Although it is not a standalone LDO since it is in parallel with a main switching regulator to improve the transient response. Also, this idea is not verified under the NTV operation (its minimum V_{IN} is 0.9V). Meanwhile, the asynchronous pulse of the asynchronous operation needs to be initiated every time at the start or the end terminals of the bidirectional pipeline. Besides, [11] also uses an asynchronous theory based multi-step switching scheme to adaptively improve resolution and transient speed, with increased design complexity and a relatively large static current of 300μA.

In this paper, we propose a dual-loop DLDO with asynchronous-flash (AF) binary coarse tuning (AF-DLDO) to deal with the speed-power-area tradeoff. This paper is organized as follows: Section II presents the proposed asynchronous-flash

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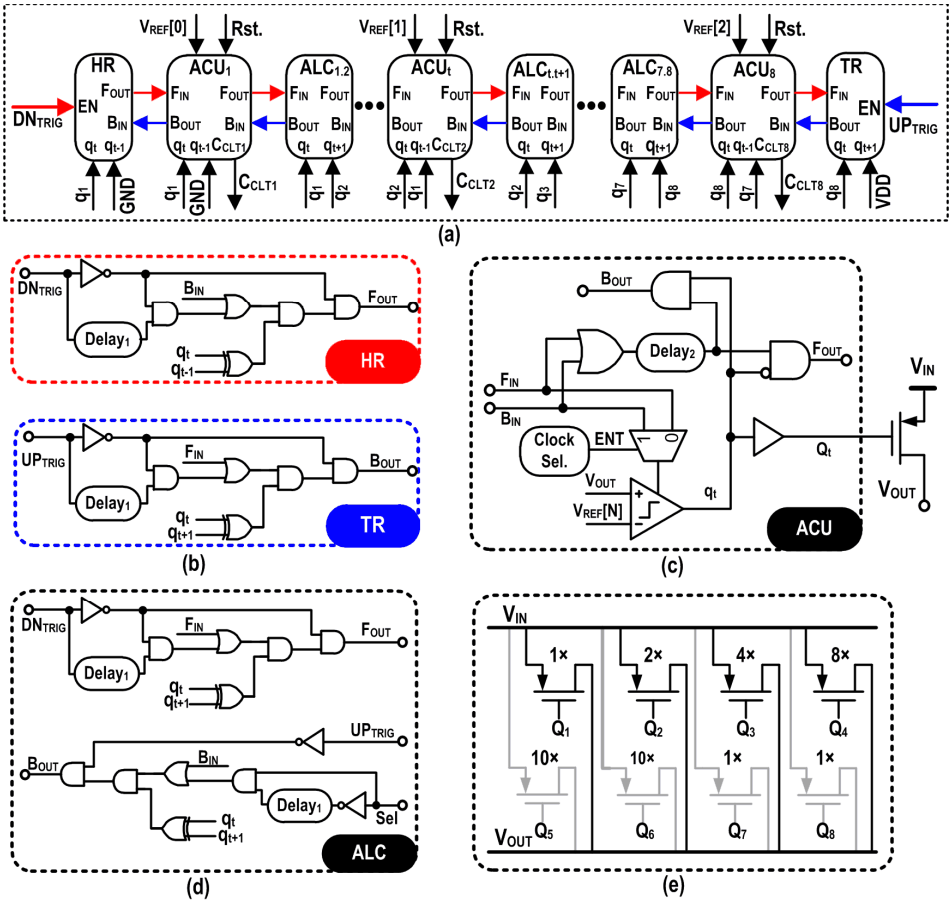

Fig.2. Implementation of the (a) asynchronous flash bidirectional SR; (b) heading reflector (HR); tail reflector (TR); (c) asynchronous control unit (ACU); (d) architectural logic connector (ALC); and (e) power transistor in the AF directed coarse tuning loop.

digital LDO, including the overall architecture, implemented AF bidirectional SR, and its operation timing diagram. Section III shows the silicon verified measurements results. Finally, Section IV draws a conclusion.

II. Proposed Asynchronous-Flash Digital LDO

In this section, the design details, such as the proposed overall architecture, the AF operation, and the control timing diagram, will be introduced.

A. Proposed Overall Architecture

Fig. 1(a) shows the overall architecture of the proposed dual-loop DLDO with AF coarse tuning, which consists of an 8-bits AF bidirectional SR controlled binary coarse loop, an 8-bits conventional SR based fine loop, and an event-alert block. Different from the prior coarse-fine DLDOs, the first 4 bits of the AF coarse loop power transistors (M_{CT}) are designed as binary-weighted PMOS switch array for tracking swift load changes, while the last 4 bits of the switch array are special designed to save some margin for preventing ringing in the load transient. The least significant bit (LSB) of M_{CT} in the coarse loop drives a current of 2mA, while the fine loop power transistors (M_{FT}) can deliver a total current of 4mA. To avoid excessive operations in the transient period, the AF bidirectional SR controller is divided into three sub-sessions which have their own reference voltages $V_{REF}[2:0]$, respectively. Therefore, the coarse switch array will be sequentially switched on and off only when V_{OUT} crosses a predefined $V_{REF}[N]$. As shown in the Fig. 1(b), we implement the event-alert block as a dead zone with a 500MHz sampling clock, which means the loading status could be detected in less than 2ns.

B. Implementation of the AF Coarse Loop

Fig. 2 illustrates the design details of the coarse tuning loop. The AF bidirectional SR, which is the core of the asynchronous coarse tuning loop, is composed of a heading reflector (HR), a tail reflector (TR), the architectural logic connectors (ALCs) and the asynchronous control units (ACUs). Essentially, the HR and TR are employed to form a closed signal transfer loop required by the asynchronous logics. Meanwhile, ALCs are inserted to enable the nearest ACUs at the very beginning of the transient response process. Specifically, 'q_t XOR q_{t+1}' acts as a control word combined with DN_{TRIG} and UP_{TRIG} to generate the enable signal and determine its transfer direction. For example, when q_t XOR q_{t+1} = 1 and $DN_{TRIG}UP_{TRIG}$ = 01, the AF bidirectional SR will conduct right-shift operation, whereas q_t XOR q_{t+1} = 1 with $DN_{TRIG}UP_{TRIG}$ = 10 triggers a left-shift action. The current signal flow will be immediately disabled when $DN_{TRIG}UP_{TRIG}$ = 11, which means the V_{OUT} has gone back within the dead-zone and the coarse tuning is terminated. Furthermore, q_t XOR q_{t+1} = 1 also locates the active boundary of $C_{CLT}[7:0]$ in steady state.

Consequently, a newly-generated enable signal could be instantly transferred starting from this border to respond to a fresh load variation. When compared to [10] which starts its asynchronous operation every time from the beginning, this control avoids vacant operations to start from either terminals of the SR pipeline and thus significantly shortening the loop delay. Each ACU contains an asynchronous clock through the in/out path connected in parallel and a clocked comparator for computing. Specifically, the in path is formed by a multiplexer controlled by 'clock sel.'to enable the comparator in this current ACU while the out path is composed of an OR gate in series with an artificial 'Delay$_2$' cell to validate the logic flow. In the transient period, ENT chooses either F_{IN} or B_{IN} to activate the comparator and the computed q_t validates an initial signal. After the delay$_2$ cell, this asynchronous clock is delivered to the next stage.

C. Timing Diagram

Fig. 3(a) presents the asynchronous-flash control scheme: an enable signal will be introduced once the ΔV_{OUT} triggers the event-alert block and then transferred to activate the comparator in the ACUs. Besides, reference ladder $V_{REF}[N]$ manipulates the comparator to direct the binary-weighted power transistor. This AF control avoids a possible V_{OUT} glitch in the conventional flash while substantially narrows the recovery time. Moreover, N-bits conventional-flash-ADC essentially needs 2^N comparators, during every dynamic action, with all comparators consuming power. However, in this design, N control words only require N comparators while every time only one remains active.

Fig. 3(b) gives the complete timing diagram with a rising loading step. In steady state, most parts of the regulator operate in freeze mode except the event-alert block, to obtain a compromise between energy efficiency and fast-transient. During large transient operation, the load (demand) goes up sharply, causing V_{OUT} to drop out from the dead-zone. A small negative error between V_{OUT} and V_{DN} forces the event-alert controller to set 'Sel' high, and a low DN_{TRIG} activates the shift-right path. Accordingly, a pulse F_{OUT} will be generated instantaneously through the heading reflector or the architectural logic connector located between two different asynchronous bits.

As a result, the comparator embedded in the asynchronous control unit is enabled, and then switches on the binary-weighted M_{CT} through a buffer in sequence to shorten the recovery time. In this sense, this right-shift action terminates when V_{OUT} beyond V_{UP} leads to UP_{TRIG} falling to low and then another pulse B_{OUT} will be re-created to proceed with a left-shift operation such that leads V_{OUT} back to the dead zone. All the asynchronous operation stops automatically once 'Sel' sets to low and the fine loop takes over. During this mode, 'Fine_en' keeps high only with a duration of T, and then, all the fine loop is forced into freeze mode. Additionally, when a small load step occurs, a supplementary enable signal for carry/borrow operation will be generated and applied to ACU_2 to improve the DC accuracy.

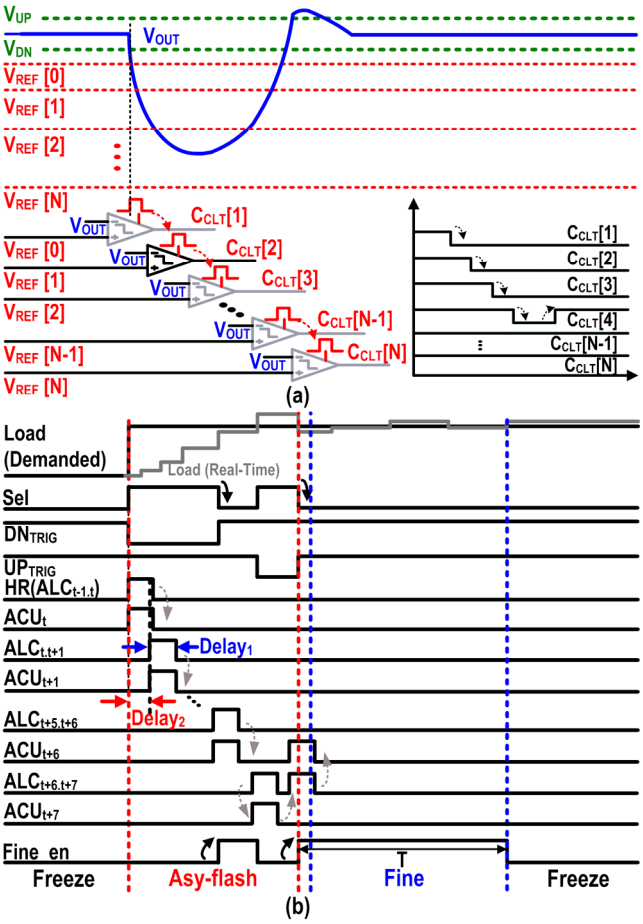

Fig.3. (a) Asynchronous-flash control law (b) Timing diagram under a raising loading step.

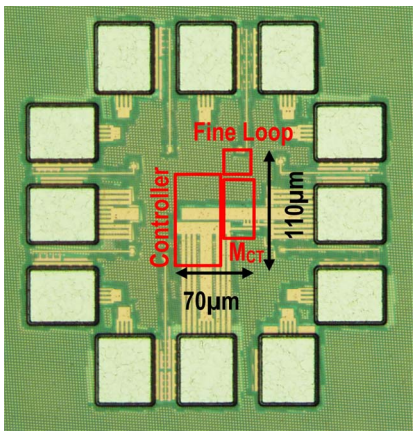

Fig.4. Chip micrograph of the proposed AF-DLDO.

III. Measurement Results

The proposed AF-DLDO has been fabricated in a 28nm bulk CMOS process. Fig. 4 shows the chip micrograph with a total chip area of 375 μm × 350 μm, including the I/O pads. The active area of the DLDO is 70 μm × 110μm.

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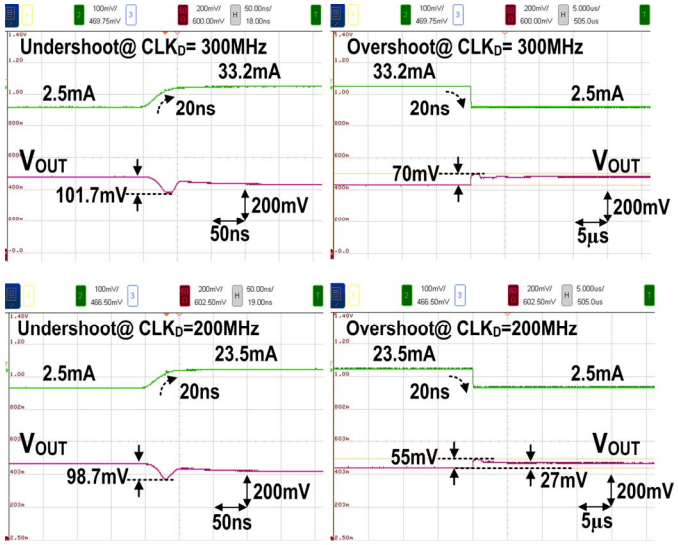

Fig. 5. Measured load transient response with V_{IN}=0.5V, V_{OUT}=0.45V, C_L=100pF, and load changes (a) from 2.5mA to 33.2mA within 20ns at CLK_D=300MHz and (b) from 2.5mA to 23.5mA at CLK_D=200MHz.

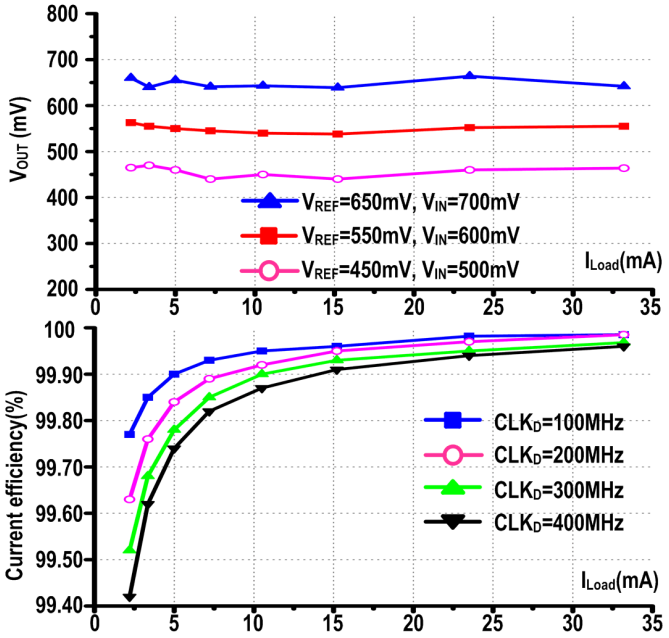

Fig.6. Measured load regulation with 50mV drop-out voltage (top) and current efficiency (bottom).

Fig.5 shows the measured load transient response with an off-chip loading capacitor C_L=100pF. Both the measurement conditions are V_{IN}=0.5V, V_{REF}=0.45V, and CLK_{FL}=10MHz. Thanks to the proposed asynchronous control algorithm, Fig. 5(a) maintains 101.7mV undershoot for $+\Delta I_{Load}$=30.7mA with 20ns edge time. The quiescent current (I_Q) is 10.5µA with CLK_D=300MHz, thereby achieving a settling time of less than 200ns. Meanwhile, Fig. 5(b) reveals 98.7mV undershoot for $+\Delta I_{Load}$=21mA with I_Q=7.95µA and CLK_D=200MHz.

Fig. 6 shows the measured load regulation (top) and current efficacy (bottom) of the proposed scheme. The peak current efficiency reaches 99.97% with CLK_D=300MHz, which has been vastly improved in contrast to conventional DLDOs.

TABLE I. PERFORMANCE COMPARISONS

	This work	[7]	[8]	[9]	[5]
Type	Digital	Digital	Digital	Digital	Digital
Process	28nm	65nm	65nm	65nm	28nm
Area [mm^2]	0.008	0.03	0.0023	0.03	0.021
Control	Asyn–flash	Event–driven	SAR/PWM	Tri–loop	Coarse/Fine
V_{IN} [V]	0.5–1	0.45–1	0.5–1	0.5–1	1.1
V_{OUT} [V]	0.45–0.95	0.4–0.95	0.3–0.45	0.45–0.95	0.9
Load range [mA]	2.5–33.2	0.014–3.356	0.0001–2	2–12	20–200
Total capacitance	0.1nF	0.1nF	0.4nF	0.1nF	23.5nF
I_Q [µA]	10.5	8.1–258	14	3.2	110
ΔV_{OUT} [mV] @ ΔI_{Load}	101.7 @ 30.7 mA	34 @ 1.44mA	40 @ 1.06 mA	105 @ 10mA	120 @180mA
Settling time @ ΔI_{Load}	150ns @ 30.7mA	11.2µs @ 1.4mA	100ns @ 1.06mA	4µs*** @10mA	N/A
Current Eff.* [%]	99.97	99.2	99.8	99.97	99.94
FOM** [ps]	0.11	20	199	0.23	7.75

* Peak Current efficiency ** FOM= $\frac{C_L \times \Delta V_{OUT}}{\Delta I_{Load}} \times \frac{I_Q}{\Delta I_{Load}}$

*** Estimated from measured result

This paper is compared with state-of-the-art DLDOs, as summarized in Table I. Our design achieves a FOM as small as 0.11ps while delivering 33.2mA output current with a static current of 10.5µA. It is the smallest among the prior arts given in the table.

IV. CONCLUSION

A dual-loop DLDO with asynchronous-flash (AF) coarse tuning has been proposed and verified in a 28nm bulk CMOS process. During the load transient, the AF coarse loop directs the binary-weighted power switches for fast transient response. In addition, a conventional fine loop was embedded for improving regulation accuracy. Therefore, a FOM of 0.11ps is measured with V_{IN}=0.5V and 50mV dropout voltage, showing 102mV undershoot during a 30mA/20ns load step.

Acknowledgements

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References

[1] Y. Lu, J. Jiang, and W. H. Ki, "A multiphase switched-capacitor DC–DC converter ring with fast transient response and small ripple," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 579–591, Feb. 2017.

[2] Y. Okuma *et al.*, "0.5-V input digital LDO with 98.7% current efficiency and 2.7-µA quiescent current in 65 nm CMOS," *IEEE Custom Integrated Circuits Conf.*, pp. 1–4, Sep. 2010.

[3] S. Gangopadhya, D. Somasekhar, J. W. Tschanz, and A. Raychowdhury, "A 32 nm embedded, fully-digital, phase-locked low dropout regulator for fine grained power management in digital circuits." *IEEE J. Solid-State Circuits*, vol. vol. 49, no. 11, Nov. 2014.

[4] S. T. Kim et al., "Enabling wide autonomous DVFS in a 22 nm graphics execution core using a digitally controlled fully integrated voltage regulator," *IEEE J. Solid-State Circuits*, vol. 51, no. 1, pp. 18–30, Jan. 2016.

[5] Y. J. Lee, *et al*., "A 200mA digital low-drop-out regulator with coarse-fine dual loop in mobile application processors." *ISSCC*, pp. 150–151, Feb. 2016.

[6] M. Huang, Y. Lu, S. W. Sin, S. P. U and R. P. Martins, "A Fully Integrated Digital LDO With Coarse–Fine-Tuning and Burst-Mode Operation," in *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 7, pp. 683-687, Jul. 2016.

[7] D. Kim, J. Kim, H. Ham, and M. Seok. "A 0.5V-V_{IN} 1.44mA-class event-driven digital LDO with a fully integrated 100pF output capacitor." *ISSCC*, pp. 346–47, Feb. 2017.

[8] L. G. Salem, J. Warchall, and P. P. Mercier. "A 100nA-to-2mA successive-approximation digital LDO with PD compensation and sub-LSB duty control achieving a 15.1ns response time at 0.5V." *ISSCC*, pp. 340–41, Feb. 2017.

[9] M. Huang, Y. Lu, S. P. U, and R. P. Martins. "An output-capacitor-free analog-assisted digital low-dropout regulator with tri-Loop control." *ISSCC*, pp. 342–43, Feb. 2017.

[10] Y. H. Lee, *et al*., "A low quiescent current asynchronous digital-LDO with PLL-modulated fast-DVS power management in 40 nm SoC for MIPS performance improvement." *IEEE J. Solid-State Circuits*, vol. 48, no.4, Apr. 2013.

[11] F. Yang and P. K. T. Mok, "A nanosecond-transient fine-grained digital LDO with multi-step switching scheme and asynchronous adaptive pipeline control," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2463–2474, Sep. 2017.

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