8.3 A Reconfigurable Cross-Connected Wireless-Power Transceiver for Bidirectional Device-to-Device Charging with 78.1% Total Efficiency

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Wireless power transfer (WPT) via inductive coupling is a convenient way to charge power-starved portable/wearable devices. Recently, device-to-device (D2D) wireless charging was demonstrated [1,2], which expands the range of WPT applications. Different from the traditional wireless charging, which obtains its energy from the AC mains and has virtually unlimited energy, the D2D charging sources power from an energy-constrained battery. Therefore, achieving the maximum-efficiency transfer is a key design issue. A zero-voltage-switching (ZVS) Class-ϕ_2 receiver with maximum efficiency tracking, but using several off-chip passives, was designed in [1] to improve the rectifier and coupling-link efficiencies for unidirectional D2D wireless charging. In [2], a reconfigurable wireless-power transceiver (TRX) with the maximum-current charging mode was proposed to turn a WPT receiver (RX) into a WPT transmitter (TX) with negligible additional hardware, which enabled the bidirectional D2D wireless charging. However, the TX mode efficiency and maximum output power in [2] are relatively low, and its WPT distance is short.

Figure 8.3.1 shows the proposed reconfigurable cross-connected (CC) wireless-power TRX with near-optimum switch-timing-control schemes for bidirectional D2D charging. As we know, CC power switches are widely used in full-wave rectifiers to reduce the switching losses, because they are driven by the LC tank with no loss [3]. On the other hand, the CMOS power transistors in the traditional Class-D power amplifier (PA) are controlled by separate buffers, generating large gate-drive switching losses. Here, we found that the CC topology can also be applied to the differential Class-D PA for switching loss reduction as well. Now, M_{P1} and M_{P2} are also cross-connected in the TX mode, charged/discharged by the resonant current I_{TX} when the ZVS of $M_{N1,2}$ is guaranteed by an optimum-switching control, significantly reducing the gate-drive losses. In addition, the multiplexers on the gate-drive paths in [2] are no longer required, saving certain area and conduction loss.

The reconfigurable controller can generate adaptive optimum switching for both modes. Figure 8.3.1 also shows the ideal critical waveforms of both modes. To achieve ZVS in the TX mode, the equivalent load impedance of the Class-D PA should be inductive, which means that the phase of the output voltage leads that of the output current. Therefore, additional variable capacitors C_{A1} and C_{A2} can be added to the RX, transformed by the resonant coupling link, making an inductive equivalent load to the TX. In the TX mode, M_{N2} turns off at t_0, prior to the I_{TX} zero-crossing point. During the deadtime t_{DT}, V_{TX2} is charged up and V_{TX1} is discharged by I_{TX}, while the operations of M_{P1} and M_{P2} swap. Then, M_{N1} is turned on at t_1 with ZVS. In the RX mode, to obtain a zero-current switching (ZCS), the off-delay of $M_{N1,2}$ is compensated by a delay-locked loop (DLL) in the reconfigurable controller. Near-ZVS of $M_{N1,2}$ can be achieved by comparators $CMP_{1,2}$ without any timing control.

Figure 8.3.2 shows the reconfigurable controller for M_{N1} and its timing diagrams. The voltage-controlled delay line (VCDL) and charge pump are reused by both modes. Separate phase detectors PD_{TX} and PD_{RX} are designed. The turn-on timing of V_{NT1} (V_{NR1}) is determined by detecting the rising edge of CLK (V_{CMP1}). While the falling edge (FE) is obtained from the VCDL delayed CLK (V_{CMP1}). During the start-up process, the delay time of the VCDL may be larger than half of the operation period, causing large transients and harming the safe operation of power transistors in both modes. Therefore, the logic AND_1 is added to limit the duty cycle of V_{NT1} and V_{NR1} to be <0.5. The PD_{TX} compensates V_{TX2} with t_{T_CP} first and detects the phase difference between V_{NT2} and V_{TX2_D}, where t_{T_CP} is the phase difference between V_{NT2} and V_{TX2} with the proper FE timing of V_{NT1}. Similarly, the PD_{RX} compensates V_{NR1} with t_{R_CP} first and detects the phase difference between V_{CMP1} and V_{NR1_D}, while t_{R_CP} is the off-delay caused by CMP_1. In the TX mode, when the deadtime is too large, I_{TX} reverses during the deadtime and charges up the discharged V_{TX2} again by the reverse current in the same half cycle. Thus, the second falling edge FE_2 misleads the PD_{TX}. Therefore, the PD_{TX} must be carefully designed to ignore FE_2.

Figure 8.3.3 analyzes the effectiveness of the typical and the proposed resonant switching topologies. To obtain inductive load on the TX side, one solution is to operate the TX at the frequency ω_{OP} higher than the resonant frequency ω_{RES}. R_{RECT} is the equivalent input impedance of the rectifier and Z_{EQ} is the equivalent load impedance on the TX side. However, this solution is only effective when the coupling coefficient k is lower than a critical value k_C. If $k \geq k_C$, Z_{EQ} is resistive and capacitive. In our case, a capacitor C_A is connected in-parallel with R_{RECT} and provides a capacitive load to L_2C_2. This capacitive load can be transformed to inductive Z_{EQ} in the whole range of k at $\omega_{OP}=\omega_{RES}$. However, C_A causes a resonant-frequency shift and reduces the current that goes into the rectifier. Therefore, the impedance of C_A should be several times larger than R_{RECT}. Here, $C_A \approx 300pF$ is selected. In the TX mode, C_A is harmful because it adds capacitive load to Z_{EQ}. Therefore, C_A should be tunable. In this design, C_A is composed of two series-connected PMOS capacitors C_{A1} and C_{A2}, with the body connected to high DC voltage. Thus, C_A can be tuned by switching its gate voltage.

To enhance the D2D total efficiency, the coupling link efficiency η_{LINK} should be also optimized. The theoretical peak link efficiency η_{MAX} can only be achieved at the optimal load resistance R_{OPT} [4], which is highly related to k. For maximum efficiency-point tracking (MEPT), a boost converter following the rectifier was used in [1], and a Q-modulation technique was proposed in [5], to tune the RX input impedance. In our design, we found that MEPT can be realized automatically if the TX and RX coils are identical and $k^2Q_1Q_2 \gg 1$, where Q_1 and Q_2 are the unloaded quality factor of L_1 and L_2, respectively. Because R_{RECT} has a very simple relationship with R_{OPT}, $R_{RECT}=(A/\eta_{PRM})\times R_{OPT}$, where A is the voltage gain of the power link and η_{PRM} is the TX coil efficiency. Thus, the lowest η_{LINK}/η_{MAX} can be estimated. When V_{BAT1}=4.2V and charges V_{BAT2} from 2.5 to 4.2V with η_{PRM} >60%, then η_{LINK}/η_{MAX} can be higher than 0.917. Figure 8.3.3 shows the theoretical η_{MAX} and the simulated η_{LINK} of our design. We can see that the η_{LINK} is very close to the theoretical η_{MAX} at different k and V_{BAT2}.

The reconfigurable CC wireless-power TRX has been fabricated in a 0.35μm CMOS process. C_{A1} and C_{A2} are placed in the space margins of the power transistors, without increasing the chip area. The total area is 3.92mm^2. Two identical PCB coils with a 4cm outer diameter are used in the measurement. Their inductance and unloaded Q-factor at 6.78MHz is 1.05μH and 111, respectively. Figure 8.3.4 shows the D2D total efficiency and P_{OUT} versus V_{BAT2} at different coupling distances. The peak total efficiency is 78.1% at P_{OUT}=0.8W. The maximum P_{OUT} of 2.7W with 62.5% total efficiency is achieved when the distance d=23mm. Figure 8.3.5 shows the measured RX voltage and current waveforms when charging a 4.7mF capacitor from 2.5 to 4.2V. Figure 8.3.6 shows the comparison with prior works. This work demonstrates the highest total efficiency and the longest transmitting distance relative to prior works in Fig. 8.3.6. Figure 8.3.7 shows the die micrograph.

Acknowledgment:
This work is supported by the Research Committee of University of Macau under MYRG2015-00107-AMSV, and the Macao Science and Technology Development Fund (FDCT) SKL-AMSV-2017-2019.

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 978-1-5090-4940-0/18/$31.00

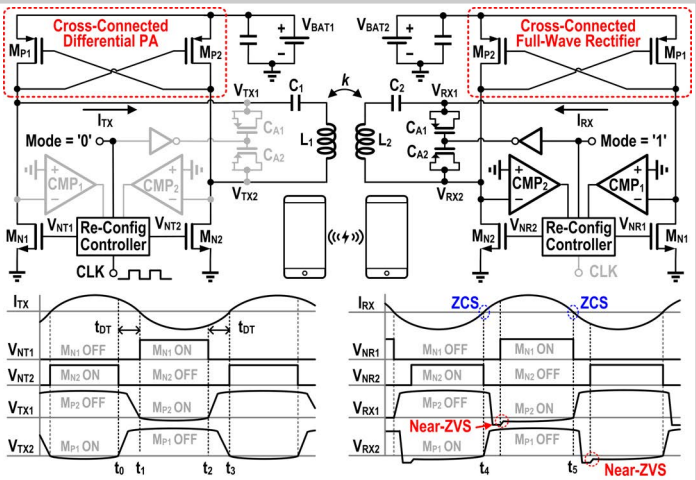

Figure 8.3.1: The proposed cross-connected reconfigurable wireless-power transceiver (top), which is configured to a cross-connected differential Class-D PA in the TX mode and a cross-connected full-wave rectifier in the RX mode, and the critical operating waveforms (bottom).

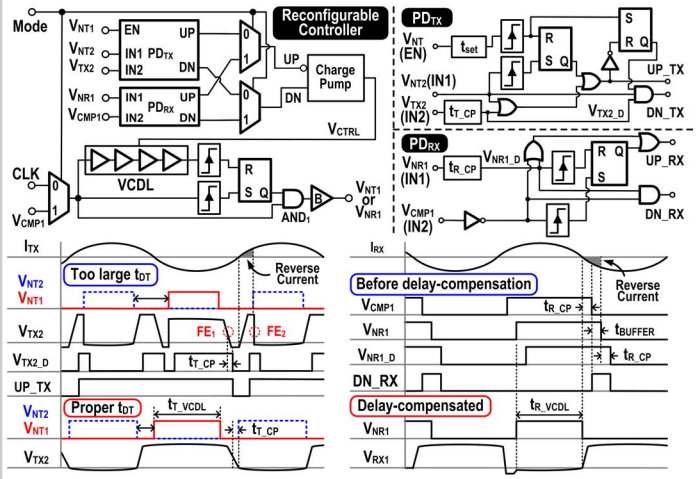

Figure 8.3.2: The block diagram of the re-configurable controller (top) and its timing diagram (bottom).

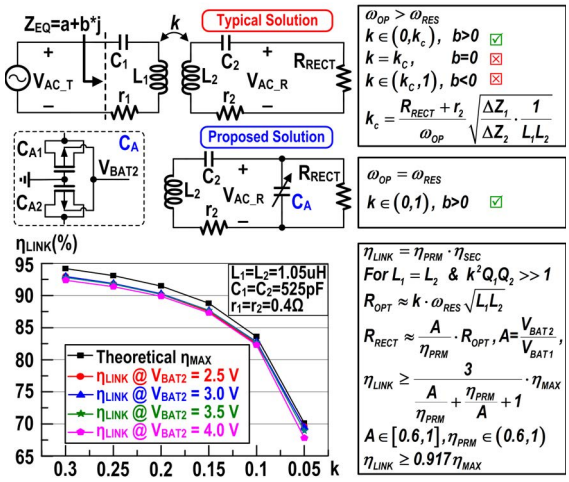

Figure 8.3.3: Comparison between a typical and the proposed solution to provide inductive TX load (top), the estimated lower limit of the power link efficiency, and the simulated power link efficiencies compared with the theoretical peak link efficiencies (bottom left).

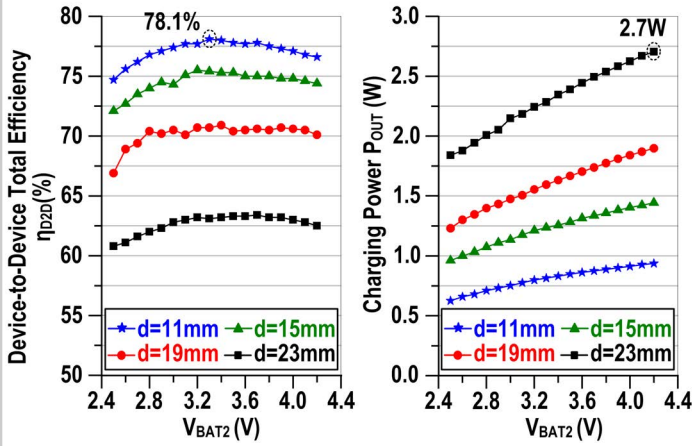

Figure 8.3.4: D2D total efficiencies and charging power at different output voltages and transmitting distances.

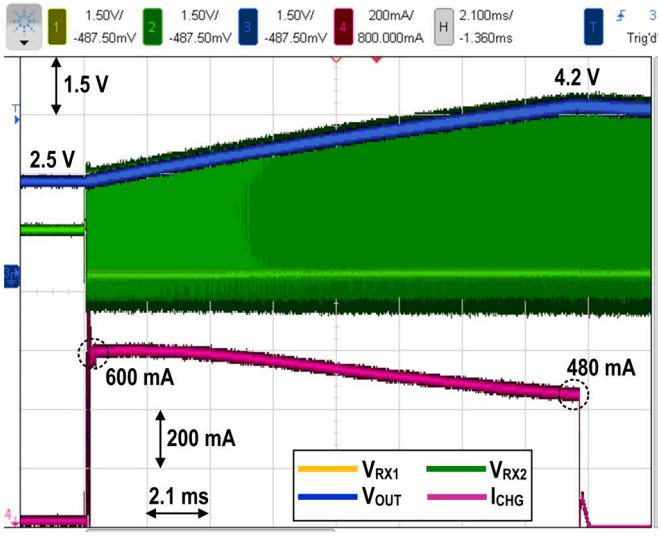

Figure 8.3.5: Measured RX AC input voltage, output voltage, and charging current when charging a 4.7mF capacitor.

	ISSCC'13 [7]	ISSCC'16 [6]	ESSCIRC'16 [1]	ISSCC'17 [2]	This Work
WPT Direction	Unidirectional	Unidirectional	Unidirectional	Bi-Directional	**Bi-Directional**
Mode	Pad-to-Device	Pad-to-Device	Device-to-Device	Reconf. D2D	**Reconf. D2D**
Process	0.35μm BCD	0.18μm BCD	0.18μm CMOS	0.35μm CMOS	**0.35μm CMOS**
Freq. (MHz)	6.78	0.1-0.3, 6.78	6.78	6.78	**6.78**
$V_{OUT,MAX}$ (V)	5	3.5	4.2	4.2	**4.2**
$P_{OUT,MAX}$ (W)	6	2.5	0.74	1.65	**2.7**
$\eta_{TOTAL,MAX}$	55%	63%	52.3%	58.6%	**78.1%**
Distance (mm)	NA	NA	19	6	**23**
Area (mm^2)	5.52	5.83	1.2	3.9	**3.92**
Off-Chip Components	5 Diodes 3 Capacitors	1 Inductors 3 Capacitors	2 Inductors 2 Capacitors	1 Capacitor	**1 Capacitor**

Figure 8.3.6: Performance summary and comparison table.

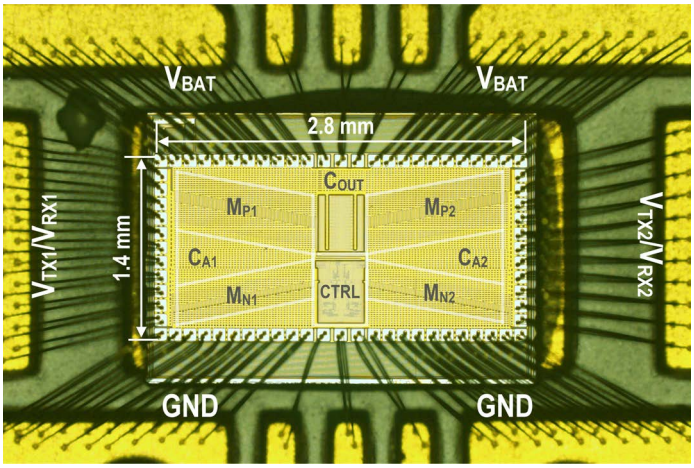

Figure 8.3.7: Die micrograph.

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