An Open-Source-Input, Ultra-Wideband LNA with Mixed-Voltage ESD Protection for Full-Band (170-to-1700 MHz) Mobile TV Tuners

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ABSTRACT

An ultra-wideband low-noise amplifier (LNA) covering the full mobile TV bands (170-to-1700 MHz) is presented. It features an ESD-protected open-source-input structure to interface the off-chip balun, such that a rail-to-rail input swing and an inductorless broadband input impedance matching can be achieved concurrently, while providing better linearity and inducing less noise. In the amplification core, double- current reuse and single-stage wideband thermal noise cancellation techniques are proposed. Optimized in a 90-nm CMOS process, the LNA achieves 20.6-dB voltage gain, 2.4-to-2.7 dB noise figure and + 10.8 dBm IIP3, while consuming 9.6 mW of power at 1.2 V. $|S_{11}| < -10$ dB is achieved up to 1.9 GHz without needing any external resonant network. Human Body Model ESD zapping tests of ± 4 kV at the RF pins cause no failure of any device.

1. INTRODUCTION

Large number of independently developed mobile TV broadcasting standards worldwide has led to the demand of multi-band solutions, which enable cost minimization of the embedded handheld devices that are intended for global market sale. Currently, three of the most dominant mobile TV standards are DVB-H (470 - 862 MHz and 1670 - 1675 MHz), T-DMB (174 - 245 MHz and 1452 - 1492 MHz), and ISDB-T 1 segment (470 - 770 MHz).

From the implementation viewpoint the digital back-end can be efficiently shared since those standards favor similar kinds of modulation (i.e., OFDM) and data coding (i.e., H.264 for video and AAC+ for audio). However, for the radio frequency (RF) front-end, a multi-band solution generally requires dedicated RF circuits optimized for each band [1], raising the manufacturing cost considerably.

This paper describes a new ultra-wideband (UWB) low-noise amplifier (LNA) covering the full mobile TV bands (170-to-1700 MHz) for cost minimization of the next-generation multi-band mobile TV tuners.

2. CIRCUIT DESCRIPTION

2.1 PMOS-based Open-Source-Input Structure

Figure 1 depicts the proposed PMOS-based open-source-input UWB LNA. To take advantage of the differential structure, a balun with center-tapped secondary is employed. Since the supported frequency can be as low as 170 MHz, the balun is very bulky in size and should be placed off-chip [1]. The balun interfaces the source, with an impedance R_S of 50 Ω, to the LNA by splitting the signal V_{rf} to M_1 and M_2, where reverse-biased P^+-diffusion diode D_P and N^+-diffusion diode D_N are adopted for pin-to-rail ESD clamp. ESD-protection rail-clamp circuits are incorporated with D_P and D_N offering low-ohmic discharge paths among the I/O supply voltage $V_{DD,I/O}$; the core supply voltage V_{DD} and the common ground *GND*. The idea of exploiting PMOS but not NMOS as the input devices (M_1 and M_2) is due to the fact that, with $V_{DD,I/O}$ as the clamping voltage, a very large input swing can be achieved, given that V_{DD} can be at midway from $V_{DD,I/O}$. On

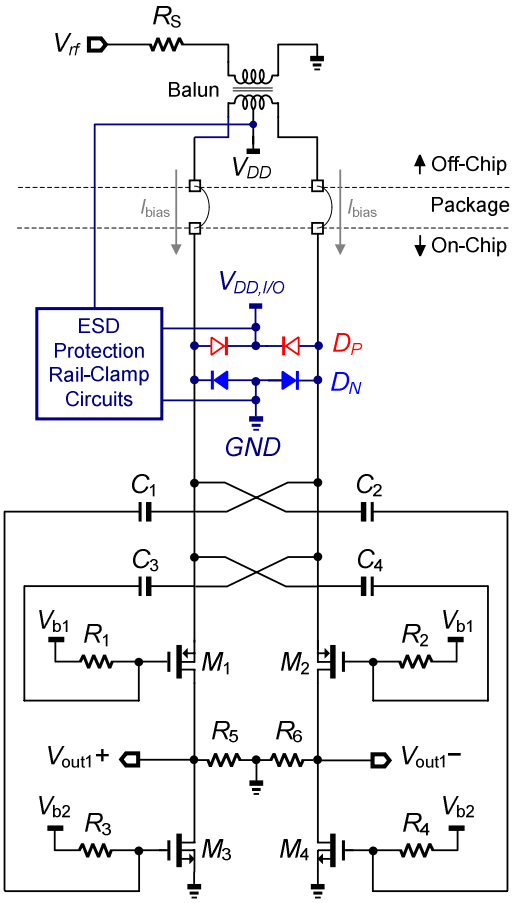

Fig. 1. Proposed PMOS-based open-source-input ultra-wideband LNA with ESD protection.

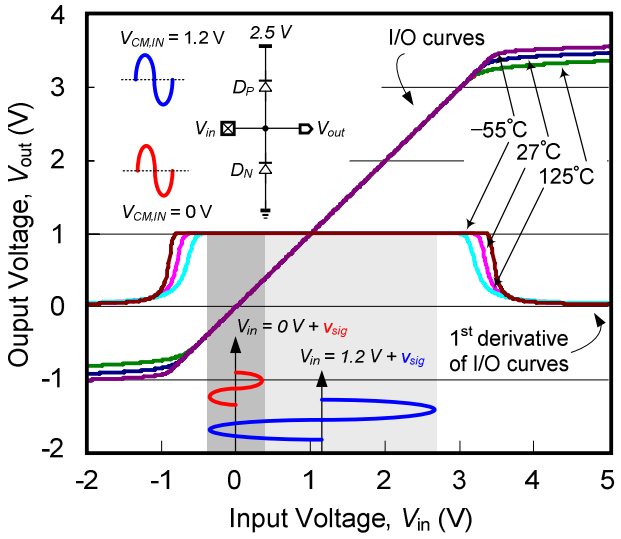

Fig. 2. Diode-clamp I/O transfer curves and their 1st derivatives at different temperatures.

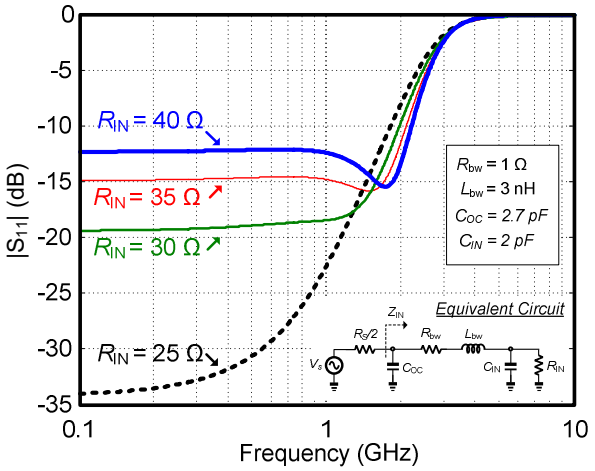

Fig. 3 Input matching design including package effects.

the other hand, the input swing will be limited by D_N in NMOS-based design [2], as the input common-mode voltage $V_{CM,IN}$ can only be close to *GND* for an optimum output swing. An example is shown in Fig. 2, wherein the diode-clamp I/O transfer curves and their 1st derivatives at the typical and extreme temperatures are plotted. The result is based on 90-nm CMOS process: i.e., V_{DD} = 1.2 V and $V_{DD,I/O}$ = 2.5 V. With $V_{CM,IN} = V_{DD}$, the AC input [$v_{sig}(t)$], even at the highest temperature, is still ~3 V in PMOS case, while it is just ~0.8 V in NMOS case with $V_{CM,IN} = GND$.

Besides that, considering the ESD robustness, $V_{CM,IN} = V_{DD}$ balances the ESD discharge capability in ± zapping events.

Furthermore, two more important advantages of using an open-source-input structure are worth to mention: 1) since the bias current I_{bias} is directly supplied through the balun, no additional current source is needed at the M_1's source node, inducing less noise and providing a higher linearity due to a wider output swing. 2) As the physical size of 90-nm transistors is very tiny, inductorless ultra-wideband input impedance matching can be practically achieved (see Section 3.1), resulting in very compact implementation.

2.2 Double-Current Reuse for Gm Enhancement

For power savings, two current reuse techniques are applied. First, M_1 and M_2 gate-source terminals are cross-coupled [3] such that the transconductance of M_1, g_{m1}, can be enhanced to g'_{m1}, i.e.,

$$g'_{m1} = (1 + A_x) g_{m1} \quad , \tag{1}$$

where A_x stands for the loss of the highpass network: C_3 and R_1 *(due to differential symmetry, we present only the left-half circuit)*. The capacitance division between C_{GS} of M_1 and C_3 makes $A_x < 1$.

The second current reuse technique is to cross-couple the input to also M_3, yielding an overall transconductance G_m as given by,

$$G_m = g'_{m1} + A_y g_{m3} \quad , \tag{2}$$

where A_y is the loss of the highpass network: C_1 and R_3. R_5 is the grounded resistor. It, in parallel with the output resistance of M_3 (i.e., r_{o3}) and by looking at the drain of M_1 (i.e., $R_{out,M1} = r_{o1} + 4R_S R_{IN}(1 + g'_{m1} r_{o1})/(R_S + 16R_{IN})$, defines the total output resistance, i.e., $R_L = R_5 // R_{out,M1} // r_{o3}$. The term $4R_S R_{IN}/(R_S + 16R_{IN})$ is the input impedance looking from the source of M_1 back to the balun (denoted as R_X hereinafter). R_{IN} is the input resistance of the LNA as given by,

$$R_{IN} = \frac{R_5 // r_{o3} + r_{o1}}{1 + g'_{m1} r_{o1}} \quad . \tag{3}$$

In overall, we obtain the differential voltage gain of the LNA, $A_{v,diff}$, as given by,

$$A_{v,diff} = \frac{2\left(\frac{1}{r_{o1}} + G_m\right)(R_5 // r_{o3})}{\frac{R_5 // r_{o3}}{r_{o1}} + 1 + \frac{R_S}{2r_{o1}} + \frac{g'_{m1} R_S}{2} - \frac{A_y g_{m3} R_S (R_5 // r_{o3})}{2r_{o1}}} \quad . \tag{4}$$

2.3 Thermal-Noise Cancellation in a Single Stage

Thermal-noise canceling LNA using a *two-stage* topology has been reported in [4]. Here, the proposed LNA has the advantage of thermal-noise cancellation in a *single stage* by using the balun and the Gm-enhancement structure (Section 2.2). Examining Fig. 1 we can observe that the thermal noise of M_1 (which can be modeled as a noise current source connecting its drain and source) not only directly injects to V_{out}+, but is also negatively coupled to the source of M_2 through the balun, and the gate of M_2 and M_4 through the coupling networks, i.e., R_2-C_4 and R_4-C_2, respectively. The same noise coupling operation occurs around M_2. Differentially, certain noise transfer paths will be out phased from the others, yielding a way to cancel out the noise of M_1 with virtually no cost. Noise analysis shows that the noise factor F of the LNA is given by,

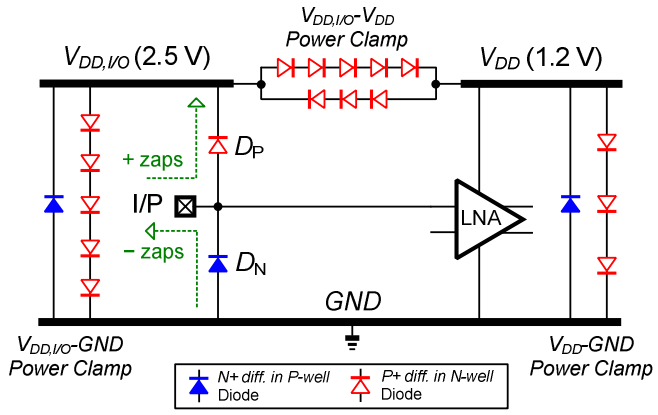

Fig. 4. Mixed-voltage ESD-protection clamps.

$$F = 1 + \frac{\left[\frac{2R_X R_{IN}}{R_X + R_{IN}}\left(g_{m1} + \frac{A_x g_{m1}}{1 + g_{m1}R_X} + A_y g_{m3}\right) - 1\right]^2 g_{m1}\frac{\gamma_1}{\alpha_1} + g_{m3}\frac{\gamma_3}{\alpha_3} + \frac{1}{R_5}}{\left(\frac{2R_{IN}}{R_S + 2R_{IN}}\right)^2 \left(g_{m1} + \frac{A_x g_{m1}}{1 + g_{m1}R_X} + A_y g_{m3}\right)^2 R_S}, \quad (5)$$

where $\alpha_1(\alpha_3)$ and $\gamma_1(\gamma_3)$ are the process- and bias-dependent parameters of M_1 (M_3), respectively. Principally, the noise of M_1 can be fully cancelled by satisfying,

$$\frac{2R_X R_{IN}}{R_X + R_{IN}}\left(g_{m1} + \frac{A_x g_{m1}}{1 + g_{m1}R_X} + A_y g_{m3}\right) = 1 \quad . \quad (6)$$

g_{m3} is the key which helps fulfilling (6) since most of the other parameters are constrained by other performance metrics (e.g., gain and S_{11}).

3. KEY PRACTICAL DESIGN ISSUES

3.1 Input Impedance Matching with Package Effects

With the package effects (Fig. 3, right bottom) taken into account, the single-ended (left-half of the circuit) input impedance, Z_{IN}, of the LNA is given by,

$$Z_{IN} = \frac{1}{sC_{OC}} // \left[sL_{bw} + R_{bw} + \left(R_{IN} // \frac{1}{sC_{IN}}\right)\right] \quad . \quad (7)$$

where L_{bw} and R_{bw} stand for the inductance and resistance of the bondwire, respectively; C_{OC} models the parasitic capacitance of the leadframe and soldering pad on the testing board; C_{IN} is the total input capacitance resulting from M_1, D_N and D_P, the parasitic capacitance of C_1 and C_3, and the bondpad (C_{PAD}).

With R_S = 50 Ω and a balun ratio of 1:1, R_{IN} = 25 Ω achieves a superior $|S_{11}|$ ($|S_{11}| = |Z_{IN}–R_S/2|/|Z_{IN}+R_S/2|$), but an insufficient bandwidth as shown in Fig. 3. Thus, R_{IN} is selected to be 35 ~ 40 Ω such that the quality factor of the equivalent circuit is reduced, resulting in wider matchable bandwidth while giving an adequate $|S_{11}|$ inherently (i.e., saving any external matching network).

3.2 Mixed-Voltage ESD Protection Scheme

Protecting the core devices from ESD events requires well-designed discharge paths to the rails. Figure 4 shows the designed mixed-voltage ESD clamps. Power clamps based on P+/N-well- diode chains can efficiently realize a sufficient high trigger voltage that is greater than the supply, such that the leakage current and the chance of accidental latching due to normal supply fluctuation are minimized. For instance, with a silicon diode threshold voltage of ~0.65 V, the $V_{DD,I/O}$-GND power clamp needs 5 diodes in series, whereas for V_{DD}-GND only 3 are necessary.

The selected number of diode in the $V_{DD,I/O}$-V_{DD} power clamp must have the precaution of different supply start-up sequences. For instance, $V_{DD,I/O}$ may start before V_{DD}. The proposed structure that shown in Fig. 4 is to minimize the forward-bias current in a safe level in all supply start-up sequences.

The dimension of D_P (D_N) is 10 × 50 µm. Since the technology determines that the parasitic capacitances resulting from D_P and D_N per unit area are C_{DP} = 0.9 fF/µm^2 and C_{DP} = 0.74 fF/µm^2, respectively, the imposed total parasitic capacitance at the input is ~870 fF, which occupies 44% of the total C_{IN} budget (Section 3.1). The rest C_{IN} budget can be reserved for the C_{PAD} (~300 fF), the input parasitic capacitance of M_1 and the parasitic capacitances of C_2, C_4 and C_5.

4. RESULTS AND COMPARISON OF PERFORMANCE

The LNA has been fully characterized in *Cadence* environment with *SpectreRF* as the simulator. The package effects at the RF input pins have been taken into account in all simulations. The ESD robustness of the RF-input pins to rail combinations is tested using the Human Body Model (HBM) reference circuit [5]. A ± HBM voltage pulse is applied to the LNA's input to induce a large +/– zapping discharge current that has a rising/falling time of ~8 ns. Verified in all combinations, the LNA can withstand minimally ± 4 kV of ESD zapping without causing internal or protection devices failure. This result fulfills the standard of "safe level" (i.e., ± 4 kV) in the chip-level ESD specifications.

To show the robustness of the LNA over PVT, a 10-time Monte-Carlo simulation result of the key frequency-domain performances are shown in Fig. 6. Minimally, the peak voltage gain is 20.6 dB, and the bandwidth is from 0.1 to 1.89 GHz [Fig. 5(a)]. $|S_{11}| < –10$ dB is achieved up to 1.93 GHz [Fig. 5(b)]. The in-band noise figure (NF) ranges from 2.4 to 2.7 dB [Fig. 5(c)]. The in-band reverse isolation ranges from 28 to 29.6 dB.

The in-band linearity is verified by two-tone test at 708 and 720 MHz (Fig. 6). An IIP3 of +10.8 dBm and a –1-dB input-referred compression point (ICP) of –7.6 dBm are obtained. Another two-tone test at 2.0 and 2.1 GHz is also conducted, which gives the out-of-band IIP3 of + 9.9 dBm and a –1-dB ICP of –3.5 dBm. Both are superior linearity performance metrics in this 1.2-V, 9.6-mW design.

Although the LNA exhibits a pseudo-differential structure, extensive use of ac-coupling helps minimizing the chain

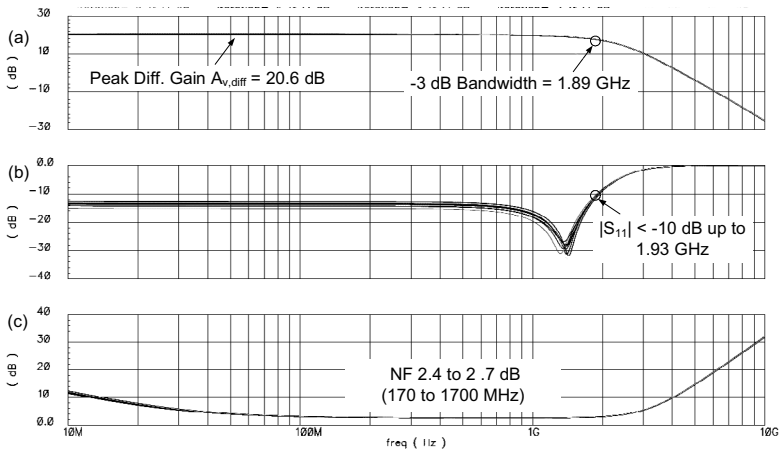

Fig. 5. 10-time Monte-Carlo simulation results of the LNA: (a) voltage gain, (b) $|S_{11}|$ and (c) NF.

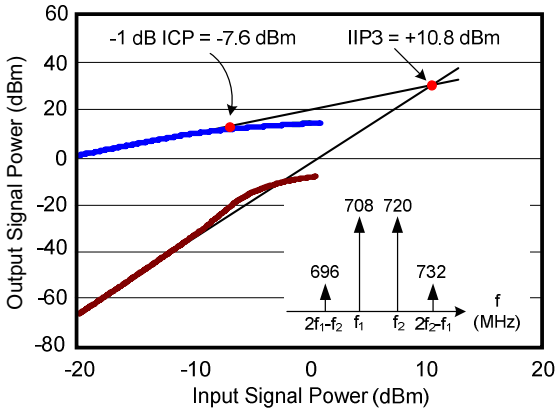

Fig. 6. Two-tone test at 708 and 720 MHz.

reaction of differential imbalance. In this LNA, ~10% size mismatch between M_1 and M_2 still maintains high in-band common-mode rejection ratio and supply rejection ratios above 50 dB.

Table 1 presents a comparison of the proposed LNA with respect to certain recently published (both measured and simulated) wideband LNAs [6]-[9] that operate at a similar frequency range. It can be observed that most performance metrics of this work are of high standard, even under high ESD protection.

5. CONCLUSIONS

A novel UWB LNA for full-band mobile TV tuners has been presented. A high ESD robustness of ± 4 kV at the RF input pins and a high input swing were achieved by using a PMOS-based open-source-input structure and the 2.5-V I/O supply as the clamping voltage. In addition, double-current reuse and single-stage wideband thermal-noise cancellation techniques were applied concurrently, resulting in high voltage gain (i.e., 20.6 dB) and high IIP3 (i.e., +10.8 dBm), as well as low noise figure (i.e., 2.4-to- 2.7 dB) and low power (i.e., 9.6 mW). $|S_{11}|$ < –10 dB was achieved up to 1.93 GHz without needing any external resonant network.

ACKNOWLEDGMENT

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Table 1. Brief performance comparison of recently published LNAs

	Technology	Bandwidth (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Supply (V)	Power (mW)	$ESD_{RF\text{-}input}$
This work	90nm CMOS	0.1 - 1.89	20.6	2.4 – 2.7	+10.8 @ 0.7 GHz	1.2 (2.5 I/O)	9.6	± 4 kV
[6] RFIC'07	90nm CMOS	0.4 - 1	16	3.5 - 5.3	–17 @ 1 GHz	1.2	16.8	No
[7] PRIME'06	130nm CMOS	0.9 - 2.5	17	2	–5	1.2	15.6	No
[8] RFIC'05	130nm CMOS	0.1 - 0.93	13	4	-10.2	1.2	0.72	No
[9] ASSCC'05	180nm CMOS	0.04 - 0.9	20.3	4	–10.8 - 12.7	1.8	43.2	No