A 7b 2 GS/s Time-Interleaved SAR ADC with Time Skew Calibration Based on Current Integrating Sampler

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***Abstract* - This paper presents a time-interleaved (TI) SAR ADC that utilizes the characteristic of the current integrating (CI) sampler for sampling time skew background calibration, while it also provides buffering and anti-aliasing filtering functions, simultaneously. The inter-sample interaction in the CI sampler enables the mapping of the time domain information to the amplitude domain. Time skew errors can therefore be extracted by comparing the output-code variance among channels without requiring a reference path. A 2-channel 2 GS/s 7b TI-SAR prototype realized in 28-nm CMOS achieves a 36.4 dB SNDR at Nyquist with >2.6 GHz ERBW after calibration. The ADC with CI sampler consumes 7.62 mW, leading to a Walden FoM of 70.8 fJ/conversion-step.**

Keywords— Time-interleaved ADC, current integrating sampler, background calibration, timing skew.

I. Introduction

The time-interleaved (TI) topologies have been widely explored in high-speed, moderate-resolution ADCs [1]-[9]. However, nonidealities from the TI sampling front-end, e.g., due to kick-back and sampling time skew, are often limiting the performance of such converters. A buffer can be placed before the sample-and-hold (S/H) circuit to reduce its kick-back [1][2][8], but the added power is a costly investment, given that the buffer acts merely as a unity-gain element. The issue of sampling time skew is a similarly costly issue, since its detection is significantly more difficult than measuring gain and offset mismatches among TI channels [1]. While it is possible to infer the time skew using a reference-free autocorrelation approach [3][4], this solution is limited to scenarios where the input closely resembles wide-sense stationarity. Alternatives that alleviate this issue use a window detector [5] or a reference channel [6]. However, the added circuitry is prone to injecting asynchronous input disturbances [4].

In this paper, we adopt a current integrating sampler [10] to address the above-described challenges. In addition to input buffering, the CI sampler provides anti-alias filtering and simultaneously enables reference-free time skew detection. Unlike other self-referenced schemes [3][4], the proposed calibration approach works under various input conditions and does not require wide-sense stationarity. Our prototype design with CI sampler front-end achieves ERBW > 2.6 GHz and exhibits 36.4 dB SNDR at Nyquist input, consuming only 7.62 mW total power with the CI sampler power included. The Walden FoM is 70.8 fJ/conversion-step based on the SNDR at Nyquist.

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II. TI-ADC Architecture and CI Sampler Overview

A. TI-ADC Architecture

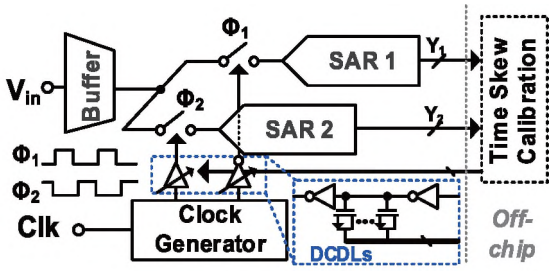

Fig. 1. Block diagram of a two-way TI-SAR ADC.

Fig. 1 depicts the two-way TI-SAR architecture used in our design. It consists of the CI-based input buffer, clock generator, two SAR ADCs that were re-used from [9], digitally controlled delay lines (DCDLs) and a time skew calibration block. The time skew information is extracted off-chip with the proposed calibration algorithm based on the ADC output codes. The input buffer alleviates the kick-back effect from the switched-capacitor sampler and provides a time-invariant input impedance. Conventionally, the buffer implemented with a source follower (SF) [1][8] tends to be power hungry given the stringent bandwidth requirement dictated by short sampling windows. In this work, we adopt the CI-based buffer to relax such power tradeoff [10], and simultaneously benefit from its inherent anti-alias filtering and time-to-voltage conversion for skew detection.

B. Overview of CI Sampler and its Characteristics

Fig. 2 illustrates the block diagram of the CI sampler with its corresponding timing strategy. First, let's consider the model without the capacitor (C_I). The CI sampler circuit consists of a Gm cell followed by the integration-and-hold path which comprises two switches with non-overlapping phases (Φ_S and Φ_r). Different from the voltage sampler, the sampling voltage

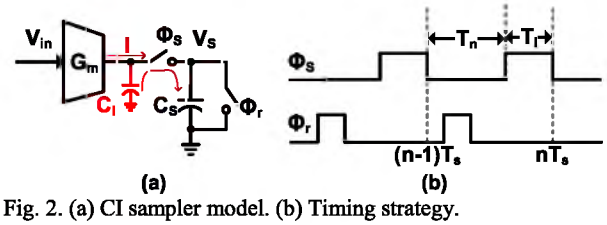

Fig. 2. (a) CI sampler model. (b) Timing strategy.

(V_S) must be fully reset before the next integration cycle to eliminate inter-symbol-interference (ISI). In the CI sampler structure, V_S not only depends on the input signal (V_{in}) and the transconductance (G_m) but also the integration time (T_I) and sampling capacitor (C_S). The sampled voltage can be expressed as:

$$V_S(n) = \frac{G_m}{C_S}\int_{nT_S-T_I}^{nT_S} V_{in}(t)\,dt, \tag{1}$$

where T_S is the sampling clock period. The impulse response of the integration process in (1) is a periodic rectangular window function whose window width and height are T_I and G_m/C_S [7], respectively. Accordingly, the frequency response is:

$$|H(f)| = \frac{G_m \cdot T_I}{C_S}\left|\frac{\sin(\pi \cdot T_I \cdot f)}{\pi \cdot T_I \cdot f}\right|. \tag{2}$$

When considering C_I in the sampling process, unlike the C_S, the C_I is still charged by the Gm cell during $\Phi_S = 0$, time slot that we call idle time (T_n) as shown in Fig. 2(b). The charge stored at C_I during the idle time will be shared to C_S at the next sample, thus leading (1) to:

$$V_S(n) = \frac{G_m}{C_I+C_S}\int_{nT_S-T_I}^{nT_S} V_{in}(t)\,dt + \frac{G_m}{C_I+C_S}\int_{(n-1)T_S}^{(n-1)T_S+T_n} V_{in}(t)\,dt + \frac{C_I}{C_I+C_S}V_S(n-1). \tag{3}$$

The first order FIR filter of the CI sampler provides an anti-aliasing function and cascades with an IIR filter (the 1st + 2nd term in (3)) introduced by the charge-sharing process between C_I and C_S [7]. The 3rd term in (3) is the unwanted ISI while its effect is not significant and can be compensated with little power overhead in the Gm cell of our design. It can be recognized from (3) that V_S is not only dependent on T_I but also T_n. Such characteristic enables the proposed time skew calibration (detailed next). Assuming r_o is the output resistance of the G_m cell, the transfer function of the CI sampler becomes:

$$H(s) = \frac{G_m}{(C_I+C_S)}\frac{1-e^{-(s+1/\tau)T_I}}{(s+1/\tau)}, \tag{4}$$

where $\tau = r_o(C_S+C_I)$ is the time constant. The depth of the nulls determines the attenuation ability of the FIR filter:

$$\frac{|H(m/T_I)|}{|H(0)|} \approx \frac{1}{m\pi}\left(1+\frac{T_I}{2\tau}\right)\frac{T_I}{2\tau}, \tag{5}$$

where m is an integer that denotes the location of the mth null. In this work, C_I is about 60 fF due to the parasitics of the G_m cell and routing, leading to an extra ~15 dB attenuation at the 1st null.

III. Timng Skew Calibration

A. Time Skew in TI-CI Sampler

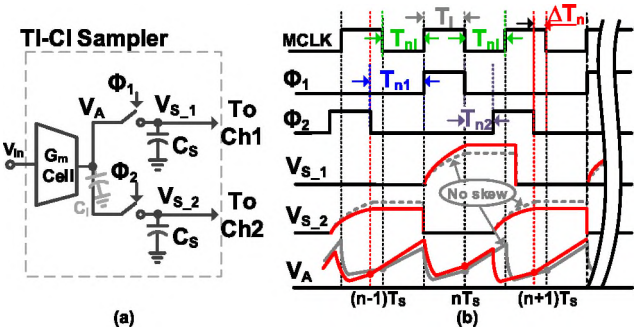

Fig. 3. (a) Block diagram of the TI-CI sampler. (b) Time diagram of the TI-CI sampler.

Fig. 3(a) displays the block diagram of the TI-CI sampler front-end, which consists of a G_m cell and two integration-and-hold channels followed by two sub-ADCs. V_{S_1} and V_{S_2} are the TI-CI sampler voltages from channel 1 and 2, respectively. Fig. 3(b) shows its timing diagram and the time skew detection concept. The master-clock (MCLK) is the sampling clock and T_S is its clock period. T_{n1} and T_{n2} are the idle times of the two channels in which none of them are in the integration mode and they are identical without time skew error. Due to the characteristic of the CI sampler as denoted in (3), the integrated charge on C_I (Q_I) also depends on the duration of the idle time. When the interleaved sampling clock suffers from time skew, the idle time of each channel deviates from the ideal value (T_{ni}) that affects Q_I. Furthermore, such charge eventually passes to C_S (from C_I) at the next sample, therefore altering the sampling voltage and mapping the time skew into the amplitude domain.

As exemplified in Fig. 3(b), channel 2 suffers from time skew with a leading time ΔT_n that reduces the idle time of channel 2 (T_{n2}) from T_{ni} to $T_{n2} = T_{ni}-\Delta T_n$, and the idle time of channel 1 increases to $T_{n1} = T_{ni}+\Delta T_n$. Fig. 3 (b) shows the voltage on C_I (V_A) with different idle times. V_A tends to become larger with longer T_{n1} and smaller with shorter T_{n2}. Then, the error of V_A resulting from the time skew transfers to (charge sharing between C_I and C_S) V_{S_1} and V_{S_2} during Φ_1 and Φ_2, respectively. The sample of channel 1 and 2 (V_{S_1} and V_{S_2}) with time skew can be expressed in a form similar to (3). It is worth observing that the time skew only affects the second term in (3), and the sampling voltage of the two channels can be rewritten as (6) and (7), respectively.

$$V_{S\_1}(n) = \frac{G_m}{C_I+C_S}\left(\int_{(n-1)T_S}^{nT_S} V_{in}(t)\,dt + \int_{(n-1)T_S-\Delta T_n}^{(n-1)T_S} V_{in}(t)\,dt\right) + \frac{C_I}{C_I+C_S}V_{S\_2}(n-1), \tag{6}$$
$$\approx \frac{G_m}{C_I+C_S}\int_{(n-1)T_S}^{nT_S} V_{in}(t)\,dt + \frac{G_m \cdot V_{in}((n-1)T_S)}{C_I+C_S}\Delta T_n + \frac{C_I}{C_I+C_S}V_{S\_2}(n-1)$$

$$V_{S\_2}(n) = \frac{G_m}{C_I+C_S}\left(\int_{nT_S}^{(n+1)T_S} V_{in}(t)\,dt - \int_{(n+1)T_S-\Delta T_n}^{(n+1)T_S} V_{in}(t)\,dt\right) + \frac{C_I}{C_I+C_S}V_{S\_1}(n), \tag{7}$$
$$\approx \frac{G_m}{C_I+C_S}\int_{nT_S}^{(n+1)T_S} V_{in}(t)\,dt - \frac{G_m \cdot V_{in}((n+1)T_S)}{C_I+C_S}\Delta T_n + \frac{C_I}{C_I+C_S}V_{S\_1}(n)$$

The second terms of (6) and (7) are the sampling voltage errors with time skew. From (6) and (7), it can be seen that $|V_{S\_1}|$ and $|V_{S\_2}|$ are proportional (with reversed polarity in channel 1 and 2) to the amount of time skew ΔT_n. As depicted in the example in Fig. 3(b), with a smaller T_{n2} and larger T_{n1}, $|V_{s\_1}|$ increases and $|V_{s\_2}|$ decreases. Consequently, the skew information is inherently transferred into the amplitude domain.

B. Proposed Time Skew Calibration Algorithm

From (6) and (7), the CI sampler front-end allows the time skew to be observed in the amplitude domain. On the other hand, a simple amplitude detection scheme at the ADC outputs (Y_1 and Y_2 in Fig. 1), such as max/min function, fails to provide sufficient accuracy as it can be easily affected by both quantization and thermal noises. To mitigate such impacts, we use the sample variances of Y_1 and Y_2 as skew estimators. These quantities are robust to ADC noise due to the inherent averaging in computing the sample statistics. Correspondingly, the convergence condition of the proposed calibration becomes,

$$Var(Y_1) - Var(Y_2) \approx \frac{8\sigma_0^2 \left[C_I/(C_I + C_S)\right]}{1 + \left[C_I/(C_I + C_S)\right]^2} \cdot \frac{\Delta T_n}{T_S}, \qquad (8)$$

where σ_0^2 is the digitized output variance without time skew. Then, it can be affirmed that the variance difference among the channels is proportional to the time skew. We calculate the variance between channels 1 and 2 from the sub-ADCs' outputs with the digitally controlled delay lines managed to minimize the difference among the variances.

As the proposed scheme extracts time mismatch from the amplitude domain, it exhibits certain different characteristics relative to its time-domain counterparts [3]-[6]. First, it does not require an extra reference channel or window detector information that minimizes the analog circuit modification overhead. Second, the proposed calibration ability does not rely on specific input properties while correlation-based schemes [3][4] need to approximate a wide-sense stationary input. Nevertheless, the input characteristic affects the convergence time of our calibration. Unlike the time-domain approach where the largest voltage error occurs at the zero-crossing region with the steepest slope, the largest error of the proposed scheme happens when the largest amount of charge accumulates on C_S during ΔT_n. Therefore, the detection of ΔT_n is more sensitive with a low input frequency where the integration area under ΔT_n interval is relatively large, requiring less samples to converge for the same accuracy. Fig. 4 plots the behavioral simulated result of the convergence at different input frequencies with similar quantization and thermal noise in this design. At high input frequency, the same calibration accuracy requires the double number of samples.

IV. Circuit Implementation

Fig. 5 depicts the schematic of the CI sampler front-end circuit. The main design considerations of the G_m cell are the transconductance (G_m), parasitic capacitance (C_I), linearity and noise. We design G_m to match the desired gain in conjunction with T_I as well as C_S. The r_o and parasitic capacitance must be designed cautiously since they lead to a deterioration in the bandwidth and gain of the CI sampler. To minimize these

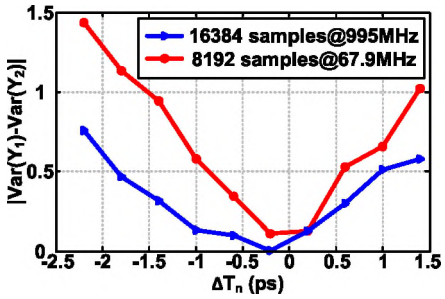

Fig. 4. Simulated convergence of variance versus time skew.

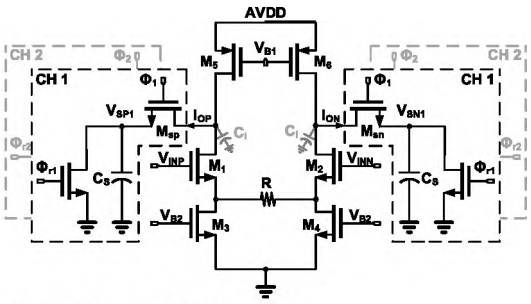

Fig. 5. CI sampler front-end circuit.

impacts we adopt a single-stage class-A architecture to implement the G_m cell, whose circuit structure determines the linearity of the CI sampler front-end; therefore, we add a source degeneration resistor (R) between the sources of M_1-M_2. In this work, C_S is 64 fF with a full swing of ~ 0.8 V peak-to-peak.

V. Measurement Results

Fig. 6 exhibits the chip micrograph of the 7-bit TI-ADC prototype fabricated in 28 nm CMOS. Its active area is 80 µm × 103 µm which includes two ADC channels with background offset calibration [9], a G_m cell buffer and a clock generator with tunable delay.

Fig. 7 shows the measured variance difference among channels (16384 samples/channel) at different input rates against the DCDL control code. When the variance difference approaches zero, it minimizes the time skew. Fig. 8 displays the measured frequency response of the CI sampler. The first notch of the CI sampler at 5.5 GHz reaches -20 dB to reject aliasing and the achieved bandwidth is around 2.25 GHz. With a T_I of 180 ps in this design, the location of the first null should be ideally at 5.55 GHz, but experiences a slight deviation due to process and mismatch effects. Fig. 9 plots the measured SNDR/SFDR versus input frequency and we obtain an ERBW>2.6 GHz. Fig. 10 depicts the ADC output spectrum at Nyquist before and after the proposed calibration. The spur from time skew reduces by more than 20 dB, and the SNDR improvement is around 8.5 dB. The maximum |DNL| and |INL| are < 1 LSB and 1.5 LSB, respectively. The power of the ADC core and clock generation is 5.58 mW, with 0.9 V power supply. The G_m cell consumes 2.04 mW from a 1.2 V supply. Table I summarizes and compares the proposed design with state-of-the-art ADCs that have an input buffer and similar

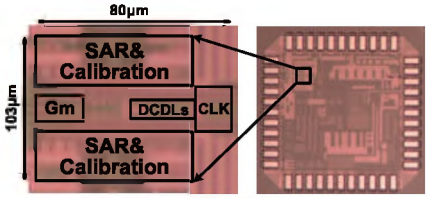

Fig. 6. Chip microphotograph.

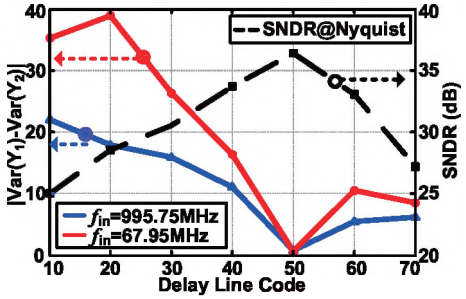

Fig. 7. Measured SNDR and variance difference versus skew calibration code.

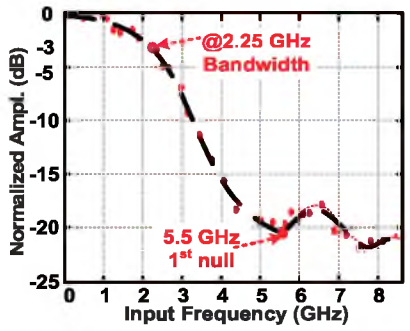

Fig. 8. Measured CI sampler frequency response.

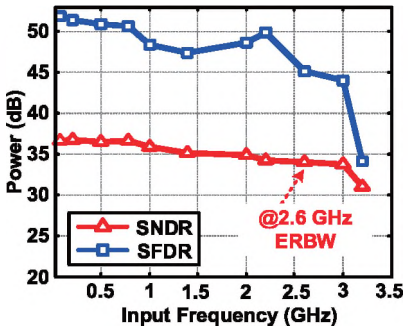

Fig. 9. Measured SFDR/SNDR versus input frequency.

specifications. Our design reaches the best energy efficiency with additional anti-aliasing ability.

VI. Conclusions

A 7b 2 GS/s 2-way TI-SAR ADC with CI sampler front-end and background time skew calibration has been presented. The CI sampler acts as an input buffer and simultaneously enables anti-aliasing and time skew calibration ability. The proposed calibration does not require an auxiliary channel and is insensitive to the input signal statistics. The ADC achieves Walden FoM of 70.8 fJ/conv-step with input buffer at Nyquist, which is superior to state-of-the-art designs.

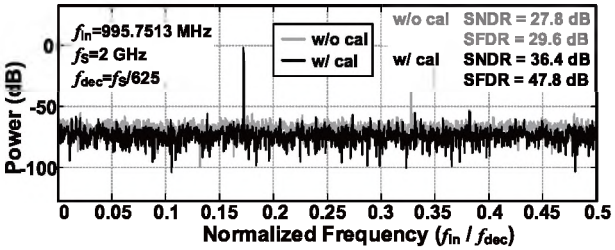

Fig. 10. Measured FFT before and after gain, offset and time skew calibration (8192 samples after decimation by 625).

TABLE I. Comparison with State-of-the-Art Designs

	CICC 2014[1]	JSSCC 2017[2]	JSSCC 2012[8]	This work
Architecture	TI-SAR	TI-SAR	TI-Subranging	TI-SAR
Technology (nm)	40	40	65	28
f_s (GS/s)	2.64	2	2.2	2
Resolution	8	8	7	7
Supply voltage (V)	1.2	2.5/1.1	1	1.2/0.9
SNDR (dB) @Nyquist	38	39.4	38	36.4
Power (mW)	39	48.5	38	7.62
FoM (fJ/conv.step)	230	318	269.9	70.8
Area (mm^2)	0.18	0.54	0.3	0.0[illegible]
Anti-aliasing filter	No	No	No	Yes

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