

# An 8-bit 0.7-GS/s Single Channel Flash-SAR ADC in 65-nm CMOS Technology

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**Abstract**—This paper presents the prototype of a single channel 8-bit 0.7-GS/s A/D converter implemented in a 65-nm CMOS process. The required thresholds are generated from the resistive interpolation embedded within the preamplifier preceding the latches. The active area of the chip is  $150 \times 220 \mu\text{m}^2$  and the total power consumption is 5.96 mW. At Nyquist, the ADC achieves 6.62 ENOB, resulting in a figure of merit equal to 86.7 fJ/conversion-step.

## I. INTRODUCTION

Ultra high-speed data converters operating at tens of GS/s use time-interleaved structures for pushing forward the single channel bandwidth limits, [1], [2]. Flash architectures for the core ADCs are an unsuitable solution for resolutions above 6 bits. Instead, the SAR architecture is a convenient choice because of its simple structure and low power consumption. Moreover, modern technologies allow relatively high conversion rates.

The speed of an N-channel time-interleaved structure is N times the conversion-rate of a single channel. A possible strategy is to choose a large interleaving factor. However, integrating many channels turns problematic the clock distribution with unavoidable clock skew that limits the resolution and generates spurious tones. The clock skew causes a non-periodic input sampling and, in order to compensate for the resulting errors, complex calibration methods must be used, [3]. A more effective strategy implies the choice of relatively low values of N and pushes the conversion rate of the single channel to the upper limit allowed by the technology. With 28-nm and 32-nm CMOS technologies, it is possible to exceed 0.7 GS/s, [4], [5]. The use of less advanced technology, like the 65-nm CMOS, enables lower conversion rates (400 MS/s with a two bit/step SAR architecture [6]).

This 65-nm ADC uses a flash-SAR architecture achieving a conversion speed of 700 MS/s with a maximum signal to noise and distortion ratio (SNDR) of 47.5 dB. The result, comparable with the one obtained with smaller line-widths, benefits from an architecture composed by the cascade of a 4-bit flash and a two-step SAR converter. Both steps determine 3-bit. The 4+3+3 bits originate the 8-bit output; the applied redundancy avoids calibration in the flash and in the first step of the SAR. The active area of the chip is  $150 \times 220 \mu\text{m}^2$  and the total power consumption is 5.96 mW.

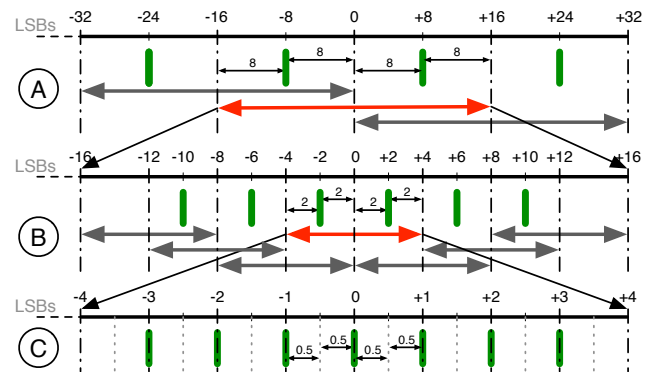


Fig. 1. Searching algorithm with redundancy. A: coarse phase, B: intermediate phase, and C: fine phase.

## II. SYSTEM IMPLEMENTATION

### A. Searching algorithm

Fig. 1 illustrates the conversion strategy. The quantization interval of the 4-bit flash converter is 16 LSBs ( $V_{FS}/16$ ). This allows an inaccuracy of  $\pm 8$  LSBs for the offset mismatch. Supposing that the flash locates the input signal within the interval  $\pm 8$  LSB, the first cycle of the SAR explores a wider range equal to  $\pm 16$  LSBs. Since the first SAR cycle determines 3 bits, the resulting quantization interval is 4 LSBs. The second SAR cycle explores an interval of 8 LSBs, granting a  $\pm 2$  LSBs of margin to the thresholds mismatch among the levels of the first cycle SAR. The second cycle of the SAR determines 3 LSBs.

Since the full scale voltage is  $1.2 V_{pp}$  and, consequently, the LSB is about 4.7 mV, a careful design and layout require a foreground calibration only for the thresholds used in the second SAR cycle.

### B. Architecture

Fig. 2 illustrates the block diagram of the architecture. A fully differential capacitive array and a single ended flash simultaneously perform the input sampling. The coarse conversion is carried out by the flash, whose output set the MSBs of the capacitive array. The generated residual is the input of a special preamplifier that provides 8+8 differential outputs. Half of these are the input of six fully differential latches whose outputs determine the three Intermediate Significant Bits (ISBs) of the first SAR cycle. The ISBs set the LSBs

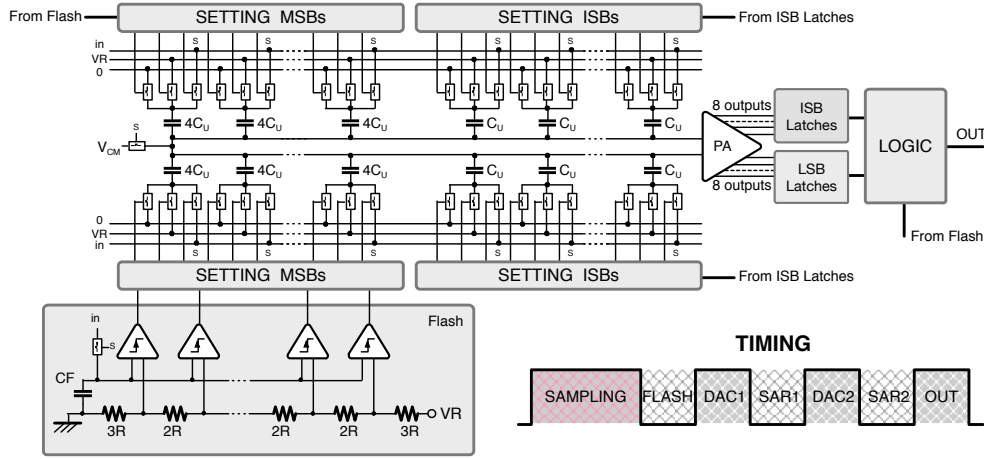


Fig. 2. Architecture of the proposed ADC.

section of the capacitive array. The new generated residual is fed into the preamplifier and, by using the other outputs, the remaining 3 bits are obtained. A simple digital logic combines the digital results to give rise to the 8-bit output.

The capacitive array has two sections, one formed by 14 capacitors of value  $4C_U$ , the other formed by 8 capacitors of value  $C_U$  for a total array of  $64C_U$ . The structure implements a 5-bit DAC suitable for the flash and for the first SAR cycle steps. Since the second SAR cycle determines three bits without using the array, the used approach reduces the capacitive array from  $256C_U$  to  $64C_U$  ( $-75\%$ ). The nominal value of  $C_U$  to satisfy the  $kT/C$  noise requirement is 9 fF ( $C_{TOT} = 576$  fF).

Fig. 2 also shows the timing of each stage for a complete conversion cycle. After sampling, the flash section carries out the first conversion step. Two subsequent phases (DAC+SAR) complete the remaining conversion steps. Finally, one time slot is allocated for the data out. In order to generate all the required phases, the converter needs an input clock and an internal phases generator with frequency twice the sampling frequency.

### C. Preamplifier with embedded thresholds generation

The small value of the quantization step in the two phases of the SAR conversion does not provide a reliable operation

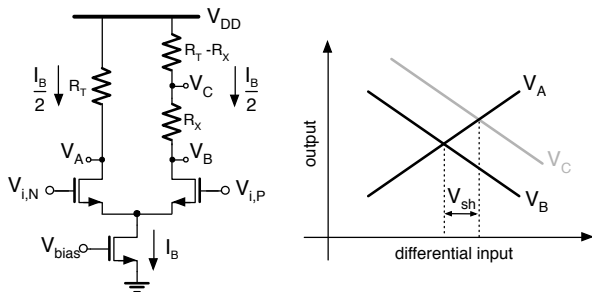


Fig. 3. Preamplifier with embedded thresholds generation.

for the latches. Therefore, a preamplifier is required. The need of preamplification has been combined with the request of generating the thresholds for the converter.

Fig. 3 describes the conceptual approach. It is a simple differential stage with resistive load, a circuit solution that grants high speed. The resistive load on the right branch is divided in two parts, so that equal voltages at nodes A and C require an input shift,  $V_{sh}$ , across the differential pair. Supposing that the shift causes a negligible signal current, it is necessary to have

$$2R_T g_m V_{sh} \approx R_X \frac{I_B}{2}$$

The preamplifier gain is

$$A_P = 2g_m R_T$$

The required shift voltage depends on the design quantities  $W/L$ ,  $I_B$ , and  $R_X/R_T$ . Suitable values of those parameters provide  $V_{sh} = \pm 1, \pm 2, \pm 3, \pm 6, \pm 10$  LSBs.

The accuracy of the shift depends on the accuracy and linearity of  $g_m$ , as the ratio among the resistors is well matched. For the first step of the SAR, the possible error is compensated for by the redundancy. For the second step, the circuit uses foreground calibration. The control of the bias current,  $I_B$ , provides a rough global calibration, before the fine calibration embedded in the latch. The nominal value of  $I_B$  is 500  $\mu$ A, ensuring very low power operation of the preamplifier.

Fig. 4 shows the schematic diagram of the multi-output preamplifier. It uses a single differential pair that can be connected to two resistive string loads, one for the first step of the SAR, the other for the second one. The values of the resistors optimize the gain for the two cases. The use of the same differential pair ensures a good matching of the operational conditions in the two modes. In order to prevent output voltages switching when the resistive load is not used, a dummy differential pair replaces the main structure in the disconnected resistive loads.

The output voltages drive the latches following the connection scheme shown in Table I. The latch structure is the one described in [7].

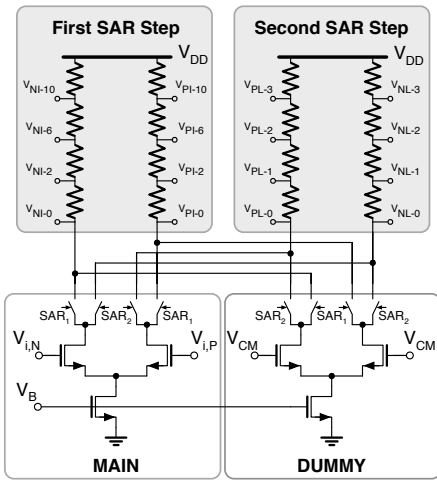


Fig. 4. Pre-amplifier schematic with dummy structure and double output branch.

TABLE I. LATCHES BANK CONNECTIONS TO PREAMPLIFIER OUTPUTS.

First SAR step latch	$V_{ip}$	$V_{in}$	Second SAR step latch	$V_{ip}$	$V_{in}$
-10 LSB	$V_{PL-0}$	$V_{NI-10}$	-3 LSB	$V_{PL-0}$	$V_{NL-3}$
-6 LSB	$V_{PL-0}$	$V_{NI-6}$	-2 LSB	$V_{PL-0}$	$V_{NL-2}$
-2 LSB	$V_{PL-0}$	$V_{NI-2}$	-1 LSB	$V_{PL-0}$	$V_{NL-1}$
+2 LSB	$V_{PL-2}$	$V_{NI-0}$	0 LSB	$V_{PL-0}$	$V_{NL-0}$
+6 LSB	$V_{PL-6}$	$V_{NI-0}$	+1 LSB	$V_{PL-1}$	$V_{NL-0}$
+10 LSB	$V_{PL-10}$	$V_{NI-0}$	+2 LSB	$V_{PL-2}$	$V_{NL-0}$
			+3 LSB	$V_{PL-3}$	$V_{NL-0}$

### III. MEASUREMENT RESULTS

This ADC has been fabricated in a 65-nm 1.2-V CMOS process. The design uses a standard multi-chip module of  $1000 \times 1500 \mu\text{m}^2$ , but the active area of the converter is  $150 \times 220 \mu\text{m}^2$ . Fig. 5 depicts the whole chip microphotograph and a magnified view of the active area where the main circuit blocks have been highlighted. The track & hold circuit is placed in the top part of the ADC. A tree structure brings the sampling clock and the input signals to the flash ADC and to the capacitive DAC. At the bottom, the pre-amplifier with the latches bank forms the comparators of the SAR ADC. The logic is distributed along the chip and does not occupy a significant amount of area.

Fig. 6 shows the SNDR measured with a full-scale sine wave input signal as a function of the sampling frequency for different supply voltages. At the nominal sup-

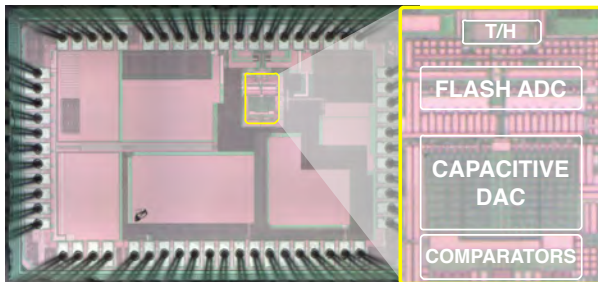


Fig. 5. Chip microphotograph.

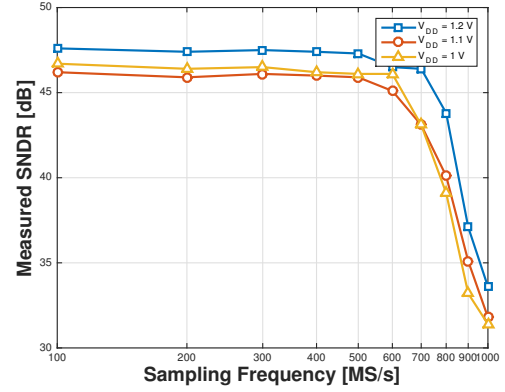


Fig. 6. Measured SNDR as a function of the sampling frequency for different supply voltages.

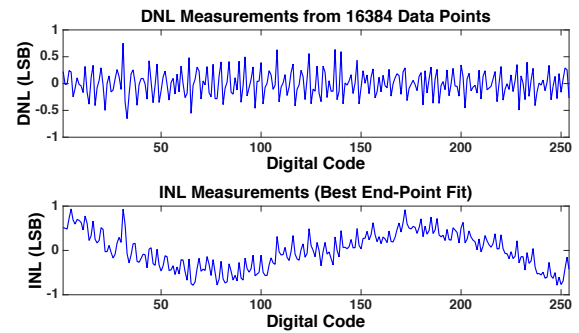


Fig. 7. Measured DNL and INL.

ply voltage ( $V_{DD} = 1.2 \text{ V}$ ), the ENOB is 7.5 bits up to  $f_s = 550 \text{ MS/s}$  and slightly drops at higher sampling frequencies. At  $f_s = 700 \text{ MS/s}$ , the ENOB is 7.4 bits. The figure shows that the circuit loses about 0.25 bit at lower supply voltages and shows a lower speed of operation.

Fig. 7 shows the measured DNL ( $[-0.65 : +0.75]$  LSBs) and the best fit INL ( $[-0.79 : +0.94]$  LSBs). In order to account for possible non-linearities occurring at high speed, the figures result from the histogram method with a sampling frequency as high as  $f_s = 700 \text{ MS/s}$ .

Fig. 8 and 9 give the measured output spectra for  $f_s$  equal to  $500 \text{ MS/s}$  and  $700 \text{ MS/s}$  when the input frequency is near Nyquist. The achieved SNDRs are 45.2 dB and 41.6 dB while the ENOBs are 7.22 bits and 6.62 bits, respectively. Third harmonic tones at  $-52 \text{ dB}_{FS}$  and  $-47 \text{ dB}_{FS}$  limit the spurious free dynamic range (SFDR). The FFTs have 16384 points and the outputs were decimated by 25x. Fig. 10 shows the measured SNDR at the nominal supply voltage as a function of the input signal frequency for different sampling frequencies.

The total power consumption is 5.96 mW ( $V_{DD} = 1.2 \text{ V}$ ). The figure of merit at  $f_s = 0.7 \text{ GS/s}$  is 86.7 fJ/conversion-step. Fig. 11 shows the power breakdown of the ADC, identifying in the digital section and the latches the power hungry part of the circuit. Scaling down the technology to 32 nm would reduce by a factor 4 that contribution, with a reduction of the consumed power by about 45%.

Table II summarises the ADC performance and provides a

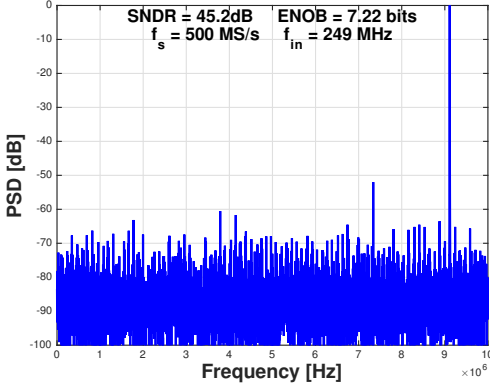


Fig. 8. Measured output spectrum at  $f_s = 500$  MS/s. (Output decimated by 25x).

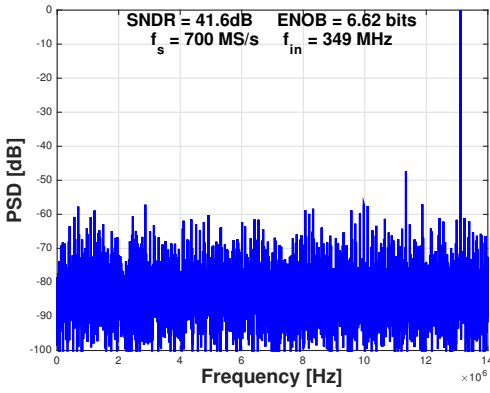


Fig. 9. Measured output spectrum at  $f_s = 700$  MS/s. (Output decimated by 25x).

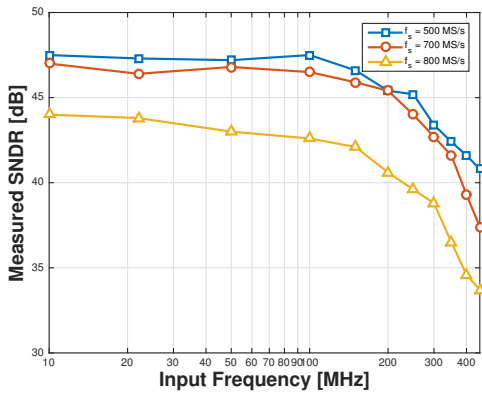


Fig. 10. Measured SNDR as a function of the input frequency for different sampling frequencies.

comparison with state-of-the-art single channel SAR ADCs. This work results faster than latest single channel ADCs presented in the same technology node with 8-bit resolution.

#### IV. CONCLUSIONS

In this paper, the prototype of a 700 MS/s single channel Flash-SAR ADC in 65-nm CMOS process was presented. A

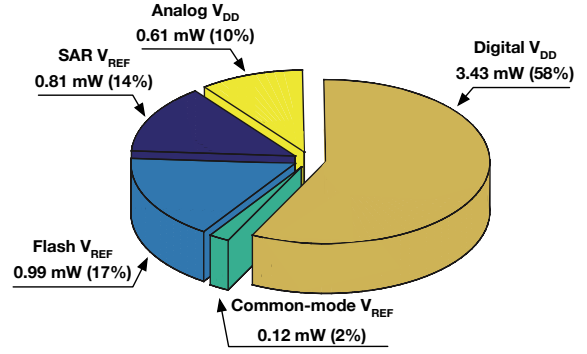


Fig. 11. Power breakdown of the ADC.

TABLE II. PERFORMANCE SUMMARY AND COMPARISON TABLE.

	[4]	[5]	[6]	<b>This Work</b>
Technology	28 nm	32 nm	65 nm	<b>65 nm</b>
Resolution	<b>8 bits</b>			
Supply Voltage	1 V	1 V	1.2 V	<b>1.2 V</b>
SNDR near Nyquist	43.3 dB	39.3 dB	44.5 dB	<b>41.6 dB</b>
Sampling Speed	0.75 GS/s	1.2 GS/s	0.4 GS/s	<b>0.7 GS/s</b>
Power	4.5 mW	3.06 mW	4 mW	<b>5.96 mW</b>
FoM/conv.-step	50 fJ	34 fJ	73 fJ	<b>86.7 fJ</b>
Area	0.004 mm <sup>2</sup>	0.0015 mm <sup>2</sup>	0.024 mm <sup>2</sup>	<b>0.03 mm<sup>2</sup></b>

multi-bit per cycle searching algorithm is used in order to speed up the conversion. Redundancy and a novel resistive interpolated preamplifier are implemented to overcome the thresholds generation limit and to reduce the calibration procedure complexity.

#### ACKNOWLEDGEMENTS

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