21.6 A 0.016mm² 144µW Three-Stage Amplifier Capable of Driving 1-to-15nF Capacitive Load with >0.95MHz GBW

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High-color-depth LCD drivers require nF-range capacitors as the charge reservoirs to handle the glitch energy during the conversion of the DAC [1]. The reference buffers based on multi-stage amplifiers can enhance the precision under low-voltage supplies, but are exposed to instability when loaded by such large capacitive loads (C_L). Frequency compensation via damping-factor control [2] is capable of extending the C_L-drivability up to 1nF, however, at the cost of penalizing the power (426µW) and area (0.14mm²). Although recent works [3-4] have enhanced gain-bandwidth product (GBW) and slew rate (SR) showing better FOM_S (=GBW·C_L/Power) and FOM_L (=SR·C_L/Power), the C_L-drivability has not been improved (i.e., 0.8nF in [3] and 0.15nF in [4]). This paper describes a three-stage amplifier managed to afford particularly large and wide range of C_L (1 to 15nF) with optimized power (144µW) and die size (0.016mm²), being very suitable for compact LCD drivers [5] with different resolution targets. The design barriers are methodically surmounted via *local feedback loop (LFL) analysis* expanded from [6], which is an insightful control-centric method. Measured at 15nF C_L, the attained FOM_S (FOM_L) is >4.48× (>2.55×) beyond that of the state-of-the-art (Fig. 21.6.1).

Design of frequency compensation classically hinges on the analysis of amplifier's transfer function H(s) once a potential topology is conceived [2-4]. Yet, the involvements cannot explicitly relate the impact of each circuit element to the pole-zero composition of H(s). In contrast, the LFL analysis upgrades the entire *pole-zero placement* to a more discerning system level, as materialized in the design of two-stage amplifiers [6]. This work extends the capability of LFL analysis to handle more complex three-stage amplifiers, allowing systematic selection of frequency compensation and comparison of merits.

Figure 21.6.2 shows the topologies of the three-stage amplifier in [3], [4], and this work. The Bode plots of their LFL are depicted in Fig. 21.6.3. Essentially, if no right-half-plane (RHP) pole appears in the LFL(s) of the amplifier (normally the case), its GBW is mainly governed by the unity-gain frequency (ω_μ) of the dominant LFL. LFL analysis shows that the $\omega_{\mu,[3]}$ in [3] is mainly contributed by the current-buffer Miller compensation (CBMC) on the outer LFL (inner LFL with G_{ma2} shows a loop gain <1). Though the LFL stability can be assured by pushing the original g_{o1}/C_{p1}-pole to a lower-frequency (g_{o1}/C_1), $\omega_{\mu,[3]}$ is still limited by the g_{o2}/C_{p2}-pole. This inspection explains why extra compensation (via C_1) and a low-gain G_{m2} were enforced in [3], offsetting the increment of $\omega_{\mu,[3]}$ offered by CBMC. The feedforward stage (G_{mf2}) only generates a high-frequency zero that has negligible impact to $\omega_{\mu,[3]}$.

The $\omega_{\mu,[4]}$ in [4] is obtained via single Miller compensation (SMC) and parasitic-pole cancellation. The latter is based on a passive left-half-plane (LHP) zero made by R_a and C_a to cancel the g_{o1}/C_m-pole, while pushing the original g_{o2}/C_{p2}-pole to a lower frequency g_{o2}/C_a. The extent of $\omega_{\mu,[4]}$ is associated with G_{m2} and R_a. Enlarging the former unavoidably calls for extra power, while the latter is upper-bounded by the LFL stability (due to the $1/R_aC_{p2}$-pole) and the criteria necessary to produce the LHP zero. Nevertheless, under the same C_L and power budget (i.e., G_{mL}), the $G_{m2}R_a$ term of $\omega_{\mu,[4]}$ can still exceed the term $(G_{m2}/g_{o2})(C_m/C_1)$ in $\omega_{\mu,[3]}$, where C_m/C_1 is limited to ~2. This insight is consistent with their reported results.

Guided by those LFL analyses, this work benefits the CBMC for its high-frequency parasitic pole, while combining it with a tailored active-LHP-zero circuit for parasitic-pole cancellation. Specifically, a high-pass network (R_z, C_z and G_{mb1}) with low output impedance offers the sought LHP zero without introducing unwanted low-frequency poles, resolving the shortcoming of its passive counterpart [4]. The loop gain of the LFL compresses the pole-zero doublet so as to suppress the slow-settling component in the step response. G_{mb2} not only offers V-to-I conversion for driving G_{mL}, but also isolates V_2 and V_3 nodes to limit C_{pb} ($<<C_{p2}$), resulting in a high-frequency $1/R_zC_{pb}$-pole. Unlike [3] and [4], $\omega_{\mu,proposed}$ is mainly limited by the G_{mb1}/C_z-pole, which sits at a much higher frequency than the g_{o2}/C_{p2}-pole in [3], and the $1/R_aC_{p2}$-pole in [4]. As a result, $\omega_{\mu,proposed}$ can surpass $\omega_{\mu,[3]}$ and $\omega_{\mu,[4]}$ under the same C_L and power budget.

Figure 21.6.4 depicts the circuit-level schematic of the proposed three-stage amplifier. The 1st-gain-stage G_{m1} features an input differential pair ($M_{1\text{-}2}$). A wideband current buffer G_{ma} ($M_{3\text{-}8}$ and $R_{1\text{-}2}$) [7] offers a low input impedance of $1/[2(g_{m5}R_1+1)g_{m8}]$, pushing the G_{ma}/C_m-pole to higher frequencies while averting reducing the output impedance of G_{m1} (drain of M_7 and M_8). The LFL of the current buffer features a moderate self loop gain ($2g_{m5}R_1+1$) to impel its own poles to high frequencies while ensuring local stability. The active LHP zero (R_z and C_z) is embodied in the 2nd-gain-stage G_{m2} ($M_{11\text{-}14}$) to spare power. G_{mb1} and G_{mb2} are realized by M_{13} and M_{14}, respectively. M_{12} (driven by M_9) offers a feedforward gain enhancing the slewing performance of G_{m2}. The 3rd-gain-stage G_{mL} (M_{15}) is combined with another feedforward gain G_{mf} (M_{16}). Targeting a >1nF C_L the SR of the amplifier is dominated by the maximum dynamic current of the 3rd gain stage, which can be designed to afford a certain amount of resistive load (e.g., add 30% quiescent current for 25kΩ) without affecting other performances.

The fabricated three-stage amplifier is optimized for C_L drivability such that the power and area remain comparable with the recent works [3,4]. The measured AC and step responses are plotted in Fig. 21.6.5. C_L can be as large as 15nF with 18.1dB gain and 52.3° phase margin, and as small as 1nF with 9.8dB gain and 83.2° phase margin. The extrapolated DC gain is >100dB. At C_L=15nF, the GBW is 0.95MHz, whereas the average SR and 1% setting time (T_S) measured in unity-gain configuration are 0.22V/µs and 4.49µs, respectively. Although the measured gain (7.8dB) and phase (79.5°) margins are not inferior when C_L is reduced to 0.5nF, a small (~0.9mV_{pp}) high-frequency (~12MHz) ringing is superimposed onto the step response, due to the LFL instability. This result is consistent with the design and simulation, giving more insight when judging the C_L variability. When C_L is further downsized to 0.1nF, both the LFL and the amplifier (in unity-gain feedback) become unstable, as two complex conjugate RHP poles have already appeared in H(s).

Figure 21.6.6 shows the performance summary. This work not only succeeds in extending the C_L-drivability to 15nF, but also shows improved FOM_S (>4.48×) and FOM_L (>2.25×), and their large-capacitive-load versions [3]: LC-FOM_S (>2.76×) and LC-FOM_L (>1.57×), with respect to the prior arts. The die occupies 0.016mm² in a 0.35µm CMOS process (Fig. 21.6.7). The robustness of the results has been confirmed through performing measurements on over 20 samples. At 15nF C_L, the σ of each key performance parameter is <13% of its mean.

Acknowledgements:
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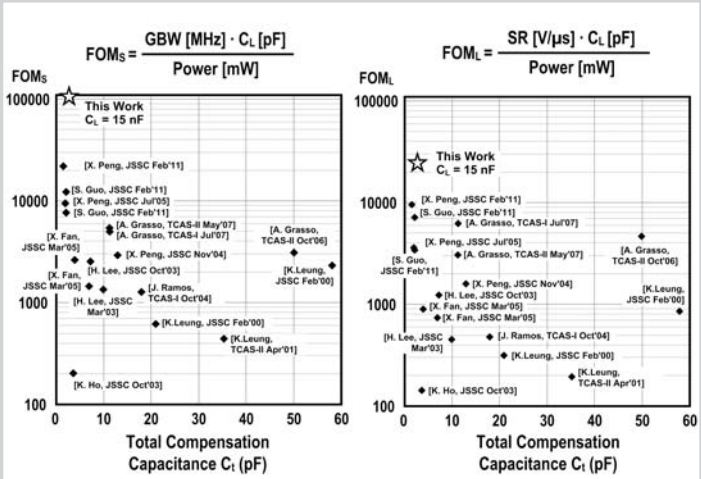


Figure 21.6.1: Benchmark of the state-of-the-art multi-stage amplifiers. This work shows improved FOM_S and FOM_L, while entailing small area (compensation capacitance C_t).

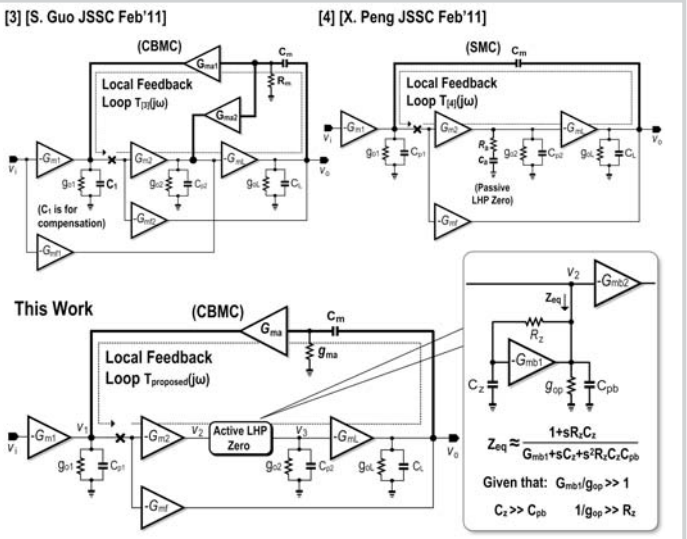


Figure 21.6.2: Three-stage amplifiers in [3], [4] and this work. "x" denotes loop break point.

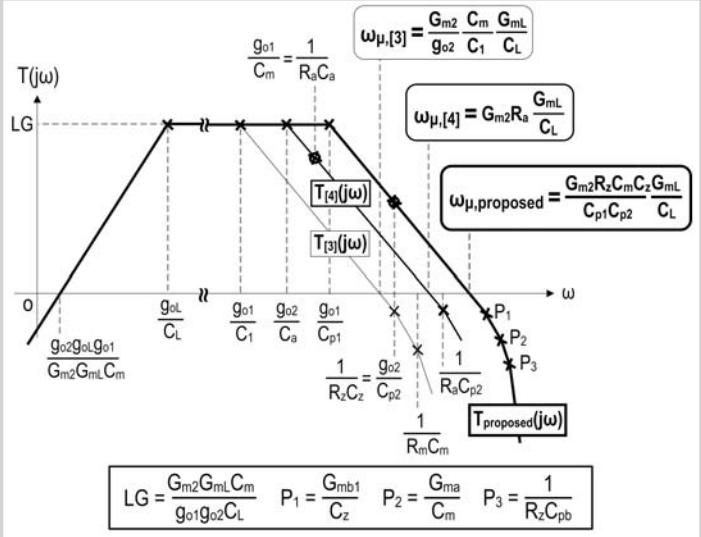
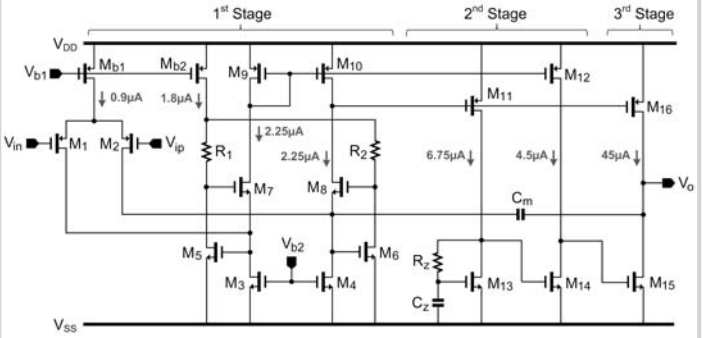


Figure 21.6.3: Bode plots of the three local feedback loops presented in Fig. 21.6.2.



Device	Size (μm/μm)	Device	Size (μm/μm)	Device	Size (μm/μm)
M_1/M_2	12/2 (x8)	M_{12}	3/1 (x4)	M_{b2}	6/2 (x2)
M_3/M_4	4/2 (x3)	M_{13}	1.5/0.6 (x3)	C_m	1.424 pF
M_5/M_6	1/0.35 (x3)	M_{14}	1.5/0.6 (x2)	C_z	1.219 pF
M_7/M_8	1/0.35 (x4)	M_{15}	1.5/0.6 (x20)	R_1, R_2	85.7kΩ
M_9/M_{10}	3/1 (x2)	M_{16}	3/1 (x40)	R_z	239.9kΩ
M_{11}	3/1 (x6)	M_{b1}	6/2		

Figure 21.6.4: Schematic and device sizes of the proposed three-stage amplifier. The bias currents are design values.

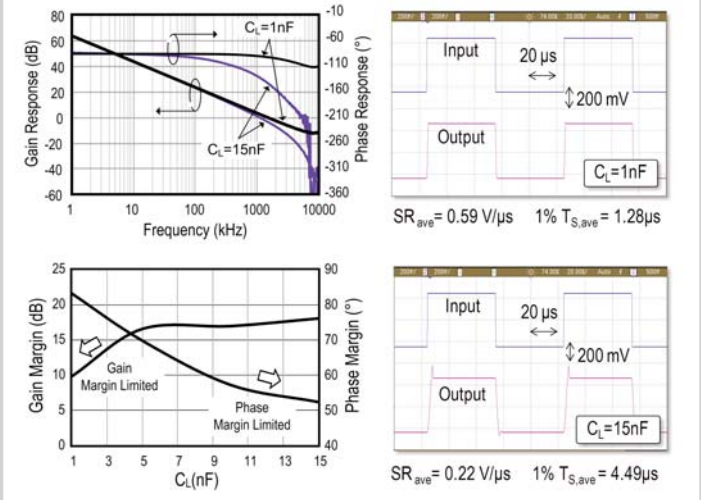


Figure 21.6.5: AC responses (left, upper) and step responses (right) at 1 and 15nF C_L. A small C_L limits the gain margin whereas a large C_L limits the phase margin (left, lower).

	[3] [S. Guo JSSC Feb'11]		[4] [X. Peng JSSC Feb'11]	This Work			
Load C_L (pF) [// R_L (kΩ)]	500 // 25	800 // 25	150	1,000	5,000	10,000	15,000
GBW (MHz)	4	3.6	4.4	1.37	1.24	1.06	0.95
Phase Margin (°)	70	58	57	83.2	69.8	57.2	52.3
Gain Margin (dB)	14 *	16 *	5 *	9.8	16.6	17.0	18.1
Average SR (V/μS)	2.2	1.7	1.8	0.59	0.50	0.30	0.22
Average 1% Ts (μS)	0.6	0.7	1.9	1.28	1.71	3.66	4.49
DC Gain (dB) (extrapolated)	>100		110	>100			
Power (μW) @ V_{DD}	260 @ 2 V		30 @ 1.5 V	144 @ 2 V			
Total Capacitance C_t (pF)	2.2		1.6	2.6			
Chip Area (mm^2)	0.014		0.02	0.016			
Technology	0.35μm CMOS		0.35μm CMOS	0.35μm CMOS			
FOM_S [(MHz · pF)/mW]	7,692	11,077	22,000	9,514	43,056	73,889	98,656
FOM_L [(V/μS · pF)/mW]	4,231	5,231	9,000	4,097	17,326	20,833	22,917
LC-FOM_S (MHz/mW)	3,497	5,035	13,750	3,659	16,560	28,419	37,945
LC-FOM_L [(V/μS)/mW]	1,923	2,378	5,625	1,576	6,664	8,013	8,814

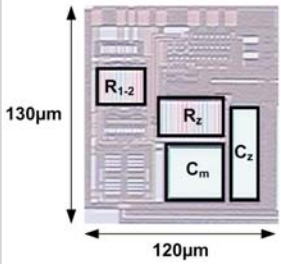
Typical FOM_S and FOM_L [3]-[4]:

$$FOM_S = \frac{GBW \cdot C_L}{Power}, \quad FOM_L = \frac{SR \cdot C_L}{Power}$$

Large-Capacitive-Load FOM_S and FOM_L [3]:

$$LC\text{-}FOM_S = \frac{GBW}{Power} \cdot \frac{C_L}{C_t}, \quad LC\text{-}FOM_L = \frac{SR}{Power} \cdot \frac{C_L}{C_t}$$

Figure 21.6.6: Performance summary and comparison. " * " denotes extracted values from plots.



20 chips, C_L=15nF	Mean	σ	$\frac{\sigma}{\text{Mean}}$ x 100%
GBW (MHz)	0.85	0.062	7.3%
Phase Margin (°)	53.2	2.64	5.0%
Gain Margin (dB)	19.96	1.42	7.1%
Average SR (V/µS)	0.21	0.014	6.7%
Average 1% Ts (µS)	4.77	0.21	4.4%
Power (µW)	140	14	10.0%
FOM_S [(MHz · pF)/mW]	89,290	10,888	12.2%
FOM_L [(V/µS · pF)/mW]	22,528	2,920	13.0%
LC-FOM_S (MHz/mW)	34,342	4,188	12.2%
LC-FOM_L [(V/µS)/mW]	8,661	1,123	13.0%

Figure 21.6.7: Chip micrograph. 20 chips were measured to confirm the robustness of the results.

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