A High Voltage Zero-static Current Voltage Scaling ADC Interface Circuit for Micro-Stimulator

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***Abstract*—This paper describes a SAR ADC interface circuit, where the input sensing voltage from a bipolar high voltage domain is linearly translated into the low voltage domain where the SAR ADC operates. The proposed interface circuit employs the principle of charge transfer amplifier to deliver information between two different power domains, in one step, without static power consumption, even if both domains do not share the the same ground voltages. To implement the charge transfer scheme using standard asymmetric LDMOS, we propose a novel dynamic body biased high voltage transmission gate. Prototype simulation using a standard 24V BCDMOS process shows that the proposed circuit draws 2.12μW of power when it senses a voltage that swings between +10V and −10V at 1 kSPS sampling frequency.**

I. Introduction

In a high density electrical stimulator system, such as retinal prosthesis, impedances of electrodes are high. For instance, Pt Black electrodes of diameter $50\mu m$ and $200\mu m$, were measured to be 8720Ω, $22n$F and 3408Ω, $110n$F, respectively [1]. Perceptual current threshold can vary between 24 μA and 702 μA (at $1ms$ pulse), depending on the distance between electrode and retinal surface and the retinal cell condition of the patients [2]. In the example of a 1 ms anodic current stimulation phase, an electrode driving $500\mu A$ across a $8k\Omega$ access resistor towards the $22nF$ double-layer capacitor of the electrode should endure a thumping $(500\mu A \times 1ms)/22nF + 8k\Omega \times 500\mu A = 26.73V$, which justifies the high voltage current drivers in stimulator design [1], [3].

Ray et. al. [4] showed that the impedance can increases in proportion to the logarithmic function of the distance between the electrode and the ganglion cell layer, as the electrode approaches from the fundus entry point to the ganglion cell layer. An important ramifications of the result is that we can infer the quality (proximity) of the contact between the electrode tip and the retinal ganglion cell layer by monitoring the voltage (and the impendence) at the electrode. Furthermore, the electrode voltage sensing can provide essential information about the power supply compliance limit for the adaptive power supply modulation techniques discussed in [3], [5]. For these reasons, we present a high voltage readout circuit which enables a low-voltage Analog-to-Digital Converter (ADC) to be connected to the electrode for low-power voltage sensing.

In the proposed system, the electrode voltage can range from −10V (HVSS) to +10V (HVDD) during the stimulation phase. In contrast, the ADC has to operate in a low voltage power domain between LVDD (+1.8V) and LVSS (0V). Because the input voltage range of the electrode is much wider than that of the ADC, we present a proper voltage scaling ADC interface, which translates the signal from the high voltage domain to the low voltage domain, with low signal distortion and power consumption, using a low-cost BCDMOS process without a symmetric LDMOS device.

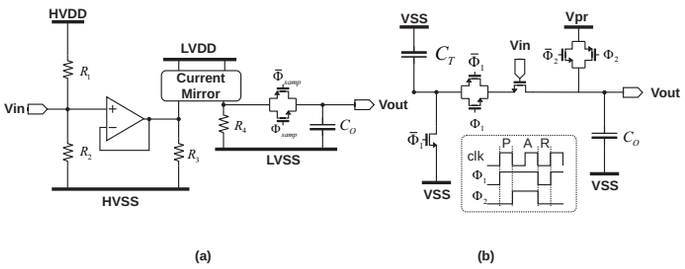

Fig. 1. (a) Conventional resistive divider and V/I converter based voltage scaling interface. (b) Charge transfer amplifier proposed in [6]

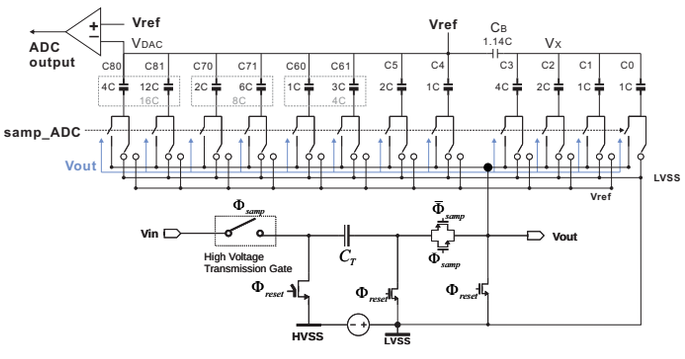

Fig. 2. The Charge Transfer Voltage Scaling ADC Interface Architecture

II. Background and Related Works

The simplest and most frequently used technique for voltage scaling is a resistor divider. In the example depicted in Fig. 1(a), the input voltage (**Vin**) is scaled down on the

resistive divider arm composed of R_1 and R_2 and crosses the voltage domain after being converted into a current through the V/I (Voltage-to-Current) converter composed of an unity follower op-amp and a current mirror. This scheme has 2 major limitations which make it unsuitable for the micro-stimulator application. Firstly, power is continuously dissipated by the constant current flowing through the resistive divider arm even when the voltage sensor is not active. Secondly, a large resistors occupies large silicon area. For instance, in the Global Foundries $0.18\mu m$ process, a $1M\Omega$ requires 17 units of $100\mu m \times 2.1\mu m$ (width $\times$ length) Nwell resistors ($1028\Omega/sq$).

Because the resistive ADC interface is unpractical for the reasons mentioned above, we need to look for an alternative interfacing scheme using capacitive charge redistribution, similar to charge transfer amplifier (CTA) [6] which is shown in Fig. 1(b). The proposed Charge Transfer Voltage Scaling InterFace (CTVSIF) operates on the principle of: (1) Output node voltage is determined by charge redistribution on top plates of the transfer (C_T) and the output capacitors (C_O), responding to the change of the input voltage at the amplification(A) phase (or the sampling phase of the CTVSIF). (2) The amount of the charge to be transferred is determined by the deviation of the input from a reference voltage defined at the preset(P) phase (or the reset phase of the CTVSIF). However, we cannot directly apply the CTA scheme for the stimulator application, because: (1) we are dealing with large input signals with rail-to-rail range, instead of the small input signal of the CTA, and (2) the input and output signals are in different voltage domain. In the CTVSIF, the amount of the charge, accumulated on the coupling capacitor (C_T) is proportional to the input voltage. The charge on C_T is fully transferred onto the output capacitor (C_O), while in the CTA, the amount of charge on C_T transferred to the output is the amount of the charge required to keep the source of the amplifying MOSFET to follow its input gate voltage.

In addition to the advantage of zero-static current, the proposed CTVSIF circuit is made more compact by integrating with the Successive-Approximation-Register (SAR) ADC. It exploits the large capacitor already found in the SAR ADC ($32C_{unit} = 32 \times 30f\text{F} = 960f\text{F}$) and uses this capacitor as the output capacitor of the CTVSIF circuit during the sampling phase; thus, a large saving in circuit area is made. In this work, we attach the CTVSIF with the column parallel SAR ADC described in [7].

III. High Voltage Charge Transfer Voltage Scaling ADC Interface (CTVSIF) Architecture

A. Operating Principle and Control Timing Sequence

Fig. 3 depicts the sequence of the operation of the CTVSIF. All the control signals are synchronized with the clock of the SAR ADC ($\mathbf{clk\_ADC}$). At the 1^{st} rising edge of $\mathbf{clk\_ADC}$, the reset control signal for the SAR ADC, which in turn turns on $\mathbf{rst\_ADC}$ at the 2^{nd} rising edge, is asserted for 1 clock cycle, to initialize the SAR ADC for the subsequent data conversion. At the 2^{nd} rising edge of the **clk_ADC**, the controller shall send a signal to connect the sampling plate

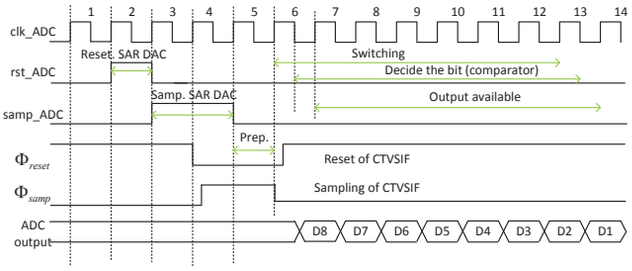

Fig. 3. Timing Diagram of the CTVSIF for SAR ADC

of the SAR DAC with the output of the CTVSIF for at least 2 cycles by asserting $\mathbf{samp\_ADC}$, which would be raised during the 3^{rd} and 4^{th} cycles: (1) During the 2^{nd} cycle, it waits for the next rising edge, completing reset operation triggered by the $\mathbf{rst\_ADC}$. (2) During the 3^{rd} cycle, it initializes the voltage at the bottom plate of the SAR DAC to LVSS. (3) During the 4^{th} cycle, it charges the bottom plate of the SAR DAC to a voltage to be sampled. To put it in terms of Fig. 2, the bottom plates of the SAR DAC (indicated by Vsig) starts to be 'seen' by the output of the CTVSIF from the 3^{rd} to the 5^{th} rising edge of the **clk_ADC**. As a result, CTVSIF clears the charge on the bottom plate of the SAR DAC, during the 3^{rd} cycle, with $\mathbf{\Phi_{reset}}$ to be asserted. When $\mathbf{\Phi_{reset}}$ is asserted, the bottom and top plate of the C_T are stuck to **HVSS** and **LVSS**, respectively, while the **Vout** node is set to **LVSS**. During the 4^{th} cycle, $\mathbf{\Phi_{samp}}$ signal is asserted, thereby turning on the both High Voltage (HV) and Low Voltage (LV) transmission gates, the amount of the charge on the top plate of C_T increases by $\Delta Q = C_T\,(V_{in} - V_{HVSS})$, compared to the 3^{rd} cycle. This amount of charge is directly transferred to the bottom plate of the SAR DAC, setting the voltage to be $V_{out} = \Delta Q/C_{SAR} = (C_T/C_{SAR}) \times (V_{in} - V_{HVSS})$, where C_{SAR} is total capacitance of the SAR DAC. We need to note that two CTVSIF control signals ($\mathbf{\Phi_{reset}}$ and $\mathbf{\Phi_{samp}}$) are non-overlapping mutually exclusive signals synchronized at the rising edge of the clock, because discharging incurred by non-zero $\mathbf{\Phi_{reset}}$ signal can soak the charges to be transferred to the output node, and thereby destroying the signal integrity of **Vout(Vsig)**. For the same reason, we need to extend the $\mathbf{\Phi_{samp}}$ phase by one clock cycle after **samp_ADC** is de-asserted to prevent abrupt signal distortion at the falling edge of $\mathbf{\Phi_{samp}}$ signal. Then, from the 6^{th} to the 13^{th} clock cycle, the SAR ADC results are readout bit-serially on each falling clock edge. The ADC completes its conversion on the rising edge of the 14^{th} clock cycle.

B. High Voltage Transmission Gate using Asymmetric LDMOS

Fig. 4 shows a typical LDMOS (Laterally Diffused Metal-Oxide-Semiconductor) found in standard CMOS processes. The LDMOS is often asymmetric, to reduce its input capacitance (mainly composed of the overlap of the junction

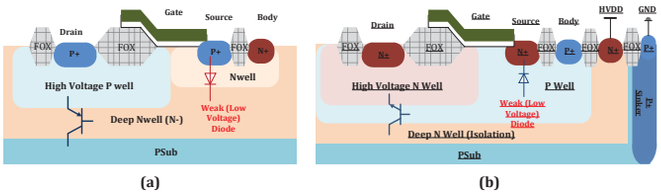

Fig. 4. Cross sections of (a) LDPMOS and (b) Isolated LDNMOS with parasitic BJT and weak diode with low breakdown voltage

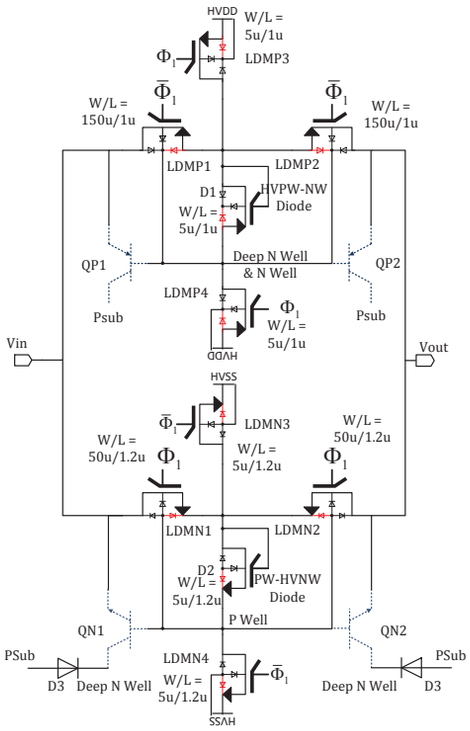

Fig. 5. Circuit schematic of the proposed HV transmission gate using LDMOS. LDMOS transistors are shown with thick gates slanted toward drain side, which is analogous to the cross section diagram (Fig. 4)

and the gate) and the feedback capacitance (mainly composed of gate-drain overlap) as well as to avoid dedicated high voltage process inducing extra cost. This asymmetry presents a big hurdle against using the LDMOS to form a conventional transmission gate, because the weak diode in Fig. 4 between the source and the body is not protected against high voltage. Thus, we developed a HV transmission gate structure, in which only drain terminals are exposed to the **Vin** and **Vout** nodes, hiding the weak diode at the source terminal inside a back-to-back configuration of 2 LDMOS transistors (LDMP1,2 and LDMN1,2), as shown in Fig. 5. Here, we adaptively bias the body of the LDMOS transistors to prevent: (1) parasitic BJTs (QP/N1,2) from being turned on, and (2) the voltage across the weak diodes from exceeding their breakdown voltage. To achieve these goals, the body and the source of the main switches (LDMP/N1,2) are tied up/down to the HVDD/HVSS, when switches are turned off (by de-asserting Φ_{samp}). And, while the switches are turned on (by asserting Φ_{samp}), the bodies of the the main switches (LDMP/N1,2) are set to the voltage levels which are one-diode drop (≈600mV) above(LDPMOS)/below(LDNMOS) the input voltage (**Vin**), through the diode-connected LDMOS (D1,2).

C. Level Shifter

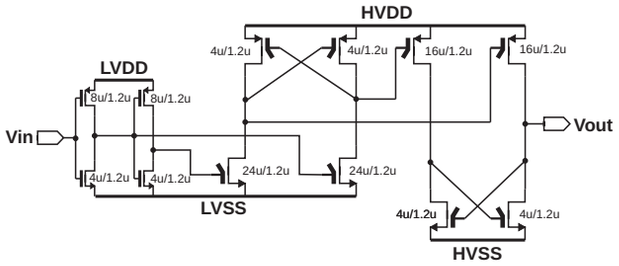

Fig. 6. Circuit schematic of the level shifter

The control signals are generated by digital logic, swinging in the low voltage domain (LVDD-LVSS). The level shifter, shown in Fig. 6 converts the control signals (Φ_{samp} and Φ_{reset} of Fig. 2) from the low voltage domain to high voltage domain in 2 steps. In the first step, a set of the low voltage complementary signal (original and inverted) is applied to the high voltage LDNMOS common source amplifies (CMA), which are coupled with a LDPMOS bi-stable latch, of which source terminals are tied up to the HVDD. As a result of the first stage operation, a set of the complementary outputs swinging between LVSS and HVDD is generated and they drive the LDPMOS CMA in the next stage, with which a latch is coupled. Here, input voltages at the input of the CMAs are not high enough to fully turn on the LD(P/N)MOS due to high threshold voltage (1.3V/1.1V for LD(P/N)MOS in this design), the size of the CMA transistors are relatively big (W/L=24μm/1.2μm for LDNMOS, W/L=16μm/1μm for LDPMOS).

IV. Simulation Result and Discussion

We performed simulations for the proposed circuit using BSIM3v3 models for the Global Foundries 0.18μm process. Fig. 7 shows the Turn-On resistance of the HV transmission gate. The size of the LDPMOS switches are 3 times larger than that of the LDNMOS switches on the conducting path, to compensate for the intrinsic electron-hole mobility disparity. A by-product of applying adaptive body biasing on the LDNMOS-only switches (bottom path of Fig. 5) is that the initial Turn-On resistance at low **Vin** is larger due to the modulated body-bias and input-dependent effective threshold voltage. Fig 8 shows that the relation ship of between V_{in} and V_{out} of the proposed CTVSIF, where HVDD = +10V, HVSS = -10V, LVDD = 1.8V, and LVSS = 0V. In this design, the simulated voltage scaling ratio (0.0914) deviates from the theoretical voltage scaling ratio ($C_T/C_{SARDAC} = 107fF/960fF \approx 0.11$), due to the

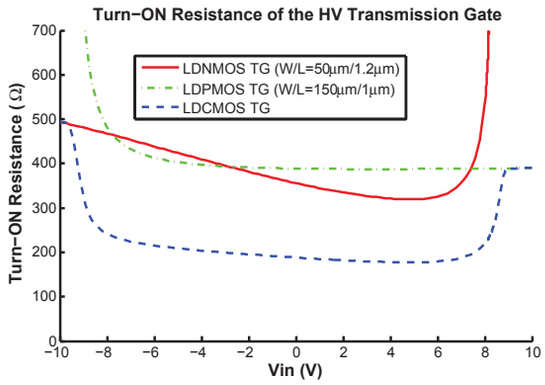

Fig. 7. Simulated Turn-On resistance of the HV transmission gate

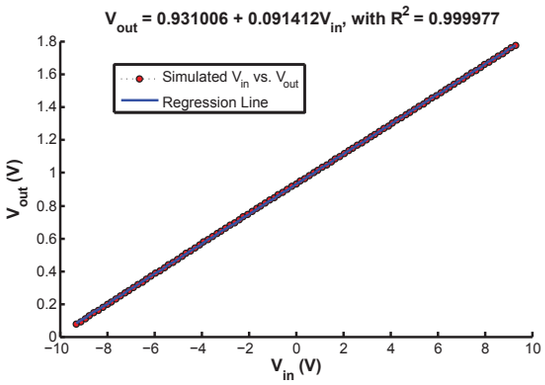

Fig. 8. Simulated Input (V_{in}) vs. Output (V_{out}) and the linear regression line calculated from the sample points generated by the simulation

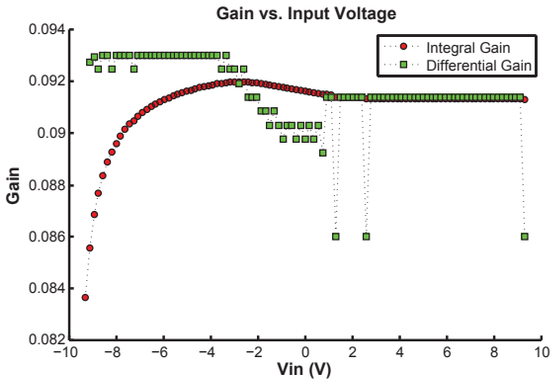

Fig. 9. Integral and differential gain of the CTVSIF

parasitic capacitance associated with switches. However, the linearity is shown to be guaranteed with the coefficient of determination (R^2) = 0.999977. Fig. 9 show the integral and differential gain of CTVSIF. Integral gain ($V_{out}/(V_{in}+10)$) describes how much the actual gain fluctuates from the ideal gain constant. Integral gain droops at the low voltage region is cased by the signal distortion introduced by the larger effective parasitic capacitance dependent on V_{out}. Differential gain ($\partial V_{out}/\partial V_{in}$) tells how steadily the output value increases between 2 closest adjacent steps. Power consumption under some operating conditions are summarized in Table I. The total power consumption is linearly proportional to the sampling frequency. Future efforts on optimizing the CTVSIF should start by using a more power efficient level-shifter with faster transition out of its meta-stable state, because it consumes more than 55% of the total power budget.

TABLE I
POWER CONSUMPTION SUMMARY (HVDD/HVSS = $10V/-10V$, LVDD/LVSS = $1.8V/0V$)

V_{in}	Block	Sampling Rate		
		1 kSPS	10 kSPS	100 kSPS
HVSS+10V	Total Power	$2.12\mu W$	$21.1\mu W$	$211\mu W$
	Level Shifter	$1.17\mu W$	$11.6\mu W$	$116\mu W$
	HV Trans. Gate	$0.57\mu W$	$5.73\mu W$	$57.2\mu W$

V. CONCLUSION

In this paper, a low-power interfacing circuit is proposed for scaling high voltage input signals to a low voltage domain suitable for integration with SAR ADCs. It works by charge transfer and consumes no static current which makes it especially suitable for micro-stimulator applications, where the ADC is activated on-demand. The fact that the micro-stimulator has to support bipolar signal makes the proposed interface more attractive, because it allows the high voltage signal to cross over into the low voltage domain in just one step; furthermore, the ground levels of the high and low voltage domains need not be the same.

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