A Continuous-Time VCO-assisted VCO-based ΣΔ Modulator with 76.6dB SNDR and 10MHz BW

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Abstract—**In this paper, a new VCO-assisted VCO-based sigma-delta (ΣΔ) modulator is proposed to improve the linearity of the VCO-based quantizer. The assistant network in the digital feedforward path reduces the input swing of the VCO-based quantizer in the main path, and then adds it together through the digital cancellation path to keep the same signal before and after quantization. Moreover, the merit of the auxiliary VCO increases the tolerance to DAC mismatches because of its intrinsic DEM function, which also simplifies the digital circuit part. A first order continuous-time (CT) ΣΔ modulator with the proposed structure is designed and simulated in a 65nm CMOS process. The performance of the modulator can reach 76.6dB/82.4dB SNDR/SNR with second order noise shaping and 84dB DR within a 10MHz bandwidth and a sampling frequency of 1.4GHz, consuming 9.4mW of power.**

I. INTRODUCTION

The performance of the continuous-time sigma delta modulator benefits from the implicit antialiasing filter, enjoying wideband capability and relaxed Op-Amp speed requirements, when compared with its discrete-time counterpart [1]. Recently, it has been quite popular in the area of analog to digital conversion. There-into, voltage controlled oscillator (VCO)-based quantizer takes its advantage of explicit first order noise shaping and intrinsic dynamic element matching (DEM) and is very suitable for embedding into the high-speed CT ΣΔ modulator for wideband applications. However, the most important issue that should be addressed carefully is related with the voltage-to-frequency tuning curve of a VCO which is highly non-linear in practice [2]. The impact of such non-linearity introduces harmonic distortion which can significantly degrade the SNDR performance of the quantizer.

Several methods have been explored to reduce the effects of VCO non-linearity. For example in [3], one flash quantizer is used before the VCO-based quantizer, allowing only the residue signal to pass through it, and thereby reducing the input swing and distortion of the VCO-based quantizer. However, the flash quantizer cannot perform the intrinsic DEM thus causing additional digital processing in a practical implementation. In another case from [4], a switched high-linearity VCO-based quantizer has been proposed to keep the intrinsic DEM and saving DAC cells by using two interleaved phases to process the main signal and the residue. But, that will imply the loss of the first order noise shaping in the VCO-based quantizer.

In this paper, a VCO-assisted VCO-based circuit is proposed. This structure can greatly reduce the nonlinearity caused by the VCO-based quantizer while keeping the intrinsic DEM which can simplify the digital implementation. Meanwhile, using a smaller number of bits than in the VCO-based quantizer, as the assistant digital path, the structure can achieve lower power consumption than its flash counterpart, while also maintaining the DEM function in the digital feedforward path.

This paper is organized as follows: Section II presents a brief theoretical review of the properties and nonlinearity problem of the VCO-based quantizer; Section III introduces the proposed VCO-assisted VCO-based structure followed by the description of this novel digital feedforward assistance, besides, circuit design issues will also be addressed; Section IV presents the simulation results, and finally Section V will draw the conclusions.

II. PROPERTIES OF THE VCO-BASED QUANTIZER

Fig. 1(a) shows the internal structure of a VCO-based quantizer with a multi-phase ring oscillator structure [4]. It can achieve voltage-to-frequency conversion with a highly digital implementation. The tuning characteristic of the VCO cell can be described as,

$$\Phi_{VCO}(t) = 2\pi K_v \int V_{Tune}(t)dt \qquad (1)$$

where the phase output of the VCO cell is proportional to the integration of the VCO tuning input, and K_v is the voltage-to-frequency gain which is also the source of nonlinearity as revealed in [2].

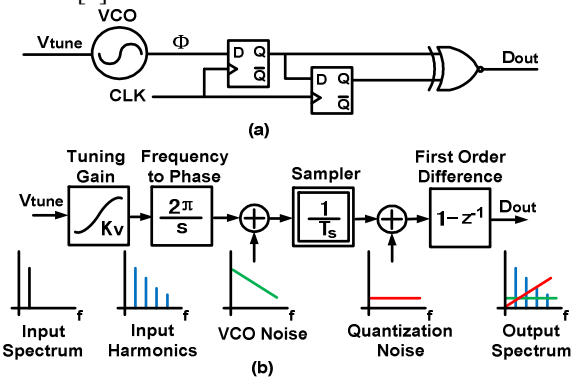

Fig. 1. VCO-based quantizer. (a)Internal structure; (b)Behavior model.

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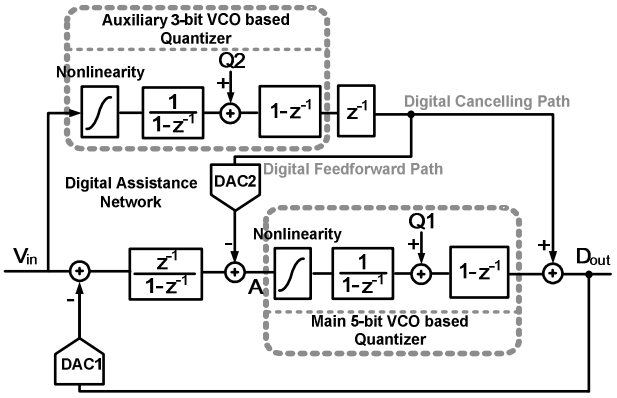

Fig. 2. Proposed 1st order SDM with a VCO-assisted circuit in the DT counterpart.

On the other hand, the D-flip-flops and XOR gate perform as the counter and register, which allows high speed operation with small latency. By using such digital structure, the phase signal is finally converted to frequency signal.

As such, the behavior model of the VCO-based quantizer can be illustrated as in Fig. 1(b) [5]. The digital part operates as a first order difference which realizes the appealing aspect of the first-order noise shaping. Specifically, the key point is related with the fact that the truncation error at the end of each clock period boundary is not lost, but rather it is accounted for in the following measurement in the next clock cycle. Besides, this corresponding $1\text{-}z^{-1}$ function is also an indication of the barrel shifting property in the DAC part, which can randomize the DAC mismatch as intrinsic DEM. The VCO operates as an integrator with a gain of $2\pi K_v$ which introduces harmonic distortion that can significantly degrade the SNDR performance of the quantizer. As the input swing increases, the harmonic distortion will also increase. Therefore, practically, the VCO-based quantizer is not a high performance quantizer due to the serious nonlinearity of the VCO that dramatically affects the performance of the modulator.

III. Proposed 1st Order CT ΣΔ Modulator with VCO-Assisted VCO-Based Quantizer

A. Proposed Structure of the DT Counterpart

To reduce the nonlinearity, a new digital assisted method has been presented to improve the linearity of the VCO-based quantizer. The design of a continuous time ΣΔ modulator is normally done starting from a discrete time prototype. Fig. 2 shows the proposed 1st order DT ΣΔ modulator with the VCO-assisted VCO-based quantizer. One extra digital feedforward path with a 3-bit VCO-based quantizer is added in front of the 5bit VCO-based quantizer, and then cancelled at its end, in this way, the signal at node A now becomes,

$$\text{Signal}_A = -z^{-1}(1 - z^{-1})(Q_1 + Q_2) \quad (2)$$

while in the traditional 1st order VCO-based circuit without digital assistance, the input signal of the quantizer is,

$$\text{Signal}'_A = z^{-1}X - z^{-1}(1 - z^{-1})Q_1 \quad (3)$$

Fig. 3 illustrates the comparison of the quantizer input swing between these two structures, where it can be found that the input swing of the quantizer in the proposed structure (in red) has significantly decreased. This ensures the linearity of a 5 bit VCO-based quantizer in the main path. The signal transfer function (STF) and the noise transfer function (NTF) of the proposed circuit can be calculated as,

$$\text{STF} = z^{-1} \quad (4)$$

$$\text{NTF} = (1 - z^{-1})^2 \quad (5)$$

where it is clearly indicated that there are no changes in the TF from the traditional VCO-based circuit, which also maintains the second order noise shaping function $(1\text{-}z^{-1})^2$.

As the number of bits in the VCO-assisted quantizer directly determines the residue signal processed in the 5 bit quantizer in the main path, to certify that the difference between the signal in the digital feedforward path and the output of the integrator is narrower, for lowering down the swing at Node A, the noise of the assistant VCO-based quantizer should be carefully considered. Fig. 4 illustrates the curve of the Signal-to-Noise- and-Harmonic-Distortion-Ratio (SNDR) varying with the number of bits of the digital assistant quantizer. From this figure, it can be deducted that as the number of bits in the assistant quantizer increases, which means that the input signal swing at node A decreases, the SNDR improves. Furthermore, when the number of bits reaches 8 or is even higher, the Total-Harmonic-Distortion (THD) will no longer dominate the performance, thus promising good linearity.

Different from the previous digital assistant method published in [6], a 3 bit VCO based quantizer is used in the digital assistant circuit rather than a 3 bit flash quantizer. Thus guaranteeing, as well, low power consumption. Furthermore, the mismatch ε_1 of the DAC in the digital feedforward path can be of second order noise shaped: with contributions from the integrator in the main path, and from the 3bit VCO-based quantizer. The signal output of this mismatch ε_1 as the noise

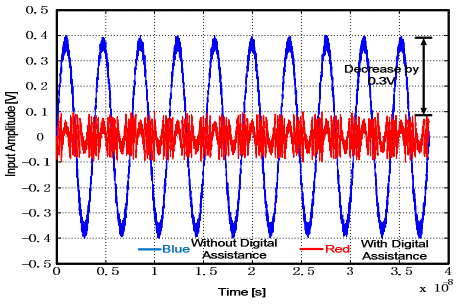

Fig. 3. Comparison of the VCO input swings between the 2 models.

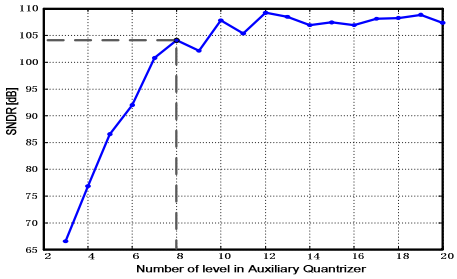

Fig. 4. Selection of the number of levels in the auxiliary VCO-based quantizer..

source is calculated now as,

$$\text{Signal}|_{\varepsilon_1} = -(1-z^{-1})^2\,\varepsilon_1 + (1-z^{-1})^2 Q_1 \qquad (6)$$

which improves the tolerance of the DAC mismatches in a real implementation. Together with the implicit DEM function of the VCO-based quantizers, which also simplifies the digital circuit and saves a considerable amount of power, the DACs mismatch in all feedback paths can also be controlled without too much influence in the performance.

Although the nonlinearity of the assistant VCO itself affects the DAC output in the digital feedforward path this non-ideality will eventually be cancelled after the digital adding path because the input swing of the 5 bit VCO based quantizer is reasonably low, and, as such, it will not contribute significantly with nonlinearity. Thus certifying that the signals (not including noise) before and after this quantizer are basically kept as the same. A Matlab simulation was performed in 2 cases with the corresponding power spectrum results shown in Fig. 5. The blue curve corresponds to the result of a typical first order ΣΔ modulator without the digital assisted network, on the other hand, the red curve represents the SNDR with a 3 bit auxiliary VCO-based quantizer as the assisted quantizer. As shown, the proposed structure not only decreases the total harmonic distortion, but also keeps an evident second order noise shaping function.

B. CT Circuit Realization

The overall circuit of the continuous-time (CT) 1st order ΣΔ modulator with VCO-assisted VCO-based quantizer is represented in Fig. 6, for a 10MHz bandwidth. The standard active RC integrator is used for simplicity and high linearity. The optional amplifier is designed with a two-stage telescopic structure in the 1st stage and a common-source in the 2nd stage, for larger dynamic range. The estimated power consumption is 8.2mW for a 60dB Gain and 2.6GHz Gain-Bandwidth (GBW).

The digital feedforward path is added to the main path by using a passive adder. This passive adder is implemented with a pair of resistors to perform the subtraction, which not only simplifies the circuit but also decreases considerably the power

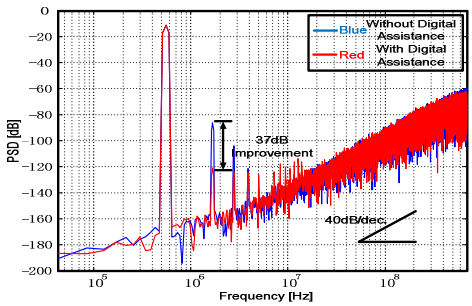

Fig.5. Improvement in SNDR using 3bit auxiliary VCO-based quantizer.

consumption. Besides, the passive attenuator that is composed by the ratio of two resistors in front of the digital feedforward network, is designed to counteract the gain of the 3bit VCO based quantizer. Then, it ensures the performance of the digital feedforward path within a high input range. Plus, the digital summing node in Fig 6 has been divided into two nodes now, being one in front of the integrator by using the additional DAC3 feedback, and the other at the end of the digital part. In this way, the implicit DEM characteristics in all the DACs including DAC1 and DAC3 will be retained.

The excess loop delay compensation is designed by using extra DAC feedback and one unit cycle delay. The unit cycle delay is achieved by D-flip-flops in the digital part of the VCO-based quantizer, these D-flip-flops make the outputs in both VCOs sampled at the same time, which also ensures the less mismatch at the point of passive adder. Benefiting from the passive adder, this delay compensation feedback can be added in front of the quantizer, now without any additional active adder. The non-return-to-zero (NRZ) DAC with current steering feedback is adopted in each DAC feedback for high speed transition and less sensitivity to the clock-jitter. Both VCO-based quantizers are sampled at 1.4GHz, with a tuning-voltage-to-frequency characteristic similar, in order that the sampling frequencies are the same in the two quantizers, The 3-bit VCO is designed based on 31 level delay units that are the same as in the 5-bit VCO, the main difference is related with the fact that we only choose 7 delay units outputs in average

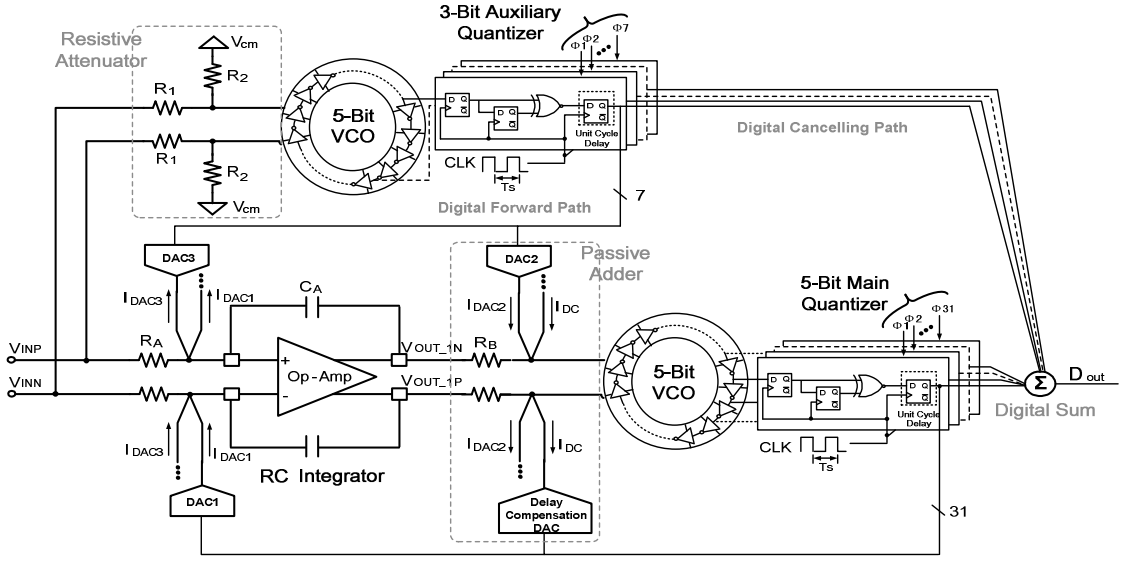

Fig. 6. Circuit implementation of the 1st order CT VCO-assisted VCO-based sigma-delta modulator.

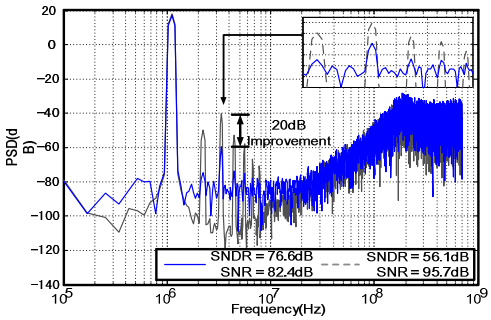

Fig. 7. Proposed CT circuit SNDR in 10MHz BW.

(each for every 4 delay cells), as mentioned in [4], to perform the quantization.

IV. Simulation Results

The proposed 1st order CT ΣΔ modulator with VCO-assisted VCO-based quantizer is implemented in a 65nm CMOS technology. The assistant VCO path is verified with a 3-bit quantizer and the VCO-based quantizer in the main path is built with 5-bit. Both of the quantizers are sampled at 1.4GHz frequency. The bandwidth of the input signal is 10MHz, and the oversampling ratio is set as 70. The simulated power spectral densities (PSD) of this ΣΔ modulator are depicted in Fig. 7, and shown in blue. The SNR can reach 82.4dB and the SNDR is equal to 76.6dB.

For comparison, a similar circuit without VCO assistance path has been also designed with the PSD result shown in gray, also in Fig.7. The SNR and SNDR is 95.7dB/56.1dB, respectively. It can be clearly deducted that the THD decreases significantly and the 3rd harmonic has decreased by 20dB with the utilization of the VCO assistance technique. This means that the linearity of the proposed modulator experiences a great improvement while keeping the second order noise shaping inherent to the behavior of the VCO. The only drawback is the noise floor that has increased by a value close to 15dB as a trade-off due to the mismatch among K_v, the gain of the resistive attenuator and the passive adder, which lead to the impossibility of cancelling the entire auxiliary VCO noise. But, that can be considered acceptable since the nonlinearity of the VCO dominates most of the overall circuit performance.

The nominal voltage supply is 1V and the total power consumption of the proposed structure is 9.4mW, where the 3-bit VCO assistant network drawing only a mere 0.3mW.

TABLE I. COMPARISON OF THE PERFORMANCE OF DIFFERENT MODULATORS

Specification	[2]	[3]	[4]	This work
Technology	0.13µm	90nm	65nm	65nm
Sampling Frequency(MHz)	900	600	575	1400
Bandwidth(MHz)	20	10	10	10
Peak SNDR(dB)	78	78	67	76.6
Power(mW)	87	16	7	9.4
FoM(fJ/conv.)	323	123	192	85

Fig. 8 shows the dynamic range of the VCO-assisted VCO-based circuit, achieving 84dB. The comparison of the proposed structure with VCO-assisted circuit with recently published circuits based on VCOs is listed in Table I, where is clearly seen the high-performance of the proposed circuit. The Figure of Merit (FoM) is calculated by Power/(2·Bandwidth·2^{ENOB}).

V. Conclusions

A novel CT VCO-assisted VCO-based ΣΔ modulator has been presented to improve the linearity of the VCO based quantizer. One digital feedforward path using a 3-bit VCO based quantizer has been introduced, first to reduce the input swing of the 5-bit VCO based quantizer by using the passive adder in the main path and then be added in the digital part, in order to keep the STF and NTF in the loop system. Meanwhile this structure maximizes the application of the intrinsic DEM function in the digital feedforward path and the feedback path simultaneously, which leads to the circuit simplification and power saving. The circuit has been implemented in 65nm CMOS, and it can achieve a SNR/SNDR in the order of 82.4dB/76.6dB, with 10MHz bandwidth, at a sampling frequency of 1.4GHz, under only one RC integrator as the loop filter, with a simple operational amplifier of relative low gain. Finally, a benchmark with similar state-of-the-art architectures compares favorably with the best FoM among all of them, with a value of 85fJ/conv.

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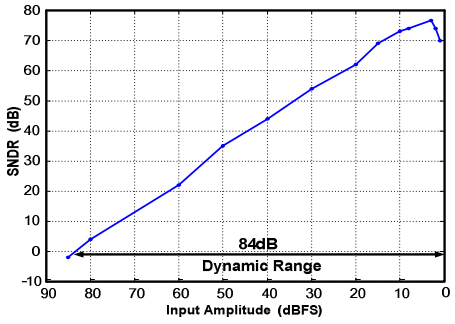

Fig. 8. Dynamic range of the CT VCO-assisted VCO-based circuit.