A Curvature Compensated BJT-based Time-Domain Temperature Sensor With An Inaccuracy of ±0.7°C From -40°C to 125°C

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***Abstract*—This paper presents a BJT-based time-domain temperature sensor with V_{BE}-curvature compensation. The temperature dependent signals from the BJT frontend are processed by the delay pulse generator to produce a temperature dependent pulse width modulation (PWM) signal for low power consumption. To further improve the sensing accuracy, the PWM signal is quantized using an on-chip current-controlled oscillator (CCO) to compensate for the intrinsic V_{BE} non-linearity. Implemented in a standard 0.18-µm CMOS process, the proposed sensor achieves an inaccuracy of ±0.7°C using only one-point calibration at 30°C, while consuming a nominal power of 5.7µW over a wide range from -40°C to 125°C.**

Keywords—CMOS temperature sensor, Time domain, Low-power, Curvature compensation

I. Introduction

CMOS temperature sensors, which feature easy circuit-level interfacing and system integration, have always been playing an important role in many emerging wireless sensing applications. They are mainly classified into three categories depending on their readout topologies: 1) voltage domain; 2) frequency domain; and 3) time domain. Most voltage-type CMOS temperature sensors are based on incremental ADCs which can suffer from high power consumption and design complexity [1]. Due to the emerging low-cost and high-performance sensing applications for biomedical and logistic uses powered by energy harvesting sources, time-/frequency-based implementations become attractive due to their simplicity and low power characteristics.

When compared with frequency-domain temperature sensors which usually exhibit small chip area and high conversion rate [2], the time-domain implementations can typically achieve relatively higher accuracy and larger sensing range [3-5]. They typically employ inverters [3] or resistors [4] to generate a PWM signal for temperature sensing. However, both inverters and resistors suffer from high non-linearity, ultimately limiting their sensing accuracy without elaborate calibration efforts. A BJT can also be utilized with low power consumption but can suffer from high inaccuracy due to the intrinsic device non-linearity, leading to a limited sensing range from 0°C to 80°C as in [5].

Typically, one of the major sources of non-linearity for a BJT is the curvature in V_{BE}. To resolve this problem, this work proposes a curvature compensated BJT-based time-domain temperature sensor. Instead of using an ideal clock for PWM signal quantization as in existing works, we propose to compensate for the V_{BE} non-linearity by using a process tracking current controlled oscillator (CCO). Implemented in a standard 0.18-µm CMOS process, this work achieves a wide temperature range from -40°C to 125°C with an inaccuracy of ±0.7°C after 1-point calibration, while consuming a nominal power consumption of only 5.7µW. Section II describes the system overview and the CMOS implementation of the proposed sensor. Section III presents the simulation results. Finally, Section IV draws the conclusions.

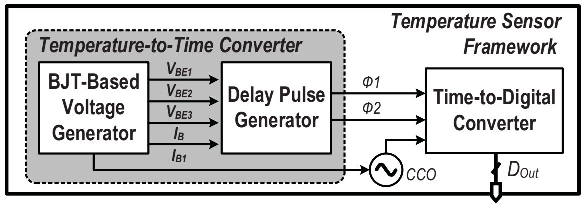

Fig. 1. Block diagram of the proposed temperature sensor.

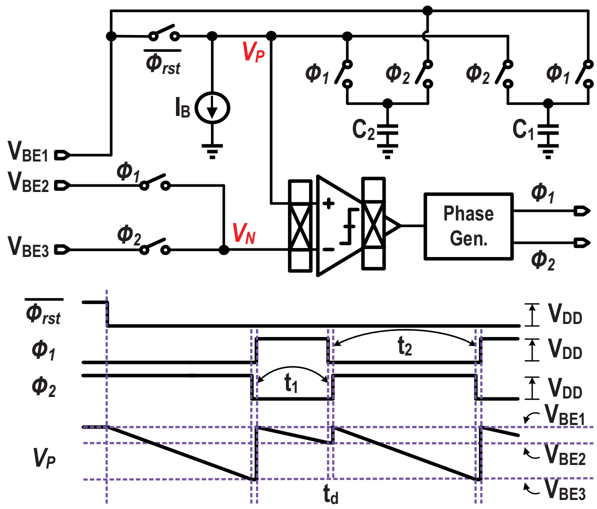

Fig. 2. Architecture of the delay pulse generator.

II. Circuit Architecture

A. System Overview

Fig. 1 shows the block diagram of the proposed temperature sensor, comprising a BJT-based frontend, a delay pulse generator, a CCO and a time-to-digital converter. The BJT frontend utilizes the base-emitter voltages (V_{BE}) of substrate PNPs to generate a complementary-to-absolute-temperature (CTAT) voltage. Instead of using power hungry incremental ADCs, the delay-pulse generator produces a temperature dependent PWM signal by discharging the capacitors while preserving the linearity. To compensate for the V_{BE} curvature for improved sensing accuracy, a current-controlled oscillator driven by a V_{BE}-dependent current source is also proposed to quantize the PWM signal while ensuring process tracking. The details of the circuit-level implementations are described next.

B. Delay Pulse Generator

The delay pulse generator mainly consists of a chopped comparator, two capacitors ($C_{1,2}$), and a complementary-to-

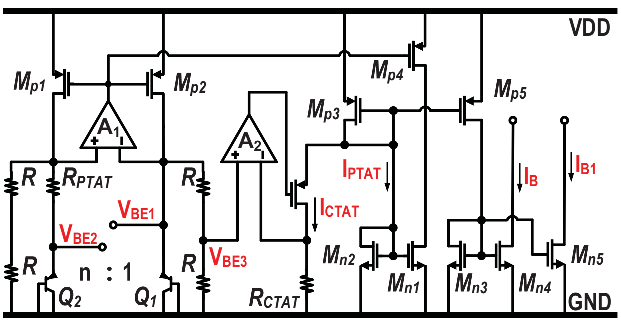

Fig. 3. Schematic of the BJT-based frontend generator.

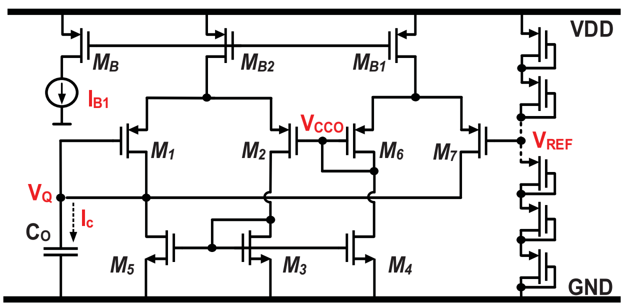

Fig. 4. Schematic of the current-controlled oscillator.

absolute-temperature (CTAT) bias current (I_B). Both $C_{1,2}$ are charged and discharged alternatively by controlling the switches as shown in Fig. 2. At the start of a temperature measurement, $C_{1,2}$ are both initialized to V_{BE1}. During Φ_1, the positive input node of the comparator V_P is connected to C_2, while V_N is shorted to V_{BE2}. C_2 is then discharged by I_B until V_P reaches V_{BE2} with a discharging time t_1. During Φ_2, C_2 is refreshed to V_{BE1} while C_1 is now connected to V_P. With C_1 discharged by I_B to V_N at V_{BE3} (which is set to $V_{BE1}/2$ by the frontend in Fig. 3), we can obtain another discharging time t_2. The discharging times t_1 and t_2 can be expressed as,

$$t_1 = \frac{C_2(V_{BE1}-V_{BE2})}{I_B} = \frac{C_2 \Delta V_{BE}}{I_B}, \tag{1}$$

$$t_2 = \frac{C_1(V_{BE1}-V_{BE3})}{I_B} = \frac{C_1 V_{BE1}}{2I_B}. \tag{2}$$

which are directly proportional to ΔV_{BE} and V_{BE}, respectively. For clarity, we define the parameter m=$2C_2/C_1$. With m set to compensate for the temperature coefficient (TC) between ΔV_{BE} and V_{BE1} to obtain a voltage reference V_{BG}, the corresponding PWM signal and duty cycle are,

$$t_{PWM} = t_1 + t_2 = \frac{m\Delta V_{BE}+V_{BE1}}{2C_1 I_B} = \frac{V_{BG}}{2C_1 I_B}, \tag{3}$$

$$D(T) = \frac{t_1}{t_{PWM}} = \frac{kT}{q}\frac{m \cdot In(n)}{V_{BG}}, \tag{4}$$

where k is the Boltzmann's constant, q is the elementary electric charge, and T is the absolute temperature. As observed in (4), $D(T)$ is proportional-to-absolute-temperature (PTAT) and can be utilized for temperature measurement. Also, as V_{BG} exhibits the V_{BE} curvature, the sensing inaccuracy is increased when quantizing $D(T)$ with an ideal clock. Consequently, we propose the use of an on-chip CCO for sensing accuracy improvement. Moreover, the simulated delay timing error t_d in Fig. 2 only contributes to negligible sensing error and can be ignored.

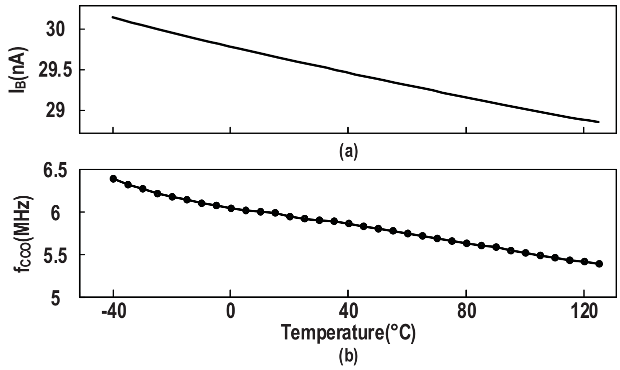

Fig. 5. Simulation results of (a) I_B vs. temperature; and (b) f_{CCO} vs. temperature.

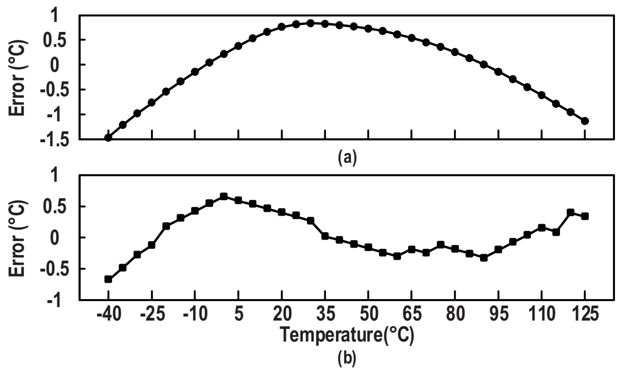

Fig. 6. Simulated error using (a) an ideal clock; and (b) f_{CCO}.

C. BJT-based Frontend Generator

Typically, a time domain CMOS temperature sensor employs resistors or inverter chains for temperature sensing [3-5], which can result in more calibration efforts to preserve the sensing accuracy. In this work, we adopted diode-connected substrate PNP BJTs for its high accuracy. Fig.3 shows the corresponding low voltage BJT-based frontend. The amplifiers A_1 *and* A_2 serve as voltage clamps for generating I_{PTAT} and I_{CTAT} through ΔV_{BE} across R_{PTAT} and V_{BE3} across R_{CTAT}, respectively. Both I_{PTAT} and I_{CTAT} are combined to generate I_B which is slightly CTAT in Fig. 2. This exploits small temperature dependency for V_{BE} curvature temperature compensation through the on-chip CCO as described next.

D. Current-Controlled Oscillator

To achieve system-level co-optimization, we propose to quantize the temperature dependent PWM signal with the CCO for sensing accuracy improvement. Fig. 4 exhibits the circuit implementation [6] with parameter optimization for effective temperature compensation. The core of the CCO is a high gain differential comparator. The positive feedback ensures a well-defined hysteresis between V_Q and V_{CCO} to periodically charge/discharge C_0 with an oscillation frequency f_{CCO}. When V_Q tends to rise above V_{REF}, M_2 conducts and feeds current into the current mirror ($M_{3\text{-}5}$) which discharges C_0. The current I_c pulls V_Q down to V_{QL}, turning on M_1 to charge C_0, sustaining the oscillation in V_{CCO}. In this work, the differential input pair $M_{1,2}$ and output pair $M_{6,7}$ are biased by I_{B1}, which is a scaled version of I_B through the current mirrors $M_{B,B1,B2}$. Assuming negligible switching delays, the CCO oscillation frequency is,

$$f_{CCO} = \frac{I_{B1}}{r(C_0\lambda^{-1})} \propto I_B, \tag{5}$$

TABLE I. PERFORMANCE SUMMARY AND COMPARISON

Parameter	**This work***	[7]	[8]	[9]	[10]
Tech. (μm)	**0.18**	0.13	0.18	0.18	0.18
Sens. Type	**BJT**	BJT	MOS	MOS	MOS
Topology	**Time**	Time	Time	Time	Time
Cal. Point	**1**	1	1	2	1
Range (ºC)	**-40~125**	-20~100	0~100	-20~120	-40~120
Supply (V)	**1**	1.05~1.4	1.8	1.8	1.8
Conv. Rate (sample/s)	**8k**	75k	N/A	1k	486k
Error (ºC)#	**±0.7**	-1.7/ +1.26	±1	-2/+2	-0.85/ +0.78
Power (μW)	**2.6~11.4**	744	N/A	93.6	260
Energy (nJ/sample)	**0.325~ 1.425**	9.92	N/A	93.6	0.535

* Simulation result # Min-Max error

where λ is the channel length modulation coefficient of M_4 and r is a constant controlled by the sizing of $M_{1\text{-}5}$. As f_{CCO} is proportional to I_{B1}, it is therefore also proportional to I_B. Since the curvature of V_{BE} results in the non-linearities of V_{BG} in (4) and the bias current I_B also suffers from the same V_{BE} curvature, we can compensate for the V_{BE}-induced non-linearity at the digital output D_{OUT} by quantizing $D(T)$ with f_{CCO}. By using (4), the curvatures in D_{OUT} due to the non-linearities in both V_{BG} and I_B will become,

$$D_{OUT}(T) = D(T) \times f_{CCO} \propto \frac{I_B}{V_{BG}} = \frac{\frac{V_{BE1}}{2R_{CTAT}} + \frac{\Delta V_{BE}}{R_{PTAT}}}{V_{BE1} + m\Delta V_{BE}}. \quad (6)$$

For simplicity, we denote the rightmost part in (6) as $D_{OUT\_curv}(T)$. For effective curvature compensation,

$$\frac{\partial^2\left(D_{OUT\_curv}(T)\right)}{\partial(T)^2} = 0. \quad (7)$$

This results in the following optimization parameter,

$$2R_{CTAT} = mR_{PTAT}, \quad (8)$$

which can be accomplished in the design stage. Both R_{CTAT} and R_{PTAT} should be implemented using the same type of resistor so they can exhibit the same temperature characteristics for effective compensation. In this work, m is chosen to be 8, and the ratio of R_{PTAT} and R_{CTAT} is determined by (8), resulting in a slight CTAT characteristic in I_B.

III. SIMULATION RESULTS

We implemented the proposed temperature sensor in a standard 0.18-μm CMOS process, with a 1V supply and a conversion time of 125μs. The simulated power consumption varies from 2.6 to 11.4μW with the temperature changing from -40°C to 125ºC (nominal at 5.7μW). Fig. 5(a) displays the measured bias current I_B versus temperature, which exhibits a slight CTAT characteristic varying from 31nA to 29 nA between -40°C and 125°C. Fig. 5(b) plots the simulated f_{CCO} as temperature changes. It can be observed that f_{CCO} also exhibits a similar trend as I_B. Fig. 6 shows the simulation results when $D(T)$ is quantized with both an ideal clock and f_{CCO}. It can be observed that the sensing error can be effectively reduced from -1.5/+1°C to -0.7/+0.7°C between -40°C and 125°C after one-point calibration, demonstrating the effectiveness of the proposed compensation method. Table I summarizes the performance of the proposed circuit and compares it with the state-of-the-art. The comparison with the other time-domain sensors reveals that this work achieves low voltage operation with low power consumption while maintaining a high sensing accuracy over a wide temperature range.

IV. CONCLUSIONS

This paper introduced a curvature compensated BJT-based time-domain CMOS temperature sensor circuit using the on-chip CCO. Implemented using a standard 0.18-μm CMOS process the proposed sensor reaches a wide operating range from -40°C to 125°C with an inaccuracy of -0.7°C/+0.7°C. The low power consumption and high accuracy make it suitable for many low-cost/low-power sensing tasks including environment monitoring, as well as biomedical and life science applications.

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