NEW IMPULSE SAMPLED IIR SWITCHED-CAPACITOR INTERPOLATORS

U Seng Pan [1], R.P.Martins [1'], J.E.Franca [2]

1 - University of Macau
Faculty of Science and Technology
P.O.Box 3001, Macau,
Phone - 853-3974363; Fax - 853-831694; E-mail - fstrpm@umac.mo
(1' - on leave from IST/Portugal)

2 - Instituto Superior Técnico
Department of Electrical Engineering and Computers
Integrated Circuits and Systems Group
Av. Rovisco Pais, 1, 1096 Lisboa Codex, Portugal
Phone / Fax - 351-1-8417675; E-mail - franca@ecsm4.ist.utl.pt

Abstract

This paper presents new Switched-Capacitor (SC) Infinite Impulse Response (IIR) Interpolators employing an efficient combination of Active-Delayed Blocks (ADB) polyphase structures and recursive direct-form II structures with frequency responses no longer affected by the input sample-and-hold filtering effect. Two different architectures are analysed: the first requires slower Operational Amplifiers (OA's) while the second allows the reduction of the number of clock phases and ADB's (1 OA per ADB). Examples are given to illustrate the behaviour of both types of SC interpolators with arbitrary input signal formats.

1. INTRODUCTION

Switched-Capacitor Interpolators are widely utilised not only for relaxing the selectivity requirement of continuous-time post-filtering in sampled-data analogue filtering and digital-to-analogue interface systems but also for realising a variety of complex signal processing functions [1-7], where they are employed to increase the sampling rate from f_s to Lf_s, with the corresponding rejection of the unwanted frequency-translated image components associated with the signals sampled at lower rate. Specialised multirate FIR SC interpolators that could take advantage of the sampling rate increase inherent to interpolation process were also developed for some practical applications [1,5]. For high selectivity and wide stopband approximations of interpolation filtering, optimum IIR SC interpolators based on recursive 1st and 2nd order SC sections combined with Direct-Form (DF) non-recursive polyphase structures have been previously introduced [2,3]. Such interpolators, however, require the modification of the original digital interpolating transfer function due to the input sample-and-hold (S/H) effect at the lower sampling rate[1], thus yielding increased distortion in the frequency response of interpolators besides demanding a more complex design procedure and circuit architecture. This limitation has been overcome in the new SC FIR interpolators by using the original prototype digital interpolating transfer function to operate exactly in the same way as in their digital counterparts [8]. Due to the inherent impulse sampled operation at the input, their amplitude responses are no longer affected by the S/H shaping at the input lower sampling rate. In this paper, a more general, systematic approach based on an efficient, amplifier-shared combination of non-recursive ADB polyphase structures and recursive direct-form II structures is proposed for realising impulse sampled SC IIR interpolators. Two circuit architectures are presented for the same low pass interpolator, one requiring a larger settling time of all OA's and the other needing less clock phases and ADB's (or OA's). Both were simulated with arbitrary input signal formats to verify the correctness of the proposed design.

2. ARCHITECTURE I - OPTIMUM SPEED REQUIREMENTS OF AMPLIFIERS

For simplicity, we consider an example of a 3rd order lowpass IIR interpolator with an interpolating factor $L=3$, output sampling rate $3f_s$= 9MHz, and the original prototype transfer function given by

$$H(z) = 0.02008 \cdot \frac{(1+2z^{-1}+z^{-2})\cdot(1+z^{-1})}{(1-1.601z^{-1}+0.7752z^{-2})\cdot(1-1.3072z^{-1})}$$
$$= 0.02008 \cdot \frac{1+3z^{-1}+3z^{-2}+z^{-3}}{1-2.9082z^{-1}+2.868z^{-2}-1.0134z^{-3}} \quad (1)$$

where the unit delay period is $1/3f_s$. After applying the multirate transformation [2,3,7,9] we obtain

$$H'(z) = \frac{(A_0+A_1z^{-1}+A_2z^{-2})+(A_3+A_4z^{-1}+A_5z^{-2})\cdot(z^{-3})^1+(A_6+A_7z^{-1}+A_8z^{-2})\cdot(z^{-3})^2+(A_9+A_{10}z^{-1}+A_{11}z^{-2})\cdot(z^{-3})^3}{1-B_1(z^{-3})^1-B_2(z^{-3})^2-B_3(z^{-3})^3}$$
$$= \frac{0.0201+0.1186z^{-1}+0.3476z^{-2}+0.6587z^{-3}+0.8813z^{-4}+0.8688z^{-5}+0.6404z^{-6}+0.3429z^{-7}+0.1202z^{-8}+0.0206z^{-9}}{1-2.6139z^{-3}+1.3149z^{-6}-1.0407z^{-9}} \quad (2)$$

Based on expression (2), the respective block diagram can be derived, as presented in Fig.1. It shows that the non-recursive ADB polyphase structures constructed by combining the direct-form parallel processing polyphase structures together with a serial processing delay line [10] implements the numerator polynomial function while the recursive direct-form II structure implements the denominator polynomial function, and both efficiently share the ADB's which produce the delay term z^{-3}. The corresponding SC circuit with an Optimum Coefficients structure, analysed next, is then implemented in Fig.2 with the respective clock phases. There, the upper 3 OA's with input Toggle-Switch-Inverter (TSI) and feedback/reset SC branches constitute 3 cascaded ADB's that produce the delay terms $z^{-5/2}$, $z^{-11/2}$ and $z^{-17/2}$, while the bottom part of the circuit is composed by 3 DF polyphase filters. These are formed by SC accumulators with input SC branches in which the capacitance values correspond to the modified-and-scaled impulse response coefficients, for realising the non-recursive delays which include the complementary delay $z^{-1/2}$. The recursive networks not only feedback to the input of the ADB1 but also contribute to the non-recursive SC branches A_0, A_1 and A_2, since the input and recursive signals add together as illustrated in Fig.1. In order to take advantage of the output SC accumulators and also the adder in the ADB, an Optimum Coefficients structure is proposed based on two sets of the same recursive networks, one that feedbacks to the input of ADB1 and the other that feedforwards to the output SC accumulator, respectively. In the first set, the positive recursive branch B_1 from the output of ADB1 to the virtual ground of OA-Ad1 and the feedback/reset branch of OA-Ad1 can be simplified to only one feedback branch with coefficient $-1+B_1$ (=1.62), while only 2 recursive branches B_2 and B_3 are needed as shown in Fig.2. In the second set, that feedforwards to the output SC accumulator, for simplicity, we consider first the case of polyphase filter $l=0$. There, the additional passive SC branches for realising coefficients $B_1 \times A_0$, $B_2 \times A_0$ and $B_3 \times A_0$ must be included in this polyphase filter in order that its accumulator could be shared. Besides, since the $B_1 \times A_0$ and A_3 branches (or $B_2 \times A_0$ and A_6 or even $B_3 \times A_0$ and A_9) are both connected between ADB1 (or ADB2 or even ADB3) output and virtual ground of OA-Ac0 in accumulator, they can be simplified to a single branch with coefficient $A'_3 = B_1 \times A_0 + A_3$ (or $A'_6 = B_2 \times A_0 + A_6$ or even $A'_9 = B_3 \times A_0 + A_9$). Similarly, the coefficients A_4 and A_7 in polyphase filter $l=1$ and A_5 and A_8 in polyphase filter $l=2$ can also be modified to $A'_4 = B_1 \times A_1 + A_4$, $A'_7 = B_2 \times A_1 + A_7$, $A'_5 = B_1 \times A_2 + A_5$

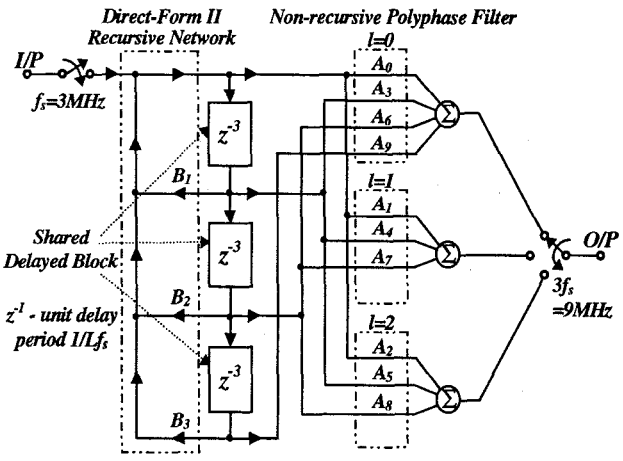

Fig.1 Recursive ADB Polyphase Structure for 3rd Order IIR Lowpass Interpolation

& $A'_8 = B_2 \times A_2 + A_8$ respectively. Two additional branches $A'_{10} = B_2 \times A_1$ and $A'_{11} = B_3 \times A_2$, are also necessary due to the recursive structure (even with $A_{10} = A_{11} = 0$). The final Optimum Coefficients are listed next:

A'_3	A'_4	A'_5	A'_6	A'_7	A'_8	A'_9	A'_{10}	A'_{11}
0.711	*1.191*	*1.777*	*0.614*	*0.187*	*-0.337*	*0.042*	*0.123*	*0.362*

In the previous SC interpolator circuit, L output individual SC accumulators are used (one for each polyphase filter) instead of one, as in the DF polyphase interpolator[1,8]. Therefore, the clock phases can be simplified in order to have a maximum pulse width $\geq 5/6f_s$ as in phase 4, so that the settling of OA's can be close to $5/6f_s$ whereas it is less than $1/6f_s$ in the former structure [1,8]. thus relaxing the settling time requirements of OA's both in the ADB's and accumulators. Since the output of the OA-Ac0 in the accumulator of polyphase filter 0 is sampled in phase 0 with pulse width $1/3f_s$, the settling of Ac0 is about $1/3f_s$ only. The output of the OA-Ac1 is sampled in phase 1 which has the same width of phase 0, but the settling of Ac1 is about $2/3f_s$ because phase 1 has an additional delay $1/3f_s$ of phase 4 whereas there is no delay between phase 0 and phase 4. Based on this analogy, the settling of OA-Ac2 is about $5/6f_s$. Another circuit enhancement for relaxing the settling requirements of all OA's in the accumulators is also proposed. If the circuit block marked with a dotted line (using a unity-gain buffer) is employed instead of one output switch of phase 0(1 or 2) in polyphase filter 0(1 or 2) as shown in Fig.2, the output of the OA's in accumulators are not sampled in phase 0, 1 and 2 directly, but they are sampled to charge the capacitors in phase 3 of the next period. Then, the output will be taken after the unity-gain buffers in phase 0, 1 and 2 in the next period, causing only a linear phase delay in the overall response and relaxing the settling time of all OA's to $5/6f_s$.

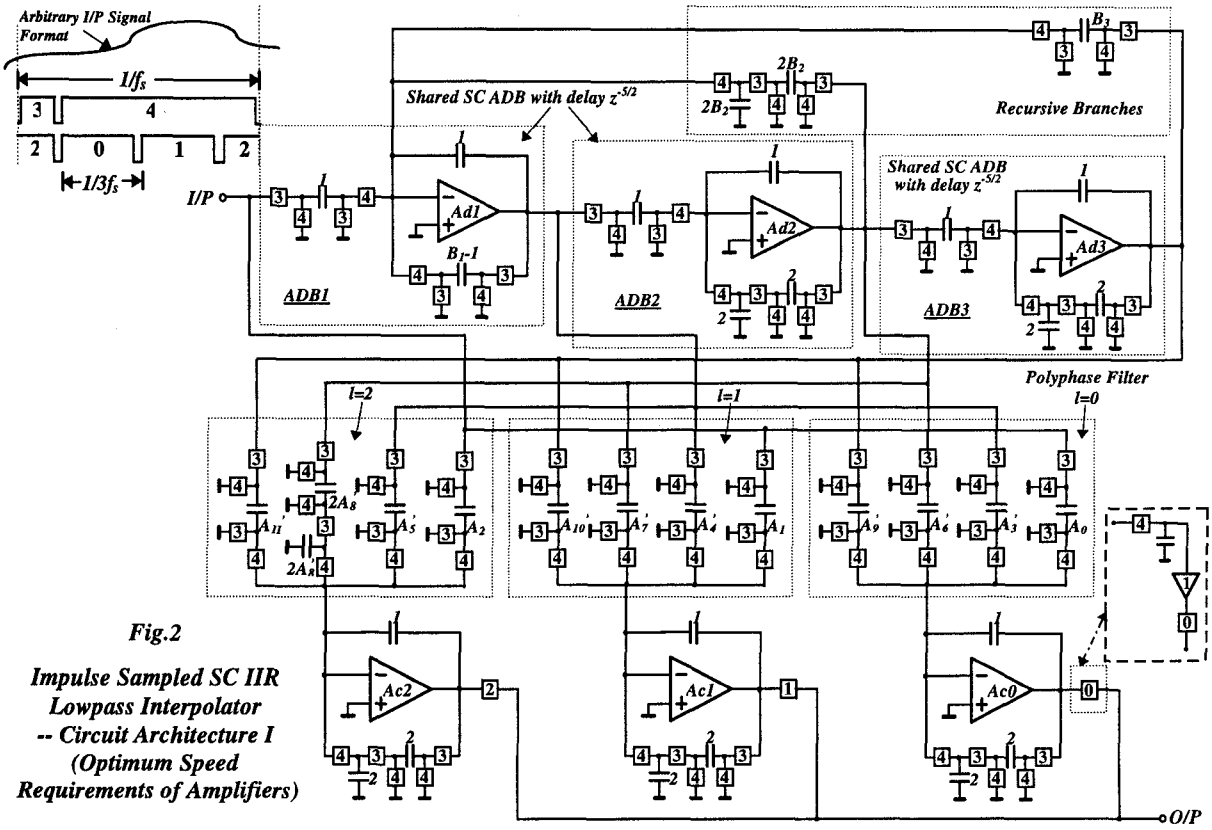

Fig.2

Impulse Sampled SC IIR Lowpass Interpolator -- Circuit Architecture I (Optimum Speed Requirements of Amplifiers)

3. ARCHITECTURE II - MINIMUM NUMBER OF CLOCK PHASES AND ADB'S

A second SC architecture for the implementation of the general block diagram of Fig.1 is depicted in Fig.3 with the respective clock phases. There, only 3 clock phases (equal to the interpolation factor L) are needed. Another significant advantage is the need of only two ADB's, due to an efficient arrangement of clock phases in all SC branches from ADB's, non-recursive polyphase filters and also from the recursive feedback network. This is possible, because the delay implemented by the input polyphase SC branches is no longer determined by the charge transfer slots but is referred to the output sampling slots of each accumulator. As shown in Fig.3, each ADB has the input positive PCTSC branch [11] for producing the z^{-3} delay, and the two cascaded ADB's provide the delay terms z^{-3} and z^{-8}, thus eliminating ADB3. It can be also concluded that for very high filter orders and larger interpolating factors, the number of ADB's saved is even higher. In the previous scheme, a Nth order interpolator needs N ADB's, while with this architecture it needs K ADB's where K is the minimum integer equal to or greater than $(NL+1)/(2L-1)$. However, the settling time of all OA's (around $1/3f_s$ in this implementation) needs to be smaller than before.

4. COMPUTER SIMULATED RESULTS

The behaviour of the SC lowpass IIR interpolator using both architectures, I and II, has been verified by computer simulation. The simulated overall and passband (0-600KHz) amplitude responses of the two circuits were obtained with arbitrary input signal formats and they are exactly the same, as illustrated in curve I and I' of Fig.4 respectively. For comparison, the overall and passband amplitude responses of the SC interpolator previously available for implementing the same interpolation but by employing a modified transfer function [1] is also plotted in Curve II and II', clearly showing that the responses are affected by the input sample-and-hold format due to the extra zeros at f_s and $2f_s$. When the output sample-and-hold effect at higher sampling rate $3f_s$=9MHz is considered, the amplitude responses in curve III and III' are obtained.

5. CONCLUSIONS

A more general, systematic design methodology, combining the non-recursive ADB polyphase and recursive direct-form II structures, for realising impulse sampled SC IIR interpolators, was introduced. The overall frequency response of such impulse sampled SC IIR interpolators is no longer affected by the sample-and-hold shaping effect at the lower input sampling frequency. Two SC architectures were proposed for implementation of the same 3rd order IIR lowpass interpolator. One with slower requirements of settling time of all OA's in the circuit, while the other has the advantage of requiring less ADB's and clock phases.

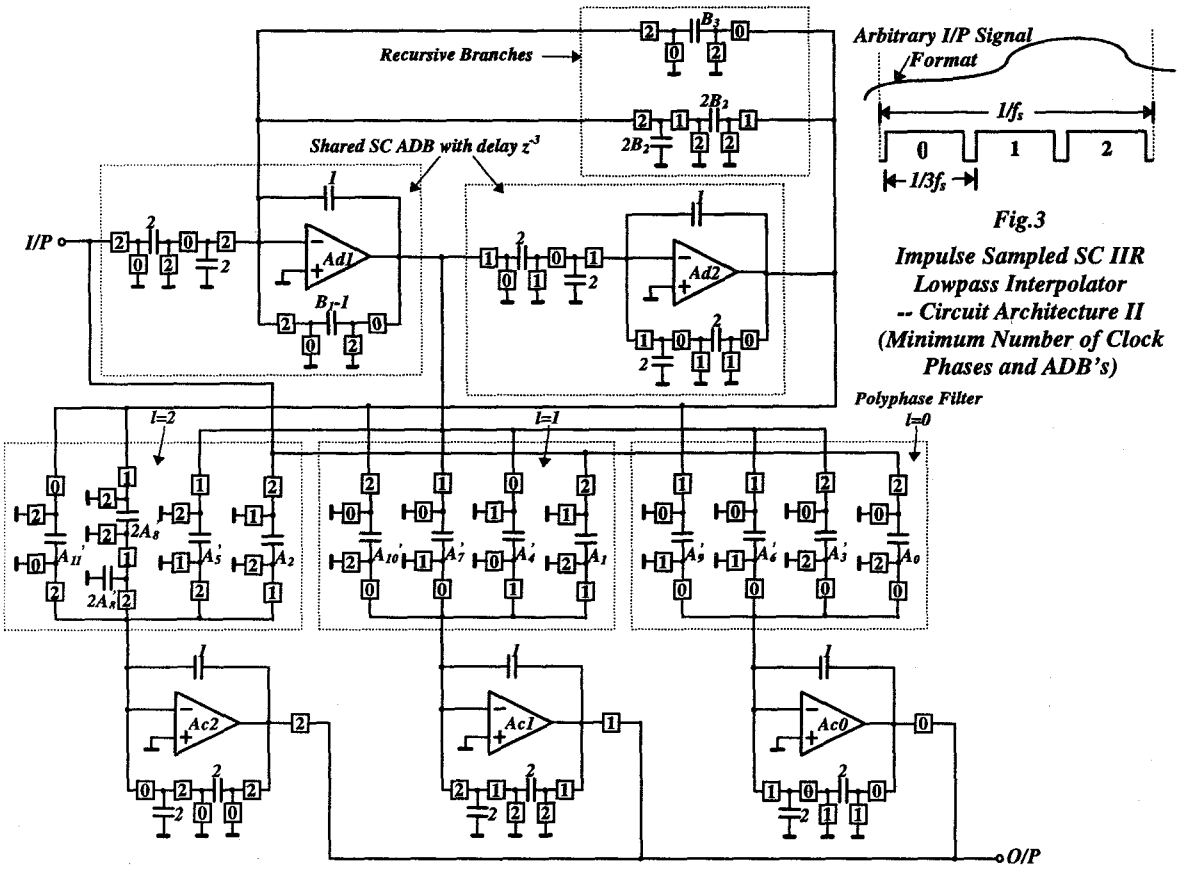

Fig.3
Impulse Sampled SC IIR Lowpass Interpolator -- Circuit Architecture II (Minimum Number of Clock Phases and ADB's)

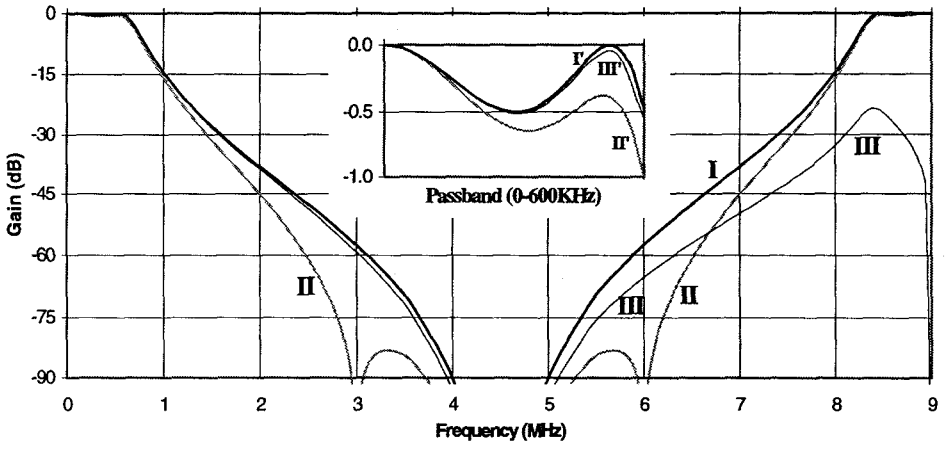

Fig.4
Computer Simulated Results of Impulse Sampled Lowpass SC IIR Interpolator - Both Circuit Architecture I and II

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