HIGH PERFORMANCE MULTIRATE SC CIRCUITS WITH PREDICTIVE CORRELATED DOUBLE SAMPLING TECHNIQUE

Seng-Pan U [1], R.P.Martins [1'], J.E.Franca [2]

1 - University of Macau, Faculty of Science and Technology, P.O.Box 3001, Macau, E-mail - fstspu@umac.mo
(1' - on leave from IST/Portugal, E-mail - rtorpm@umac.mo)

2 - Instituto Superior Técnico, Integrated Circuits and Systems Group, Av. Rovisco Pais, 1, 1096 Lisboa Codex, Portugal, E-mail - franca@gcsi.ist.utl.pt

ABSTRACT – This paper proposes the design of multirate Switched-Capacitor (SC) filters with the employment of the predictive Correlated Double Sampling (CDS) as a means of achieving higher accuracy, good linearity and higher dynamic range as well as lower power dissipation for high frequency and/or low voltage CMOS applications. Such new technique will be first explored by proposing the novel fundamental building blocks: unit delay circuit and accumulator for multirate SC circuits with the reduction of the effects of op-amp imperfections with respect to the input referred DC offset voltage, $1/f$ noise as well as finite gain, and then be consolidated by implementing a specific video application.

1. INTRODUCTION

The increased use of multirate sampled-data techniques has encouraged research activities for higher frequency CMOS applications, such as the video analog/digital interface [1,2], magnetic disk read channel coders [3], frequency subsampling downconvertion [4] and Direct Digital Frequency Synthesizer (DDFS) channel [5] for wireless CMOS transceiver. However, the large bandwidth of the active element – operational amplifiers (op-amp) trades off the open-loop gain that is often inadequate to obtain the satisfactory performance. Moreover, as the application- and technology-driven constraints are scaling down the system supply voltage, the achievable amplifier gain is often quite low for a better output signal swing. Besides, the DC offset and low frequency noise of amplifiers will reduce the dynamic range. Therefore, the compensation of these non-ideal properties of amplifiers becomes more and more necessary for modern analog integrated systems. The Correlated Double Sampling (CDS) technique, which samples and subtracts the amplifier noise and offset in each clock period, is inherently appropriate for sampled data circuits when compared with another chopper stabilization (CHS) technique which is preferable for continuous-time systems [6]. This paper proposes novel circuit architectures and building blocks for high performance multirate SC circuits with the employment of the Predictive CDS (P-CDS) technique which has the superiority over the conventional CDS of an exact compensation to the nonlinear gain characteristics of the amplifier in a much wider signal frequency range.

2. PREDICTIVE CDS (P-CDS) BUILDING BLOCKS FOR MULTIRATE SC CIRCUITS

The specialized multirate SC filters, namely decimators and interpolators, which are based on the polyphase structures, have been effectively proved to operate with less power and silicon dissipation due to higher efficiency in terms of the required number and speed of the active elements [7-12]. Generally speaking, they, either decimators or interpolators, can be mainly classified into Direct-Form (DF) [7,8], non-recursive Active-Delayed Block (ADB) [9,10], Recursive ADB [11,12] polyphase architecture for FIR or IIR filtering characteristics. Nevertheless, unity-delay circuits (unit delay is referred to the lower sampling period), namely ADB's and accumulators, are two fundamental building blocks for all these structures. Therefore, the unity-delay SC ADB circuits and SC accumulators with predictive CDS will be investigated in the following. Note that the ADB's in decimation circuits, which function for the combination of the unit-delay together with the accumulation due to the multi-feed-in SC coefficient-branches, can indeed be categorized into SC accumulator circuits.

2.1 Predictive CDS SC Unit-Delay ADB's with Mismatch-Free Property

As the SC unit-delay ADB's are cascaded as a serial processing delay line which contributes to the transfer function coefficients implementation, the nonlinear errors in ADB's will be accumulated along this serial delay line that will considerably affect the coefficients precision. We have proposed several different novel implementation of SC delay circuits that are all insensitive to finite gain, DC offset errors as well as capacitance mismatch in reference [13]. As they are all suitable for serving as ADB with an arrangement of multirate clock phases, and for simplicity, employed here is a more general and a highly accurate unit-delay circuits as presented in Fig.1 with clock phases. The gain and offset compensation is fulfilled by the predictive CDS technique [6,14,15] which predicts a much closer approximation of finite gain and offset errors that are expected to be presented in next output phase by performing a similar switching operation preliminarily, thus attaining a very accurate and almost frequency-independent compensation. Here, the double sampling C_1 and C'_1 branches generate unity delay multiplexly; and a sole C_F branch performs a similar preliminary operation for both double sampling SC branches for predicting the gain and offset errors at virtual ground which will be stored in the offset-storage capacitor C_h. The resulting gain and phase errors caused by finite gain is extremely small, i.e. <0.0036dB and <0.0078° with A=100 and all parasitics (10% of unit capacitance) [13]. It is also evident that there is no charge transferring operation, thus eliminating the physical mismatch problem of capacitance ratio.

0-7803-5471-0/99/$10.00©1999 IEEE

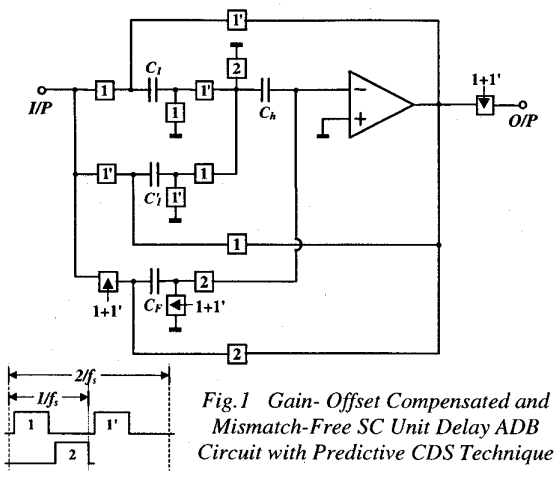

Fig.1 Gain- Offset Compensated and Mismatch-Free SC Unit Delay ADB Circuit with Predictive CDS Technique

2.2 Predictive CDS SC Accumulator/Summer

The errors in output SC accumulator mainly leads to a nonlinear deviation of the transfer function coefficients as well as the overall gain response offset. We implement here in Fig.2(a)-(c) three different types of P-CDS SC accumulator circuits by using the same sample correction property [16]. These circuits predict and correct the finite gain and offset errors by switching the virtual ground from uncompensated to error-compensated during the same charge transferring phase with the only one same sample. This indeed is fulfilled by a small error correction capacitor C_e at the inverting node of amplifier. Note that the value of this capacitor should be as small as possible – normally set to unit capacitance, due to the fact that the additional charge redistribution between it and accumulation capacitor C_A will occur during the error-prediction phase. Nevertheless, the accumulation capacitor has normally the biggest value in whole circuit as it is the denominator of coefficient capacitance ratios, which means the ratio $k=C_e/C_A$ is relatively small in most cases, thus a small error will be introduced. In fact, even for the worst case, i.e. ratio is unity, the gain and phase errors are still better than conventional CDS technique (discussed next).

Note that the clock phases of Fig.2a and Fig.2b are simplified for easy to apply in also other general purpose SC circuits. The circuit in Fig.2b is the modified version of Fig.2a with a special feedback branch C'_A for transferring the charges accumulated in phase 1 to C_A at phase 2, thus allowing that the charge transfer or summation can be occurred in both two phases 1 and 2 which is especially suitable for decimation circuits. Meanwhile, the summation is only valid in phase 2 in circuit of Fig.2a due to the reset of accumulation capacitor in phase 1. The circuit of Fig.2c, which is specialized for sampling rate change of 4, is also derived from Fig.2a with the multiplexed summing capacitors for efficiently acting as one time-shared accumulator for multiple polyphase filter paths especially for SC interpolators.

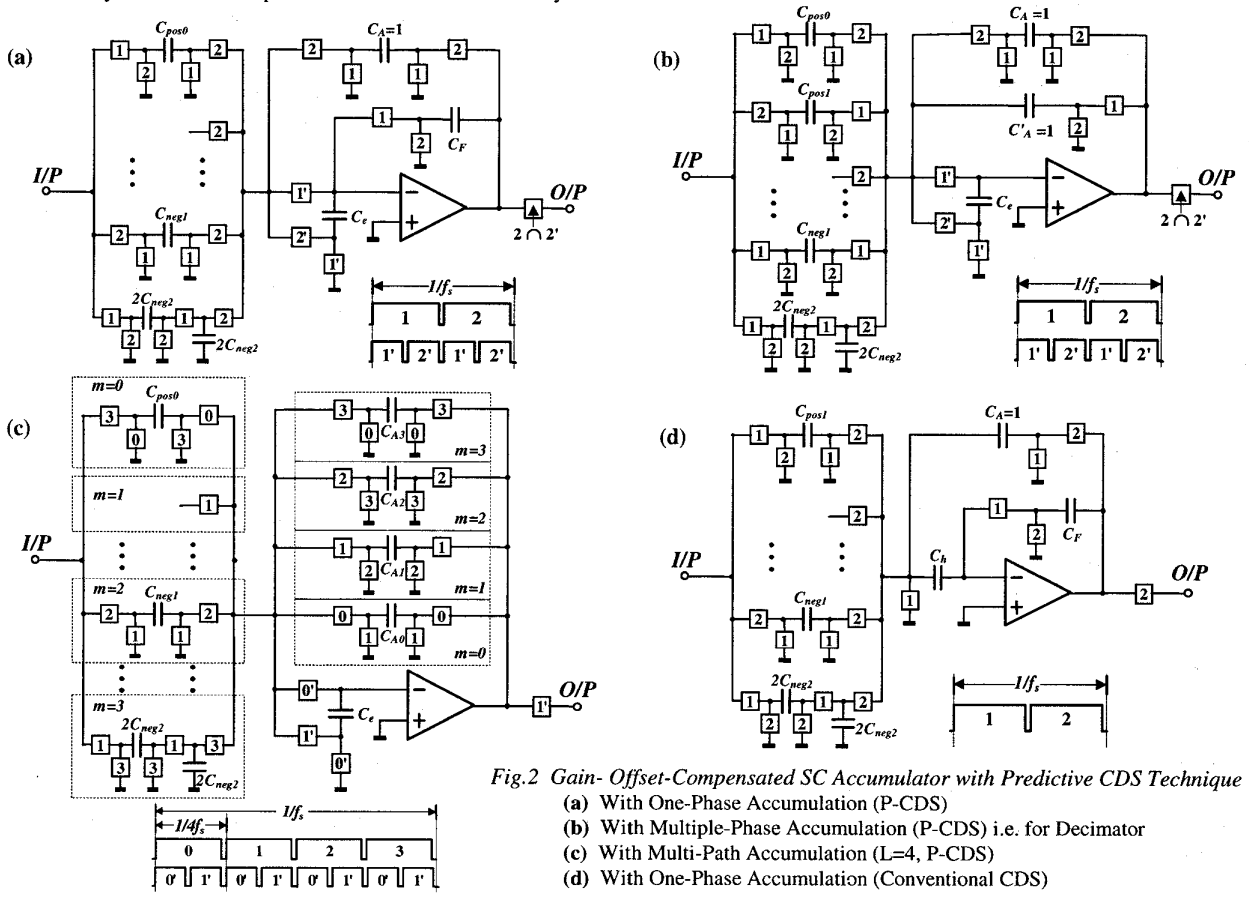

Fig.2 Gain- Offset-Compensated SC Accumulator with Predictive CDS Technique
(a) With One-Phase Accumulation (P-CDS)
(b) With Multiple-Phase Accumulation (P-CDS) i.e. for Decimator
(c) With Multi-Path Accumulation (L=4, P-CDS)
(d) With One-Phase Accumulation (Conventional CDS)

The gain and phase as well as offset errors are all obtained both from theoretical calculation and computer simulation which both show a very good consistency between their results. The standard uncompensated SC accumulator proposed in [7] and a GOC accumulator with the conventional CDS presented in Fig.2d will be utilized for comparison. The SWITCAP simulated results are shown in Fig.3. For a more conservative study, we consider the moderate coefficient spread of 6, thus $k=C_e/C_A=1/6$, the errors caused by finite gain of circuit Fig.2a and b are almost the same as shown in curve I and II respectively, and the maximum gain and phase errors are about 0.03dB and -0.1° which are much better than 0.2dB & -0.65° in curve III and 0.4dB & -1.1° in IV for Conventional CDS (C-CDS) circuit of Fig.2d and uncompensated one respectively. More importantly, the minimum gain errors at DC for all CDS circuits are around 0.002dB while the uncompensated is 0.1dB which is about 50 times of CDS cases. In addition, as mentioned before, even for the worst case: $k=C_e/C_A=1$ (coefficient spread =1), the circuits with P-CDS are still much superior to conventional CDS or standard uncompensated cases, as shown in curves I', II', III' and IV'. Simulated results also show that the parasitics (10% of the unit capacitor) at all adjoined nodes slightly increase the gain error by only less than 0.0037dB which can be neglected. Moreover, the suppression factor to DC offset voltage becomes approximately $1/A$ for circuits with CDS technique while it is about 2 for the uncompensated.

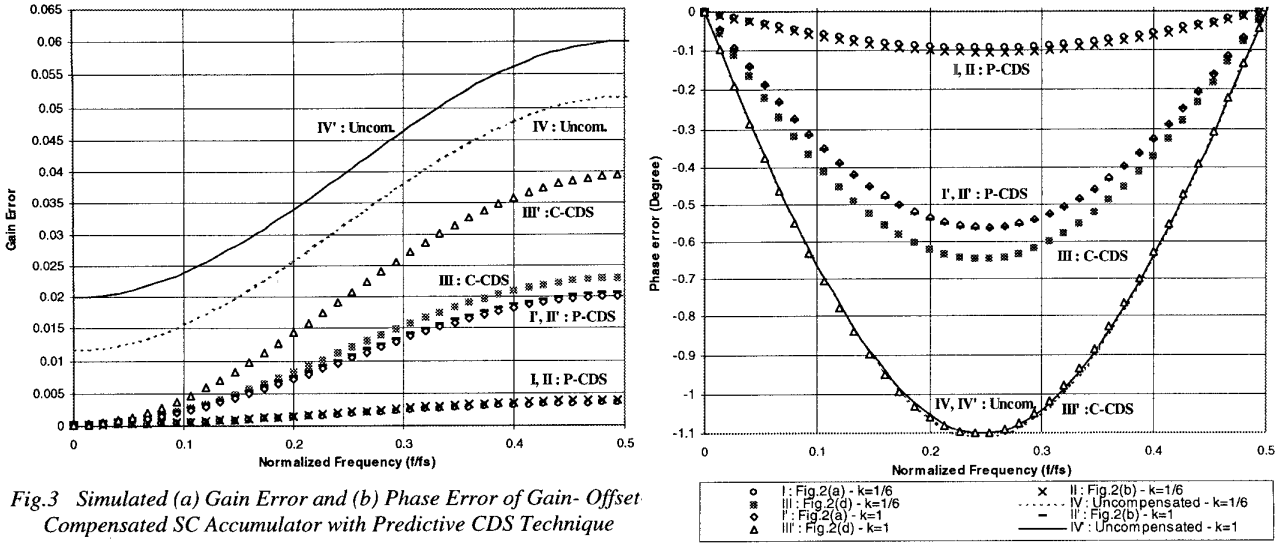

Fig.3 Simulated (a) Gain Error and (b) Phase Error of Gain- Offset Compensated SC Accumulator with Predictive CDS Technique

3. DESIGN EXAMPLE OF PREDICTIVE CDS MULTIRATE SC CIRCUITS

The effectiveness of the proposed P-CDS building blocks for multirate circuits has been established by implementing a 4-fold SC multirate video interpolator with amplifier's gain of 100. Such interpolator increases sampling rate by 4 fold and achieves the 15-tap FIR lowpass filtering which requires passband ripple less than 0.2dB with linear phase characteristics and attenuation of the images greater than 50dB. For simplicity and generalization, only the simulated results of the circuit employing the novel P-CDS unit-delay ADB in Fig.1 and multi-feed-in time-shared accumulator in Fig.2c are presented here in Fig.4. It is clearly evident that the transmission zeros variation due to the finite gain error is so extremely small as plotted in the zeros patterns of Fig 4b that the simulated amplitude responses are almost fully matched to the ideal one as shown in Fig.4a. While for the uncompensated one, its maximum passband and stopband variation are more than 0.7dB and 10dB respectively due to the distorted location of zeros shown in Fig.4b. For comparison, the simulated results of interpolator with conventional CDS technique are also presented in Fig.4a whose performance is better than the uncompensated but worse than predictive CDS circuit due to its inherent narrow band compensation property. Note that the comparison is indeed just a conservative simulation in studying its impact in view of the neglect of the capacitance mismatch in ADB's and DC offset error in these circuits.

4. CONCLUSION

The novel specific gain- and offset-compensated techniques for high performance multirate SC circuits in terms of the accuracy, linearity and dynamic range by manipulating the predictive correlated double sampling have been presented, thus exploring its potential for high speed and low voltage applications. The fundamental P-CDS SC multirate building blocks, namely the mismatch-free unit delay circuits and accumulators have been proposed with their superiority in terms of their considerably small gain, phase and offset errors. More importantly, these building blocks can be actually treated as the standard cells for normal SC circuits in many applications. Moreover, a real video interpolation filter has been realized by combining such blocks with an almost ideal response. All these circuit behaviors have been verified

successfully by both rigorous theoretical and computer simulated analyses with also a detailed comparison with traditional uncompensated and the conventional CDS implementations.

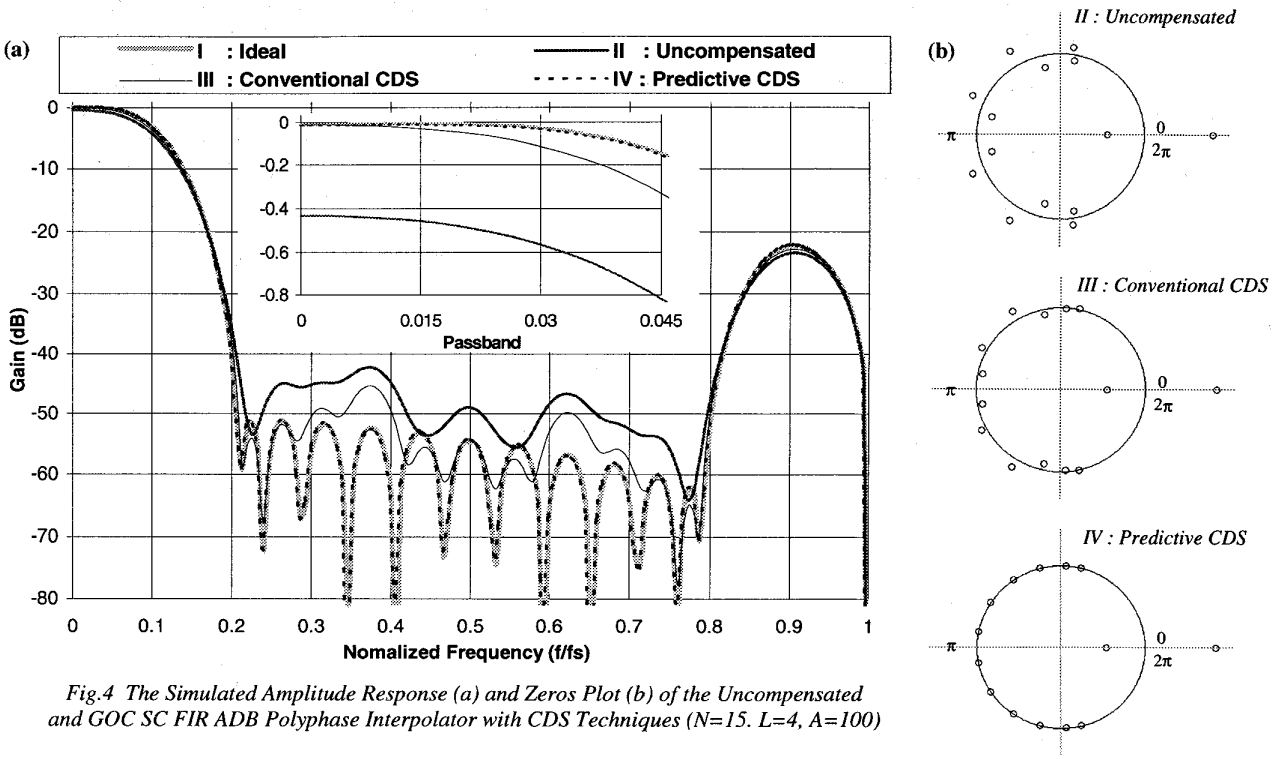

Fig.4 The Simulated Amplitude Response (a) and Zeros Plot (b) of the Uncompensated and GOC SC FIR ADB Polyphase Interpolator with CDS Techniques (N=15. L=4, A=100)

References :

[1] R.P.Martins, J.E.Franca, "A 2.4μm CMOS Switched-Capacitor Video Decimator with Sampling Rate Reduction From 40.5MHz to 13.5MHz," in *Proc. IEEE CICC*, May 15-19, San Diego, USA, 1989.

[2] M. Segato, A. Baschirotto, G. Biaggioni, G. Cortelazzo, E. Malavasi, "SC realization of anti-aliasing CCIR-601 video filters," *IEEE Trans. on Consumer Electronics*, Vol.40, No.3, pp.274-281, Aug.1994

[3] G.T.Uehara, P.R.Gray, "Practical Aspects of High Speed Switched-Capacitor Decimation Filter Implementation," in *Proc. IEEE ISCAS*, San Diego, USA, May, 1992.

[4] R.F.Neves, J.E.Franca, "A Switched-Capacitor N-Path Decimating Filter," in *Proc. IEEE ISCAS'98*, pp.I-472-I-475, USA, May, 1998.

[5] P.J.Santos, J.E.Franca, "Switched-Capacitor Interpolator for Direct-Digital Frequency Synthesizers," in *Proc. IEEE ISCAS'98*, USA, May, 1998.

[6] Christian C.Enz, G.C.Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," *Proc. of The IEEE*, Vol.84, No.11, pp.1584-1614, Nov.1996.

[7] J.E.Franca, "Non-recursive Polyphase Switched-Capacitor Decimators and Interpolators," *IEEE Trans. Circuits and Systems*, Vol. CAS-32, No.9, pp.877-887, Sep. 1985.

[8] U Seng Pan, R.P.Martins, J.E.Franca, "Switched-Capacitor Interpolators Without the Input Sample-and-Hold Effect," *Electronics Letters*, Vol.32, No.10, pp.879-881,May 1996.

[9] J.E.Franca, S.Santos, "FIR Switched-Capacitor Decimators with Active-Delayed Block Polyphase Structures," *IEEE Trans. Circuits and Systems*, Vol. CAS-35, pp.1033-1037, Aug. 1988.

[10] Seng-Pan U, R.P.Martins, J.E.Franca, "Impulse Sampled FIR Interpolation With SC Active-Delayed Block Polyphase Structures," *Electronics Letters*, Vol.34, No.5, pp.443-444, 5th Mar.1998.

[11] W.Ping, J.E.Franca, "New Form of Realization of IIR Switched-Capacitor Decimators," *Electronics Letters*, Vol.29, No.11, pp.953-954, 27th May 1993.

[12] U Seng Pan, R.P.Martins, J.E.Franca, "New Impulse Sampled IIR Switched-Capacitor Interpolators," in *Proc. IEEE ICECS'96*, pp.203-206, Rodos, Greece, Oct.1996.

[13] Seng-Pan U, R.P.Martins, J.E.Franca, "Highly Accurate Mismatch-Free SC Delay Circuits with Reduced Finite Gain and Offset Sensitivity," in *Proc. IEEE ISCAS'99*.

[14] L.E.Larson, G.C.Temes, "Switched-Capacitor Gain Stage with Reduced Sensitivity to Finite Amplifier Gain and Offset Voltage," *Electronics Letters*, Vol.22, No.24, pp.1281-1282, Nov.1985.

[15] K.Nagaraj, T.R.Viswanathan, K.Singhal, J.Vlach, "Switched-Capacitor Circuits with Reduced Sensitivity to Amplifier Gain," *IEEE Trans. on CAS*, Vol.CAS-34, No.5, pp.571-574, May 1987.

[16] H.Shafeeu, A.K.Betts, J.T.Taylor, "Novel Amplifier Gain Insensitive Switched Capacitor Integrator with Same Sample Correction Properties," *Electronics Letters*, Vol.27, No.24, pp.2277-2279, Nov.1991.