# A Reduced Jitter-Sensitivity Clock Generation Technique for Continuous-Time ΣΔ Modulators

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***Abstract*—A clock generation technique for reducing the clock-jitter sensitivity of Switched current (SI) Return-to-Zero (RZ) DAC in CT ΣΔ modulators is presented in this paper. While realizing the clock-jitter insensitivity, this technique ensures that the feedback period can be utilized more efficiently so that the amplitude of feedback current can be reduced. The proposed technique employs simple digital elements to generate a fixed-pulse-width feedback control clock. It was verified in a 2nd order, 1-bit CT ΣΔ modulator with SI RZ feedback. Simulation result shows that the clock-jitter tolerance using the proposed technique is up to 2% of a clock cycle with SNDR larger than 62dB. While using the traditional clock generation method, clock-jitter tolerance is only 0.1% of a clock cycle.**

***Keywords*—Clock-jitter sensitivity, continuous-Time, sigma-delta modulator, switched current DAC.**

## I. INTRODUCTION

Continuous-Time ΣΔ Modulator (CTSDM) is being a popular choice in mobile communication system with its advantages of low power, high speed and inherent anti-aliasing function. However CTSDM has its own practical non-idealities comparing with Discrete-Time (DT) SDM, the feedback Pulse-Width (PW) variation caused by the jitter in master clock can significantly degrade system performance [1] [2]. Jitter-induced PW variation will directly introduce feedback noise to the input of the integrator. Especially for the first stage loop filter, this noise cannot be shaped by noise shaping function.

Two types of feedback are the most common choice in CTSDM implementations. One is Non-Return-to-Zero (NRZ) feedback and the other is Return-to-Zero (RZ) feedback. RZ feedback has a better tolerance on Excess Loop Delay (ELD) in contrasting to NRZ method. But it is more sensitive to clock-jitter effect. Comparing with NRZ method, RZ feedback suffers the jitter effect on both rising and falling clock edges [1] [2]. The jitter-induced PW variation will change the feedback pulse shape in every feedback period. It leads the total feedback charges vary randomly in every period, which is equivalent as white noise.

RZ feedback leaves time margin for DAC operations, hence the existing solutions on clock-jitter sensitivity reduction are mostly proposed based on RZ feedback. In existing literatures, shaped-feedback waveform is a popular technique to reduce clock-jitter effect. Several such types of DAC were proposed, such as the SCR DAC proposed in [3] and the SCSR DAC proposed in [4]. This type of feedback DAC has some disadvantages: SCR DAC increases the requirement of slew rate and GBW of the integrator; SCSR DAC requires complicated control phases. In the design of shaped-feedback waveform DAC, a careful choose of discharge time constant is required to guarantee that neither compromise the jitter insensitivity nor cause nonlinear problem in op-amp.

In practice, shaped-feedback waveform method cannot control the amount of feedback charge to be a defined value, it is because clock-jitter will more or less change the feedback current area even this effect has been reduced. A method that can fix the feedback PW and reduce the jitter sensitivity would be preferred. In [5], a simple technique to generate jitter insensitive feedback control clock is introduced. It can fix the PW of a rectangular feedback pulse immune to clock-jitter effect. However this technique has a limitation on the width of feedback pulse. The detail discussion of this limitation will be presented in Section II.

In this paper, a jitter insensitive clock generation technique with extended feedback PW is proposed. Inverter-based delay line is applied to generate a series of delayed clock signals then determine the feedback PW by logic operations. D-Flip-Flop (DFF) is employed to generate the control clock to SI DAC. To make a comparison, both proposed and traditional RZ feedback techniques were implemented in a designed 2nd order single-bit CTSDM.

A detail discussion of the proposed jitter insensitive clock generation technique is presented in Section II. A CTSDM design and implementation to verify the effectiveness of the proposed technique are given in Section III. Section IV shows the comparison of the simulation results of using proposed and traditional feedback technique. Finally a conclusion is summarized in Section V.

## II. JITTER INSENSITIVE CLOCK GENERATION TECHNIQUE

### *A. PW Limitation*

A method to generate jitter-reduced control clock to the SI feedback DAC is introduced in [5]. However by using this

technique, the generated PW of the control clock cannot be larger than 50% of a clock cycle ($0.5T_s$). In practice, because of the consideration of the time margin leaving for tolerating clock-jitter effect, the practical generated PW should be within $0.4T_s$ if the maximum jitter tolerance is 5% of a clock cycle. Hence more than half of the feedback period cannot be utilized which causes higher feedback current amplitude. This limitation is due to the method of generating the feedback pulse. The core part of the technique introduced in [5] is shown in Fig. 1.

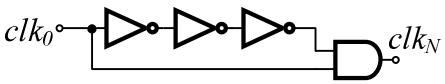


Fig. 1 Jitter reduced clock generator.

$clk_N$ is the generated clock to control the feedback pulse. Because it is generated by simply delaying the single phase master clock then do AND operation, the feedback PW cannot be wider than 50% of a cycle of $clk_0$. This PW limitation causes the inefficient utilization of the feedback period. In more than half of a clock cycle, there is no feedback operation. This leads also the increase of feedback current amplitude.

*B. Jitter Insensitive Feedback with Extended PW*

The proposed jitter insensitive clock generation technique is shown in Fig. 2. The circuit implementation consists of an inverter-based delay line, a logic AND gate and a DFF. Its operation principle is illustrated by the waveforms shown in Fig. 3. The operations under different conditions, without and with clock-jitter, will be introduced respectively.

*1). Without clock-jitter effect.* In ideal case, there is no jitter in the single phase master clock $clk_0$. The red regions in Fig. 3 which denote the jittered clock edges can be ignored here. $clk_0$ is passed through the inverter-based delay line then several delayed clocks can be generated. $clk_{d1}$ is generated by delaying $clk_0$ by $t_{d1}$. It is used to triggering the DFF to control the SI DAC feedback. The delay time $t_{d1}$ is the time distance between sampling time instants and feedback time instants. $t_{d1}/T_s$ is the value of $\alpha$ when applying the method introduced in [2] to calculate the RZ feedback coefficients. When the DFF is triggered by $clk_{d1}$, it will detect the modulator's output then transfer it to output terminal Q. Since the settling of quantizer can be finished in $t_{d1}$, the DFF can correctly determine the feedback polarity. For easy observation, $V_{out}$ is assumed as '1' in the illustration in Fig. 3. The delay enhancement loading shown in Fig. 2 were implemented by parallel connected inverters.

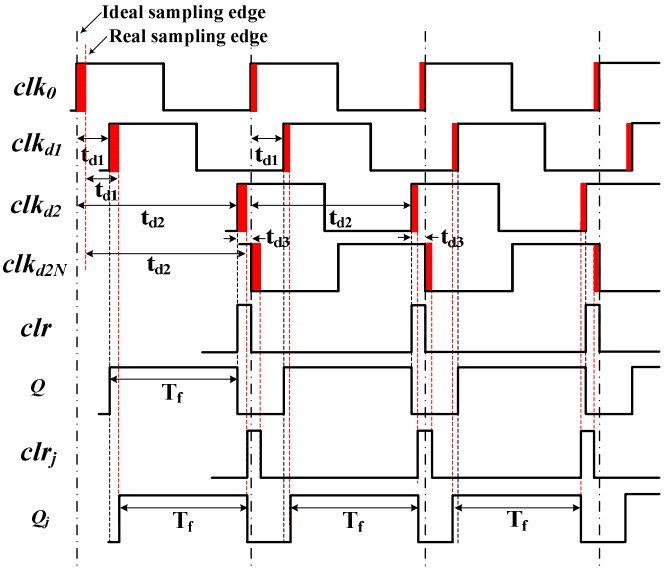


Fig. 3 Operation principle of the proposed technique.

$clk_{d2}$ is generated by delaying $clk_0$ by $t_{d2}$. $t_{d2}/T_s$ is the value of $\beta$ in RZ feedback coefficients calculation. $clk_{d2N}$ shown in Fig. 3 is generated by inverting and delaying $clk_{d2}$ by $t_{d3}$. By doing AND operation to $clk_{d2}$ and $clk_{d2N}$, the reset clock $clr$ of the DFF can be generated as shown in Fig. 3.

The DFF is triggered by $clk_{d1}$ then generates the SI DAC control signal. So the feedback phase is started from $(t_0 + t_{d1})$ in every period. After $t_{d2}$, $clr$ resets the DFF then the output $Q$ is cleared to '0' and the feedback current is switched off. Clock $Q$ shown in Fig. 3 is the feedback control clock of the SI DAC. The PW $T_f$ of the feedback current is equal to the PW of clock $Q$ which is $T_f = (t_{d2} - t_{d1})$ as shown in Fig. 3. This PW can be larger than half of $T_s$, in this work $T_f$ is set as $0.7T_s$.

*2). With clock-jitter effect.* The red regions in Fig. 3 represent the jitter caused PW variation. Only the jittered rising edges are marked because all the related clocks are generated based on the rising edge of the master clock. Jitter on the falling edges does not affect the feedback pulse shape. Since $clk_{d1}$, $clk_{d2}$ and $clk_{d2N}$ are all generated by delaying the master clock, jitter caused PW variation cannot affect the relative positions between $clk_0$ and each of them. It means the delay time $t_{d1}$, $t_{d2}$ and $t_{d3}$ are not affected by clock-jitter. Thus the feedback PW $T_f$ is not affected by clock jitter. The jittered $clr_j$ and $Q_j$ shown in Fig. 3 show that comparing with ideal case the only effect induced by the clock-jitter is the time interval between the end of the feedback pulse and the next

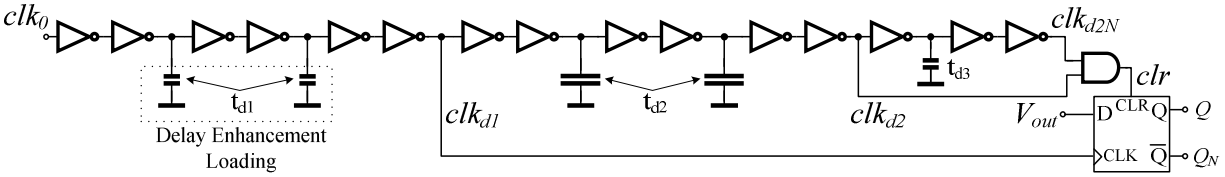


Fig. 2 The proposed jitter insensitive clock generation technique.

sampling edge. This effect does not change the width and position of feedback pulse; therefore it will not increase feedback noise. The value of $t_{d1}$ and $t_{d2}$ are chosen based on the required jitter tolerance in a design.

## III. CTSDM Design and Implementation

To verify the effectiveness of the proposed clock-jitter insensitive feedback technique, a 2nd order, single-bit CTSDM with RZ SI feedback is designed and implemented in 65nm CMOS with 1V supplied voltage.

### A. CTSDM Design

The systematic architecture of the designed 2nd order, single-loop, 1-bit CTSDM is shown in Fig. 4.

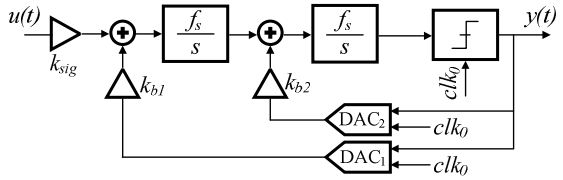


Fig. 4 2nd order 1-bit CTSDM architecture.

The clock rate of the designed CTSDM is 250MHz and the signal bandwidth is 2MHz which is targeted on the baseband standard of 3G WCDMA receivers. The oversampling ratio is 64. Based on the corresponding coefficients in DT case, the CT coefficients were obtained by using impulse invariant transform. With the scaled CT coefficients, Matlab model simulation gives a 73dB SNDR in ideal case.

The schematic of the designed CTSDM is shown in Fig. 5. The 2nd order loop filter was implemented by employing active RC integrators for good linearity. The op-amp in the 1st stage integrator was implemented using folded-cascode structure with gain boosting amplifier. The requirement of the 2nd stage op-amp is much relaxed. The single-bit quantizer was implemented using output latched dynamic comparator.

The feedback phase is from $\alpha T_s$ to $\beta T_s$ in RZ feedback. In this design, $\alpha$ is set as 0.2 to leave enough time for quantizer settling. $\beta$ is chosen as 0.9 in order to tolerate 5% of a clock cycle jitter effect. The feedback pulse shape is shown in Fig. 6. A comparison to the feedback pulse shape in [5] is also provided. It can be seen that the proposed technique can extend the feedback PW by $0.3T_s$, thus the normalized feedback current is reduced by 43%.

### B. Feedback DAC Design

SI feedback DAC was employed in the designed CTSDM as shown in Fig. 5. The circuit of the SI feedback DAC connected to the 1st stage integrator is given in Fig. 7 [6]. The charge dump control circuit is shown in Fig. 7(b). When feedback current is switched off, $d_p$ and $d_n$ will turn on the switches to transfer the charge from the cascade current source to a supplied voltage source. This operation is for

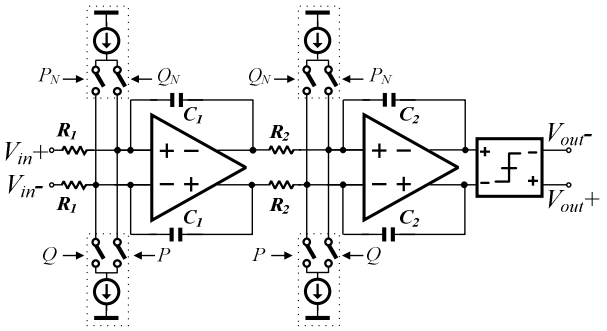


Fig. 5 Circuit implementation of the 2nd order, 1-bit, CTSDM.

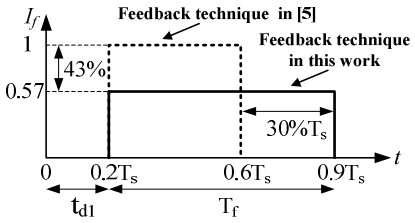


Fig. 6 Comparison of feedback pulse shapes.

avoiding the transistors of current source going into triode region, because it will take a long recovery time [7]. Fig. 7(c) shows the DFFs in the clock generation circuit shown in Fig. 2 to generate control signal to switch on/off feedback current.

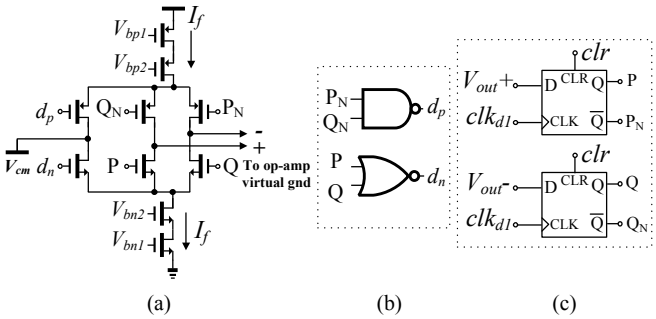


Fig. 7 (a) SI component in feedback DAC. (b) Charge dump control generation. (c) Current switch control generation.

## IV. Simulation Results

The proposed clock-jitter insensitive feedback technique was verified by the simulation on transistor level. The testing signal is a -2dBFS sine wave at 100kHz. Thermal noise, kT/C noise, flicker noise and quantization noise were simulated by transient noise simulation. Clock-jitter was injected into the master clock. Fig. 8 gives out the simulated results for the CTSDM using proposed and traditional feedback techniques with the clock-jitter-induced PW variation form 0.001% to 5% of a clock cycle. Through the comparison in Fig. 8, it can be seen that the proposed jitter insensitive feedback technique can effectively reduce the clock-jitter effect and improve the SNDR up to 25dB. With 62dB SNDR requirement, the CTSDM employing proposed jitter insensitive technique can

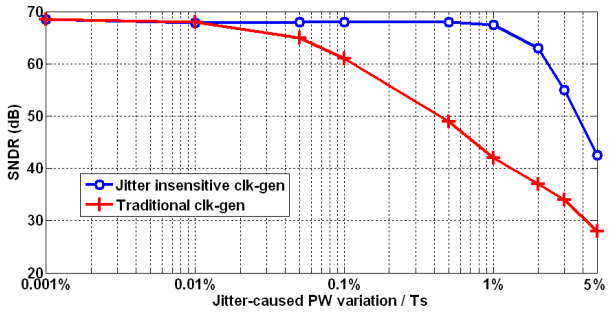


Fig. 8 Simulation result of the clock-jitter effect to the designed CTSDM with the proposed jitter insensitive and the traditional feedback DAC.

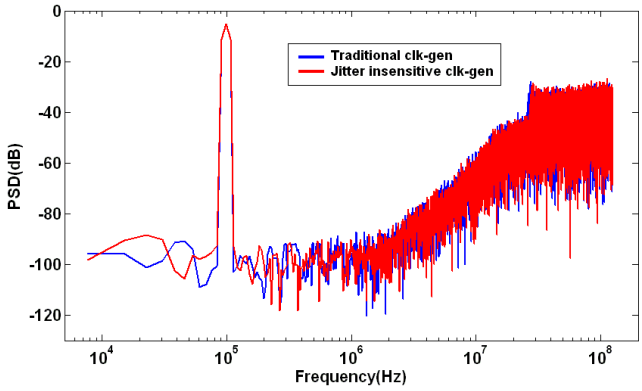


Fig. 9 PSDs of the simulated results for the CTSDM using proposed and traditional feedback without clock-jitter effect.

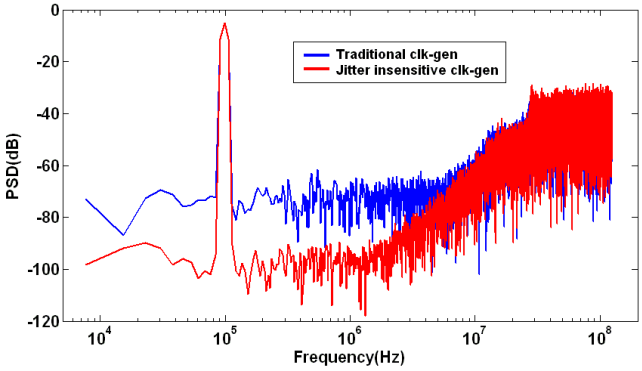


Fig. 10 PSDs of the simulated results for the CTSDM using proposed and traditional feedback with 1% of the clock cycle clock-jitter effect.

tolerate the jitter-induced PW variation up to 2% of a clock cycle while the CTSDM using traditional jitter sensitive clock generation can tolerate only 0.1%.

The Power Spectrum Densities (PSDs) of the simulated results are shown in Fig. 9 and Fig. 10. Fig. 9 shows the comparison of the simulated PSDs for the CTSDM using proposed and traditional feedback technique without clock-jitter effect. Both results have the very similar PSD shape and quite closed noise floor.

The PSDs of the simulated results with 1% of a clock cycle jitter-induced PW variation are shown in Fig. 10. It can be seen that the noise floor of the result using proposed jitter insensitive technique is almost not changed comparing with the case of no jitter effect. But the noise floor of the result using traditional feedback technique is increased by more than 20dB which results the SDNR dropped to 43 dB.

The total power consumption of the designed CTSDM using proposed feedback technique is 4.1mW. Thereinto the 1st and the 2nd stage RC integrator consume 2.3mW and 1.05mW power respectively. The proposed clock generation circuit consumes less than 300μW power only. While the power consumption of the CTSDM employed traditional clock-jitter sensitive feedback technique is 4.03mW. The proposed reduced jitter-sensitivity clock generation technique does not increase power consumption clearly.

## V. Conclusions

In this paper, a jitter insensitive clock generation technique is proposed for RZ SI feedback DAC used in CTSDMs. Rectangular feedback pulse shape was employed for low feedback current amplitude and easy generation. Without compromising clock-jitter reduction function, the feedback PW generated by using proposed technique was extended in order to reduce the feedback current amplitude and utilize the feedback period more efficiently. The jitter insensitivity of the proposed technique was verified by simulated a designed 2nd order, 1-bit CTSDM in transistor level. Simulation results show that the proposed technique can effectively reduce the CTSDM's clock-jitter sensitivity without evident increase of system power consumption.

## Acknowledgment

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