

Design of an ESD-Protected Ultra-Wideband LNA in Nanoscale CMOS for Full-Band Mobile TV Tuners

Pui-In Mak, *Member, IEEE*, and Rui Martins, *Fellow, IEEE*

Abstract—This paper presents an electrostatic discharge (ESD)-protected ultra-wideband (UWB) low-noise amplifier (LNA) for full-band (170-to-1700 MHz) mobile TV tuners. It features a PMOS-based open-source input structure to optimize the I/O swings under a mixed-voltage ESD protection while offering an inductorless broadband input impedance match. The amplification core exploiting double current reuse and single-stage thermal-noise cancellation enhances the gain and noise performances with high power efficiency. Optimized in a 90-nm 1.2/2.5-V CMOS process with practical issues taken into account, the LNA using a constant- g_m bias circuit achieves competitive and robust performances over process, voltage and temperature variation. The simulated voltage gain is 20.6 dB, noise figure is 2.4 to 2.7 dB, and IIP3 is +10.8 dBm. The power consumption is 9.6 mW at 1.2 V. $|S_{11}| < -10$ dB is achieved up to 1.9 GHz without needing any external resonant network. Human Body Model ESD zapping tests of ± 4 kV at the input pins cause no failure of any device.

Index Terms—CMOS, electrostatic discharge (ESD), low-noise amplifier (LNA), mobile TV tuner, radio frequency (RF), thermal-noise cancellation, ultra-wideband (UWB).

I. INTRODUCTION

A LARGE number of independently developed mobile TV standards worldwide has led to the demand of multiband silicon tuners for cost minimization of the embedded handheld devices that are intended for global market sale. Presently, the most dominant mobile TV standards are: terrestrial—digital multimedia broadcasting (T-DMB), integrated services digital broadcasting—terrestrial (ISDB-T), MediaFLO, digital video broadcasting—handheld (DVB-H) and digital multimedia broadcasting—terrestrial (DMB-T). Their brief profiles are listed in Table I.

From the implementation viewpoint, the digital back-end can be efficiently shared since those standards favor similar kinds of modulation and data coding. For the radio frequency (RF) front-end, however, state-of-the-art solutions still require dedicated RF circuits optimized for each band, e.g., [1]. Yet, with the advance of fabrication technologies, multistandard-compliant system-on-chip (SoC) solutions using wideband techniques to

TABLE I
BRIEF PROFILES OF THE MOST DOMINANT MOBILE TV STANDARDS

Mobile TV Standard	Frequency	Data Coding	Air Interface
T-DMB (Korea, China, Europe)	174 – 245 MHz 1452 – 1492 MHz	Video: H.264 30 fps/QVGA Audio: BSAC/AAC+	OFDM (QPSK)
ISDB-T (Japan, Brazil)	470 – 770 MHz	Video: H.264 15 fps/QVGA Audio: AAC+	OFDM (QPSK/16QAM)
DVB-H (Europe, US)	470 – 860 MHz 1670 – 1675 MHz	Video: H.264 30 fps/QVGA Audio: AAC+	OFDM (QPSK/16QAM/64QAM)
DMB-T (China)	470 – 860 MHz 1670 – 1675 MHz	Video: H.264 30 fps/QVGA Audio: AAC+	OFDM (QPSK/16QAM/64QAM)
MediaFLO™ (US)	712–722 MHz	MPEG4 (Video)	OFDM

cover multiple applications would have the highest potential to yield the optimum cost [2].

This paper presents the circuit techniques enforced in the design of an electrostatic discharge (ESD)-protected ultra-wideband (UWB) low-noise amplifier (LNA) for mobile-TV applications. It covers the full band of mobile-TV services from 170 to 1700 MHz such that only one LNA is necessary to support multiple standards. Unlike the design of narrowband LNAs, concurrent reception over a wide range of spectrum necessitates the LNA to feature high linearity, preventing desensitization by the high-power blockers. This requirement, in conjunction with the design goals of high ESD protection level, low noise figure (NF), low power, impedance match, and high gain, constitute hard tradeoffs to obtain a sensible balance in between. Being realized in a 90-nm CMOS process, the proposed LNA is optimized by introducing novel circuit techniques, together with careful sizing and biasing strategies, to achieve competitive and robust RF performances over process, supply voltage, and temperature (PVT) variations.

The organization of this paper is as follows. Section II describes the circuit structure and design issues of the proposed LNA. The practical issues governing the robustness of the LNA over PVT variation are summarized in Section III. The simulation results and benchmarks of this work to prior arts are given in Section IV. Section V concludes the paper.

II. CIRCUIT DESCRIPTION

A. Full-Band Mobile-TV Tuner Architecture

Fig. 1 shows the block diagram of the full-band mobile-TV tuner to which the proposed LNA is referred. The architecture is based on a direct-conversion receiver that is differential to avoid common-mode pickups and even-order distortion. As addressed

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P.-I. Mak is with the Analog and Mixed-Signal VLSI Laboratory, University of Macau, Taipa, Macao, China (e-mail: pimak@umac.mo).

R. Martins is with the Analog and Mixed-Signal VLSI Laboratory, University of Macau, Taipa, Macau, China, and also with the Instituto Superior Técnico (IST)/TU of Lisbon, 1049-001 Lisbon, Portugal (e-mail: rmartins@umac.mo).

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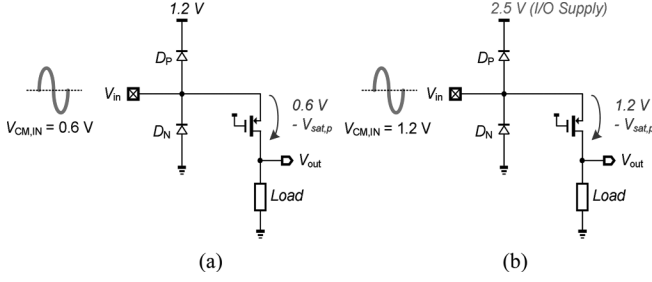


Fig. 4. Diode clamps with a pMOS-input structure. (a) $V_{CM,IN} = 0.6$ V. (b) $V_{CM,IN} = 1.2$ V, but the clamping voltage is the $V_{DD,I/O} = 2.5$ V.

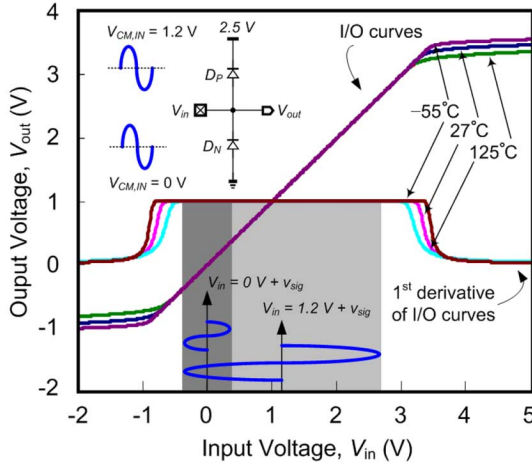


Fig. 5. Diode-clamp I/O transfer curves and their first derivatives at different temperatures, showing the linear input swing versus the selected $V_{CM,IN}$.

diode-clamp I/O transfer curves and their first derivatives at typical and extreme temperatures (Fig. 5). With $V_{CM,IN} = V_{DD} = 1.2$ V, the linear input $[v_{sig}(t)]$, even at the highest temperature, has a swing of roughly $3 V_{pp}$ in the pMOS case, while it is just roughly $0.8 V_{pp}$ in nMOS case with $V_{CM,IN} = GND$ (0 V).

C. Double Current Reuse for g_m -Enhancement

Current reuse is power-efficient in gain enhancement. In this study, current is doubly reused to boost the transconductance (g_m). A simplified small-signal half-circuit equivalent of Fig. 2 is shown in Fig. 6. First, M_1 gate-source terminals are coupled with a gain of -1 (i.e., capacitive cross-coupling [8]) such that the transconductance of M_1 , g_{m1} , is enhanced to g'_{m1} , as given by

$$g'_{m1} = (1 + A_x)g_{m1} \quad (1)$$

where A_x stands for the voltage transfer of the high-pass network: C_3 and R_1 . The capacitance division between M_1 's C_{GS} and C_3 gives $A_x < 1$.

The capacitive cross-coupling reuses in the nMOS device M_3 to further enhance the overall transconductance G_m as given by

$$G_m = g'_{m1} + A_y g_{m3} \quad (2)$$

where A_y is the voltage transfer of the high-pass network: C_1 and R_3 . R_5 is a grounded resistor. R_5 and C_{OUT} in parallel with the output resistance of M_3 (i.e., r_{o3}), and the resistance

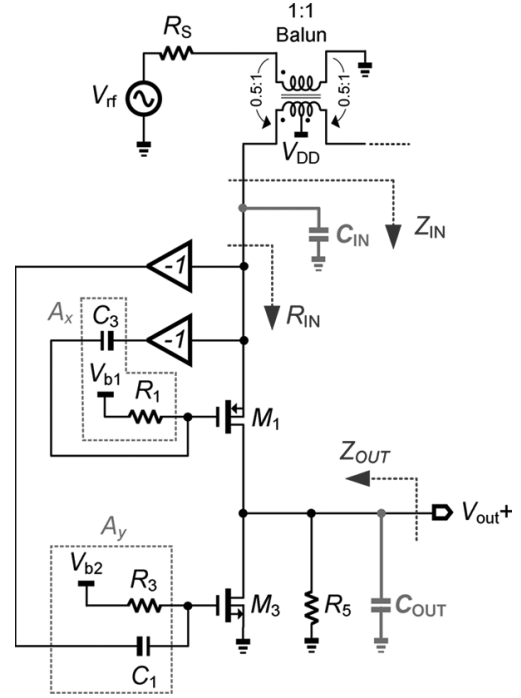


Fig. 6. Single-ended small-signal equivalent circuit of the proposed LNA.

looking into the drain node of M_1 [i.e., $R_{out,M1} = r_{o1} + R_S + g_{m1}r_{o1}(A_x + 1)R_S$], gives the total output impedance Z_{OUT} as

$$Z_{OUT} = R_5 \parallel [r_{o1} + R_S + g_{m1}r_{o1}(A_x + 1)R_S] \parallel r_{o3} \parallel \frac{1}{j\omega C_{OUT}}. \quad (3)$$

Grounded R_5 implemented with a high-resistive polysilicon is to linearize Z_{OUT} and optimize the output common-mode voltage. Since nanoscale transistors suffer from strong channel-length modulation, the conventional $1/g_m$ approximation of the LNA's source-node input impedance leads to poor matching between the calculated and simulated results. An accuracy expression of the resistive input impedance R_{IN} has to count all finite output impedances into account, i.e., r_{o1} of M_1 and r_{o3} of M_3 , yielding

$$R_{IN} = \frac{R_5 \parallel r_{o3} \parallel \frac{1}{j\omega C_{OUT}} + r_{o1}}{1 + g'_{m1}r_{o1}}. \quad (4)$$

R_{IN} in parallel with the input parasitic capacitance C_{IN} gives the input impedance Z_{IN} of the LNA as given by

$$Z_{IN} = R_{IN} \parallel \frac{1}{j\omega C_{IN}}. \quad (5)$$

After all, the differential voltage gain of the LNA, $A_{v,diff}$, can be obtained as

$$A_{v,diff} = \frac{V_{out+} - V_{out-}}{V_{rf}} = \frac{2Z_{IN}}{R_S + 2Z_{IN}} G_m Z_{OUT}. \quad (6)$$

D. Single-Stage Thermal-Noise Cancellation

Noise-cancelling LNAs using a cascading configuration have been reported, e.g., [9], [10]. However, additional amplification stages lead to higher NF and poor linearity. In this study,

thermal-noise cancellation can be achieved in a single stage by taking advantages from the bi-directional coupling behavior of the balun and the structure of the LNA after double-current reuse. Reexamining Fig. 2, we can observe that the thermal noise of M_1 (which can be modeled as a noise current source connecting its drain and source) is partly injected to V_{out+} and partly negatively couples to the source of M_2 through the balun and to the gate of M_2 (M_4) through the cross-coupling network $R_2 - C_4(R_4 - C_2)$. An identical noise coupling operation occurs around M_2 . Differentially, certain noise transfer paths will be out phased from the others, yielding a way to cancel out the noise of M_1 with virtually no cost. Based on R_{IN} (but not Z_{IN} to simplify the noise analysis), it can be shown that the noise factor F of the LNA is given by

$$F = 1 + \frac{\left[\frac{R_S R_{IN}}{R_S + 2R_{IN}} G_m - 1 \right]^2}{\left(\frac{2R_{IN}}{R_S + 2R_{IN}} \right)^2} \frac{g_{m1} \frac{\gamma_1}{\alpha_1} + g_{m3} \frac{\gamma_3}{\alpha_3} + \frac{1}{R_5}}{G_m^2 \frac{R_S}{2}} \quad (7)$$

where α_1 (α_3) and γ_1 (γ_3) are the process- and bias-dependent parameters of M_1 (M_3), respectively. A detailed deduction of (7) is given in the Appendix. Principally, the noise generated by M_1 (M_2) can be minimized by designing

$$\frac{R_S R_{IN}}{R_S + 2R_{IN}} G_m = \frac{R_S R_{IN}}{R_S + 2R_{IN}} (g'_{m1} + A_y g_{m3}) \rightarrow 1. \quad (8)$$

Regrettably, since (6) and (7) are inter-dependent by most parameters, there is no straight way to minimize the overall system NF ($NF = 10 \cdot \log F$) since $A_{v,diff}$ also affects the input-referred noise contribution of the succeeding circuits.

In order to cooptimize the key performance metrics, a constraint-based semi-computed design flow is applied. Given a power budget of 10 mW and a -3 -dB output bandwidth of > 1.7 GHz when driving a 0.3 -pF load (the input capacitance of the polyphase I/Q-mixer scheme), the size of M_1 and R_5 are picked to fulfill the required R_{IN} , which must be close to $R_S/2$ for an acceptable S_{11} (< -10 dB). R_5 is relatively low (250Ω) to desensitize r_{o3} in (5) such that, without affecting the input match, tuning the size of M_3 can trade the $A_{v,diff}$, NF and linearity. Simulation results are plotted in Fig. 7(a) and (b), where the size multiplier (N) of M_3 is swept from 1 to 9. Selecting $N = 5$ yields the highest input-referred third-order intercept point (IIP3) since the third-order derivative of the dc characteristic is close to zero at this N . The corresponding $A_{v,diff}$ is over 20 dB and NF is 2.5 dB. The -3 -dB output bandwidth (1.84 GHz), $|S_{11}|$ (-16.3 dB) and power budget (9.6 mW) are satisfied.

III. KEY PRACTICAL DESIGN ISSUES

A. Package Effect on Input Impedance Match

With the package effect (Fig. 8) taken into account, the single-ended (left-half) input impedance Z'_{IN} of the LNA is given by

$$Z'_{IN} = \frac{1}{j\omega C_{OC}} \left\| \left[j\omega L_{BW} + R_{BW} + \left(R_{IN} \left\| \frac{1}{j\omega C_{IN}} \right\| \right) \right] \right. \quad (9)$$

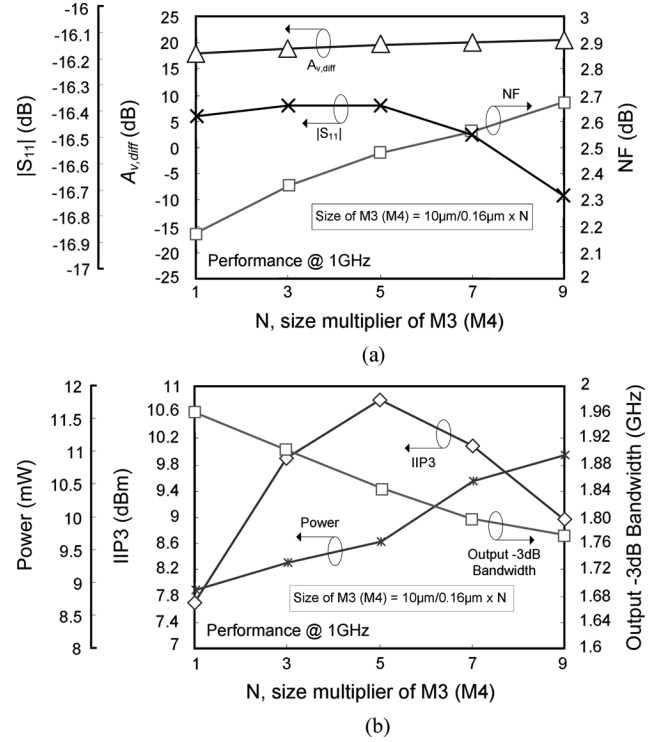


Fig. 7. Size of M_3 (M_4) versus RF performances. (a) $|S_{11}|$, $A_{v,diff}$ and NF . (b) Power consumption, IIP3, and output -3 -dB bandwidth.

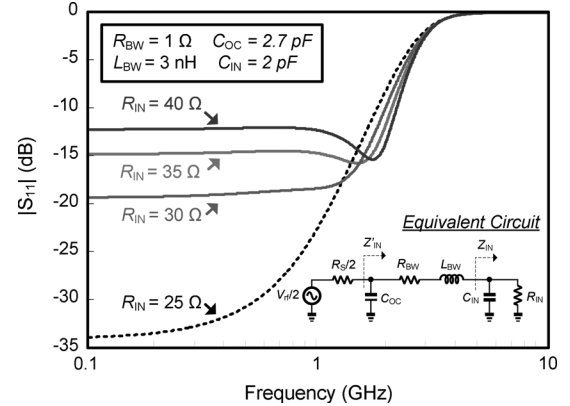
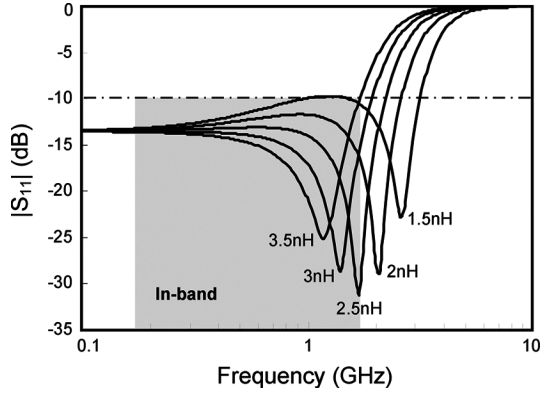
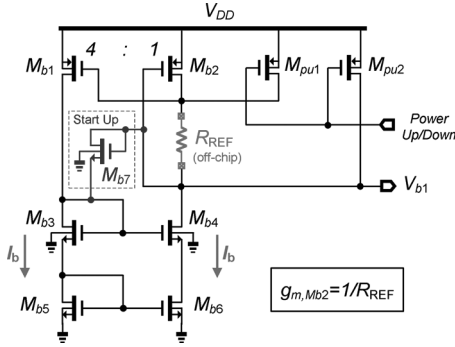


Fig. 8. Input-matching design including package effects.

where C_{OC} denotes the parasitic capacitance of the leadframe and soldering pad on the testing board. L_{BW} and R_{BW} stand for the inductance and resistance of the bondwire, respectively, C_{IN} is the total input capacitance resulting from M_1 , D_N , and D_P , the parasitic capacitance of C_1 and C_3 , and the bondpad (C_{PAD}).

Similar to the analysis addressed in [11], targeting an in-band $|S_{11}| < -10$ dB requires an input reflection coefficient magnitude $|\Gamma_{IN}|$ to satisfy

$$|\Gamma_{IN}| = \left| \frac{Z'_{IN} - \frac{R_S}{2}}{Z'_{IN} + \frac{R_S}{2}} \right| \leq 0.32. \quad (10)$$

Fig. 9. Input matching versus the inductance (L_{BW}) variation of the bondwire.Fig. 10. Self-startup constant- g_m bias circuit (with power up/down control).

With $R_S = 50 \Omega$ and a balun ratio of 1:1, $R_{IN} = 25 \Omega$ achieves a superior $|S_{11}|$. However, the matched bandwidth is insufficient since C_{IN} will lower Z_{IN} when frequency is increasing. Thus, as shown in Fig. 8 as well, the optimal R_{IN} that can result in a broadened bandwidth should be a higher value in practice. Here, R_{IN} between 35–40 Ω gives an adequate $|S_{11}|$ over the desired bandwidth, avoiding any external resonant network.

Since the exact value of L_{BW} is uncertain in practice, the picked R_{IN} must guarantee a $|S_{11}| < -10$ dB over an acceptable range of inductance variation [12]. As shown in Fig. 9, the tolerable L_{BW} variation is from 1.5 to 3.5 nH for $R_{IN} = 40 \Omega$.

B. Self-Startup Constant- g_m Bias Circuit

To tackle the PVT variation, a self-startup constant- g_m bias circuit is adopted. As depicted in Fig. 10, an off-chip resistor R_{REF} serves as the reference, such that $g_{m,Mb2}$ can be fixed to the inverse of R_{REF} by equalizing the dc bias current of M_{b1} and M_{b2} (they exhibit a ratio of 4:1 and are both long-channel devices) [13]. The generated V_{b1} is the bias voltage of the LNAs M_1 and M_2 . R_{REF} is scaled up by 10 \times to reduce the power consumption. Thus, the size ratio of M_{b2} to M_{b1} is set to 1:10 for a correct transconductance ratio.

The self-bias structure requires a start-up circuit. Diode-connected M_{b7} guarantees that the bias circuit can be started up at power-on by satisfying

$$V_{T,Mb5} + V_{T,Mb3} + V_{T,Mb7} + |V_{T,Mb2}| < V_{DD} \quad (11)$$

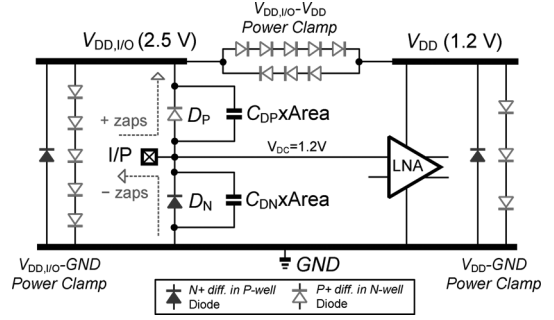


Fig. 11. Mixed-voltage ESD-protection scheme.

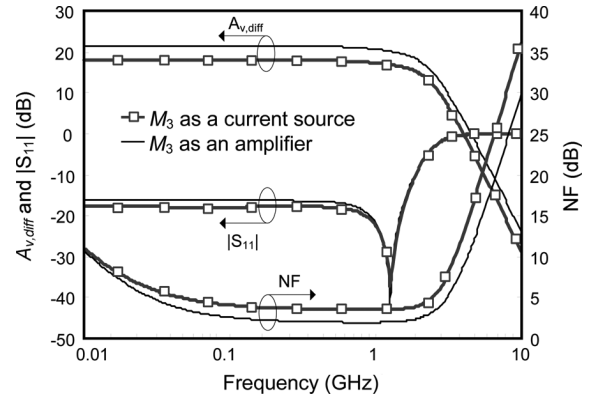
and shut down afterwards by satisfying

$$V_{GS,Mb5} + V_{GS,Mb3} + V_{T,Mb7} + |V_{GS,Mb2}| > V_{DD} \quad (12)$$

where V_T is the threshold voltage of the transistor.

TABLE II
DEVICE DIMENSION

Device	Size	Device	Size
M_1, M_2	(10 $\mu\text{m}/0.08\mu\text{m}$) \times 10	R_{REF}	400 Ω
M_3, M_4	(10 $\mu\text{m}/0.08\mu\text{m}$) \times 5	M_{b1}	(10 $\mu\text{m}/0.08\mu\text{m}$) \times 4
R_1 – R_4	1 μm \times 40 μm = 40k Ω	M_{b2}	(10 $\mu\text{m}/0.08\mu\text{m}$) \times 1
C_1 – C_4	1 μm \times 40 μm = 2.7pF	M_{b3} – M_{b7}	(1 $\mu\text{m}/0.32\mu\text{m}$) \times 8
R_5, R_6	10 μm \times 3 μm = 250 Ω	D_P, D_N	(1 $\mu\text{m}/50\mu\text{m}$) \times 10

Fig. 12. RF performance comparison of using M_3 as a current source (i.e., only capacitive cross coupling of M_1) or as an amplifier (double-current reuse).

C. Power-Up/Down Control With Reliability Concern

Nanoscale circuits for mobile TV require particular attention of reliability in power-down condition since DVB-H uses time-slicing operation. In the employed 90-nm CMOS process, the proposed LNA operating at 1.2 V is free from hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB), and absolute maximum rating (AMR). The primary concern is the negative bias temperature instability (NBTI) of all pMOS devices. To prevent large V_{GS} or V_{GD} in power-down mode, M_{b1} and M_{b2} in the self-startup constant- g_m bias circuit (Fig. 9) are pulled up to V_{DD} . In this way, the NBTI stress is transferred to the pull-up switches, M_{pu1} and M_{pu2} , which show no impact

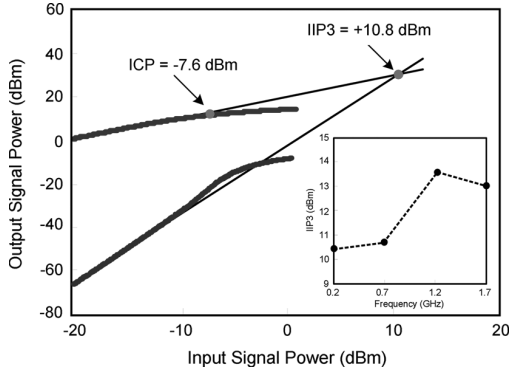
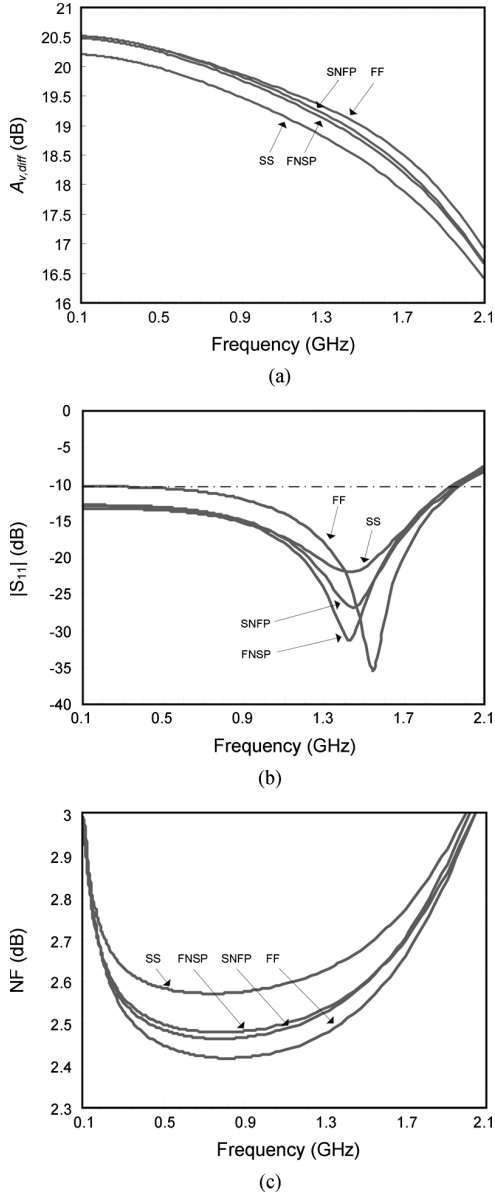


Fig. 13. Two-tone tests at 695 and 700 MHz.

Fig. 14. RF performance in process corners: FAST-FAST (FF), SLOW-SLOW (SS), FAST-NMOS-SLOW-PMOS (FNFP) and SLOW-NMOS-FAST-PMOS (SNFP). (a) $A_{v,diff}$, (b) $|S_{11}|$, and (c) NF.

to the LNA in active mode. This technique simultaneously pulls up V_{b1} to V_{DD} , guaranteeing M_1 and M_2 of the LNA are also shut down in the same manner.

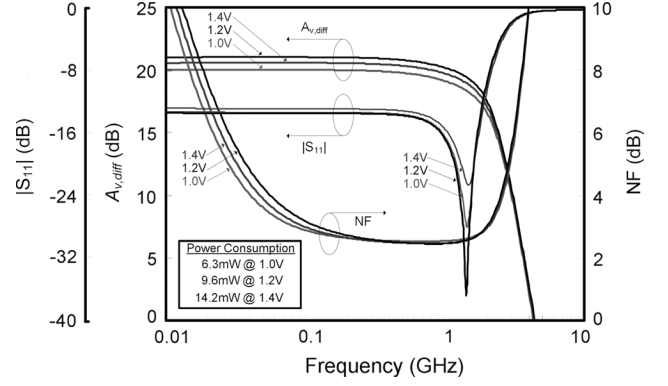


Fig. 15. RF performances versus supply voltage variation.

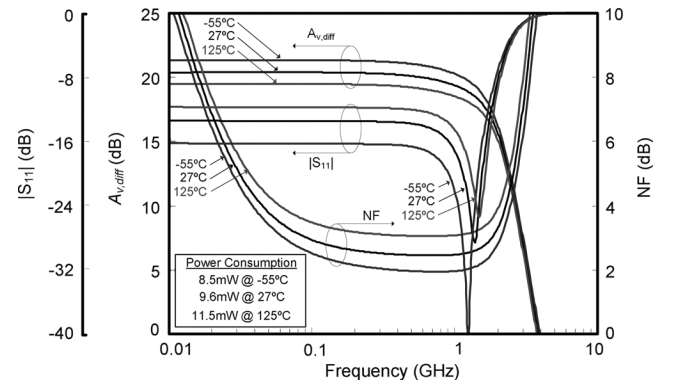


Fig. 16. RF performances versus temperature variation.

D. Mixed-Voltage ESD Protection Scheme

Protecting the nanoscale thin-oxide devices from ESD events requires well-designed discharge paths to the supply rails. Fig. 11 shows the designed mixed-voltage ESD clamps. Power clamps based on p+/n-well diode chains efficiently realize a sufficient high-trigger voltage that is greater than the supply, such that the leakage current and the chance of accidental latching due to normal supply fluctuation are minimized. For instance, with a silicon diode threshold voltage of ~ 0.65 V, the $V_{DD,I/O}$ -GND power clamp needs five diodes in series, whereas for V_{DD} -GND only three are necessary. The selected number of diodes in the $V_{DD,I/O} - V_{DD}$ power clamp have had the precaution of different supply start-up sequences. For instance, $V_{DD,I/O}$ may start before V_{DD} . The proposed scheme is optimized to avoid the happening of any forward-bias current in all supply start-up sequences.

The dimension of $D_P(D_N)$ is $1 \mu\text{m}/501 \mu\text{m} \times 10$. Since the technology determines that the parasitic capacitances resulting from D_P and D_N per unit area are $C_{DP} = 0.9 \text{ fF}/\mu\text{m}^2$ and $C_{DN} = 0.74 \text{ fF}/\mu\text{m}^2$, respectively, the imposed total parasitic capacitance at the input is $\sim 870 \text{ fF}$, which occupies 44% of the total C_{IN} budget. The remaining C_{IN} budget can be reserved for the C_{PAD} ($\sim 300 \text{ fF}$), the input parasitic capacitance of M_1 , and the parasitic capacitances of C_2 , C_4 , and C_5 , which are all metal-over-metal (MoM) capacitors.

TABLE III
BRIEF PERFORMANCE COMPARISON OF RECENTLY PUBLISHED WIDEBAND LNAs

Ref - Year	Technology	Bandwidth (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Supply (V)	Power (mW)	No. of inductors	ESD protection
[15] & This work ^S	90nm CMOS	0.1 ~ 1.89	20.6 ^{VG}	<2.7	+10.8 @ 0.7 GHz	1.2 [*]	9.6	0	± 4 kV
[16] JSSC'08 ^M	65nm CMOS	0.2 ~ 5.2	13 -15.6 ^{VG}	<3.5	> 0	1.2	21	0	No
[17] JSSC'08 ^M	130nm CMOS	0.8 ~ 2.1	14.5 ^{VG}	2.6	+16	1.5	17.4	0	No
[18] ASSCC'07 ^M	180nm CMOS	0.05 -0.86	15 ^{VG}	2.5	+ 8.3	1.8	7.2	0	No
[19] RFIC'07 ^m	90nm CMOS	0.4 ~ 1	16 ^{PG}	<5.3	-17 @ 1 GHz	1.2	16.8	0	No
[20] TCAS-II'07 ^S	130nm CMOS	0.2 ~ 3.8	11.2 ^{VG}	<2.85	-2.7 @ 3 GHz	1.2	1.9	0	No
[20] TCAS-II'07 ^S	130nm CMOS	0.2 ~ 6.2	10.5 ^{VG}	<2.85	-2.7 @ 3 GHz	1.2	1.9	2	No
[21] TCAS-I'07 ^M	180nm CMOS	2.8 ~7.2	19.1 ^{PG}	<3.8	-1 @ 6 GHz	1.8	32	7	No
[22] PRIME'06 ^S	130nm CMOS	0.9 ~ 2.5	17 ^{PG}	2	-5	1.2	15.6	4	No
[23] RFIC'05 ^M	130nm CMOS	0.1 ~ 0.93	13 ^{PG}	4	-10.2	1.2	0.72	0	No
[24] CICC'05 ^M	130nm CMOS	0.1 ~ 6.5	19 ^{PG}	<4.2	+1	1.8	11.7	4	No
[25] ESSCIRC'05 ^M	130nm CMOS	3 ~ 5	26 ^{VG}	4	-13	1.5	45	4	± 1.5 kV
[26] ISCAS'05 ^S	130nm CMOS	3 ~ 10.7	11 ^{PG}	3	-8.2	1.2	4.8	5	No
[27] ASSCC'05 ^M	180nm CMOS	0.04 ~ 0.9	20.3 ^{PG}	4	-10.8 ~ -12.7	1.8	43.2	0	No
[28] ISCAS'05 ^S	180nm CMOS	1.5 ~ 2.6	15.4 ^{PG}	0.9	-2.5	1.5	11	4	No
[28] ISCAS'05 ^S	180nm CMOS	3.2 ~ 4.8	17.9 ^{PG}	1.6	-4.5	1.5	13.2	4	No
[29] JSSC'05 ^M	180nm CMOS	2 ~ 4.6	9.8 ^{PG}	<5.2	-7	1.8	12.6	3	No
[30] TCAS-I'05 ^M	250nm CMOS	3.2 ~ 4.8	7 ^{PG}	<3.7	4 @ 4GHz	2.5	20	2	No
[31] ISSCC'04 ^M	180nm CMOS	2.3 ~ 9.2	9.3 ^{PG}	5.2	-6.7	1.8	9	5	No
[31] ISSCC'04 ^M	180nm CMOS	2.4 ~ 9.5	10.4 ^{PG}	5.3	-8.8	1.8	9	5	No
[32] MWSCAS'03 ^S	180nm CMOS	3 ~ 7	15.3 ^{PG}	<1.9	N/A	1.8	15	4	No

S: simulation results M: measurement results *: 2.5 V for ESD protection diode PG: power gain VG: voltage gain

IV. SIMULATION RESULTS, DISCUSSIONS, AND BENCHMARKS

The LNA has been extensively characterized in *Cadence* environment with SPECTRE as the simulator. The device dimensions are listed in Table II. The package effects and parasitic capacitances at the input and output nodes have been modeled in all simulations. An extra load capacitor of 0.3 pF is added to account for the input capacitance of the succeeding polyphase I/Q-mixer scheme. The ESD robustness of the RF-input pins to rail is tested using the Human Body Model (HBM) reference circuit [14]. A \pm HBM voltage pulse is applied to the LNA's input to induce a large \pm zapping discharge current that has a rising/falling time of ~ 8 ns. Verified in all combinations, the LNA can withstand minimally ± 4 kV of ESD zapping without causing internal or protection devices failure. This result fulfills the standard of "safe level" (i.e., ± 4 kV) in the chip-level ESD specifications.

It would be interesting to compare the effectiveness of the double-current reuse technique to the simple capacitive cross coupling. As shown in Fig. 12, with M_3 serving as an amplification device, there are roughly 1-dB and 3-dB improvements in terms of NF and $A_{v,diff}$, respectively.

Multiband reception of mobile-TV standards does not pose rigid group-delay variation specification as the bandwidth usage of each standard is relatively small in comparing with that of the LNA. The simulated inband gain delay is 233 ± 21 ps.

The in-band linearity is verified by two-tone tests as shown in Fig. 13. Thank to the cascode-free structure of the LNA and optimal gate-source voltage biasing, high IIP3 of +10.8 dBm and -1-dB input-referred compression point (ICP) of -7.6 dBm are concurrently achieved. Other IIP3s among the desired signal band varies between +10.5 to +13.7 dBm. An out-of-band two-tone test at 2.0 and 2.1 GHz is also conducted (not shown), obtaining an out-of-band IIP3 of +9.9 dBm and a -1-dB ICP of -3.5 dBm. Both demonstrate superior linearity performance metrics in this 1.2-V 9.6-mW LNA design. The power-down leakage is 47 μ W.

The effects of differential imbalance to the performances of the LNA are simulated. A 10% size mismatch between M_1 and M_2 still maintain the in-band common-mode and supply rejection ratios > 50 dB. Since the LNA is intended to drive an integrated mixer, testing the reverse isolation S_{12} necessitating using a 50- Ω test buffer cannot tell the stability information of the LNA in its true operating condition. Thus, only the reverse voltage gain (i.e., the differential outputs coupled back to the input node) and transient simulation results can help to estimate the stability of the LNA. The simulated in-band reverse voltage gain is < -28 dB. The tolerable C_L is up to 1 pF without affecting the targeted $|S_{11}|$ of -10 dB. These tests give confidence that the LNA will be stable in practice.

As the impact of transistor variability in nanoscale process is continuously increasing, process corner and Monte Carlo (MC) simulations are essential to investigate the robustness of the

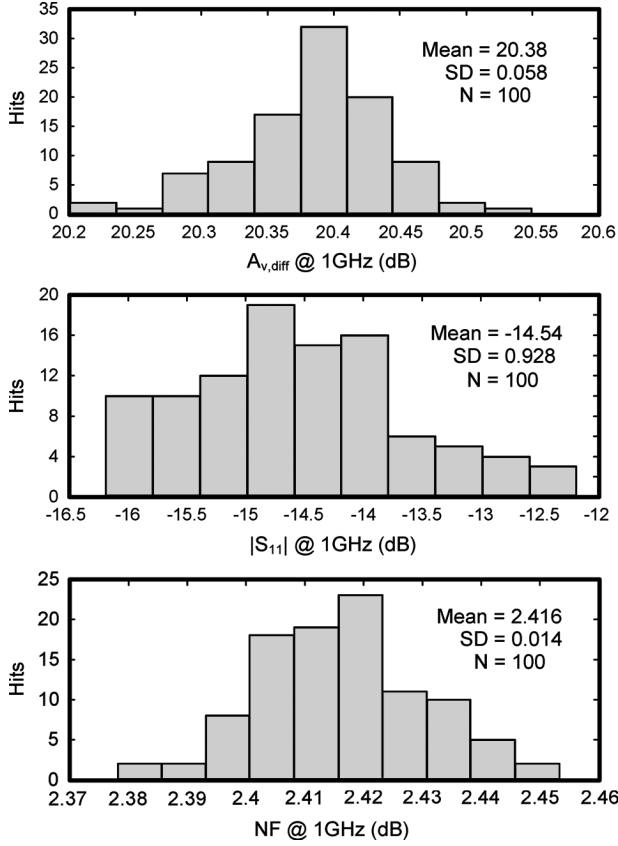


Fig. 17. 100-time MC simulation results of the RF performances.

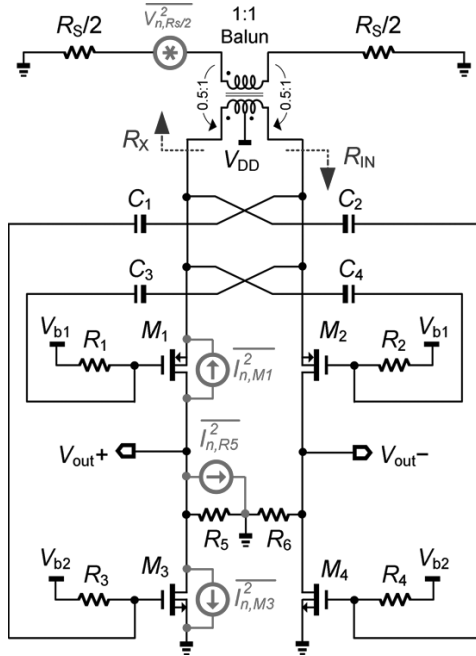


Fig. 18. Noise model of the proposed LNA.

RF performances over PVT. A set of simulation counting the process (Fig. 14), supply voltage (Fig. 15), and temperature (Fig. 16) variations have been conducted. In addition, a set of 100-time MC simulation of the RF performances was done

(Fig. 17). These presilicon results rigidly verify the effectiveness of the proposed circuit techniques and the completeness of the design consideration. The LNA will be experimentally verified with the entire TV tuner.

Table III gives a comparison of the proposed LNA with respect to the recently published wideband CMOS LNAs [15]–[32] (design with both simulation and measurement results are considered). It can be observed that most performance metrics of the current design are superior, in particular the voltage gain, power and linearity, even under high ESD protection.

V. CONCLUSION

An ESD-protected UWB LNA covering 170 to 1700 MHz for full-band mobile TV tuners in a 90-nm CMOS process has been described. ± 4 -kV ESD robustness at the RF input pins and +10.8-dBm IIP3 have been concurrently achieved by exploiting a 1.2/2.5-V-mixed ESD protection scheme and a pMOS-based open-source input structure. Reliability- and PVT-conscious bias techniques lead to competitive and robust RF performances. The LNA core employed double-current reuse and single-stage thermal-noise cancellation achieves 20.6-dB voltage gain and <2.7-dB NF with 9.6-mW power consumption.

APPENDIX

The noise factor F of the proposed LNA is calculated by considering first the noise model of the key devices, as shown in Fig. 18. Due to differential symmetry, separating R_S into two $R_S/2$ resistors and calculating the left-half circuit is sufficient as the noise contribution of M_1 , M_3 , and R_5 are equal to that of M_2 , M_4 , and R_6 , respectively. The four sources of noise, $R_S/2$, M_3 , R_5 , and M_1 , are given by

$$\overline{V_{n,Rs/2}^2} = 4KT \frac{R_S}{2} \quad (A1)$$

$$\overline{I_{n,M3}^2} = 4KT g_{m3} \frac{\gamma_3}{\alpha_3} \quad (A2)$$

$$\overline{I_{n,R5}^2} = \frac{4KT}{R_5} \quad (A3)$$

$$\overline{I_{n,M1}^2} = 4KT g_{m1} \frac{\gamma_1}{\alpha_1}. \quad (A4)$$

Second, the principle of superposition will be applied to calculate the differential output squared noise current due to each noise source, yielding

$$I_{n,Rs/2,diffout}^2 = \left| \frac{2R_{IN}}{R_S + 2R_{IN}} \frac{4R_{IN}}{R_S + 2R_{IN}} G_m V_{n,Rs/2} \right|^2 \quad (A5)$$

$$I_{n,M3,diffout}^2 = |I_{n,M3}|^2 \quad (A6)$$

$$I_{n,R5,diffout}^2 = |I_{n,R5}|^2 \quad (A7)$$

$$I_{n,M1,diffout}^2 = \left| \left(\frac{2R_X R_{IN}}{R_X + R_{IN}} G_m - 1 \right) I_{n,M1} \right|^2. \quad (A8)$$

R_X in (A8) represents the impedance observing from the LNA's input back to the balun as given by

$$R_X = \left[\left(\frac{2}{1} \right)^2 R_{IN} \parallel \left(\frac{R_S}{2} + \frac{R_S}{2} \right) \right] \left(\frac{1}{2} \right)^2 = \frac{R_S R_{IN}}{R_S + 4R_{IN}}. \quad (A9)$$

Finally, F in (7) is obtained by dividing the total output noise power by the noise power of $R_S/2$ as given by

$$F = 1 + \frac{I_{n,M1,diffout}^2 + I_{n,M3,diffout}^2 + I_{n,R5,diffout}^2}{I_{n,Rs/2,diffout}^2}. \quad (A10)$$

Theoretically, for a perfectly matched input impedance (i.e., $R_S = 2R_{IN}$) and ideal cross-coupling networks ($A_x = A_y = 1$), the noise contribution of M_1 can be fully cancelled in a single stage by setting $g_{m3} = 2g_{m1}$, recalling that $G_m = (1 + A_x)g_{m1} + A_y g_{m3}$.

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Pui-In Mak (S'00–M'08) received the B.Sc. and Ph.D. degrees in electrical and electronics engineering from the University of Macau (UM), Macao, China, in 2003 and 2006, respectively.

He was with Chipidea Microelectronics Ltd., Macau, in 2003. Since 2004, he has been with the Analog and Mixed-Signal VLSI Laboratory at UM, where he was a Research and Teaching Assistant (2004–2006), Invited Research Fellow (2006–2007), and (Co-)Coordinator of the Wireless (Biomedical) Research Lines (2008–). He is currently an Assistant Professor with UM. His current research interests are on wireless and biomedical circuits and systems, and engineering education. He authored a book, *Analog-Baseband Architectures and Circuits for Multistandard and Low-Voltage Wireless Transceivers* (Springer, 2007), and over 40 articles in IEEE/IET journals and conferences. He has one U.S. patent pending and several more in applications.

Dr. Mak was the corecipient of the 2003 ASICON Student Paper Award, the 2004 MWSCAS Student Paper Award, the 2004 IEEJ International Analog VLSI Workshop Best Paper Award, the 2005 PRIME Silver Leaf Certificate, the 2005 DAC/ISSCC Design Contest Award, and the 2008 APCCAS Merit Student Paper Certificate. He received the 2009 Clare-Hall Visiting Fellowship from the University of Cambridge, U.K. He was the first student of UM to be decorated by the Macao Government in 2005 with the Honorary Title of Value. He is with the Technical Committee CASCOS of the IEEE Circuits and Systems Society (CASS) and the Technical Program/Review/Organization Committee of AVLSIWS'04, APCCAS'08, ICCS'08, ICICS'09, ISCAS'09, PrimeAsia'09, and ISCAS'10. He is the Tutorial Co-Chair of APCCAS'08. He is the Region-10 GOLD Representative (2007–) and Member (2009–2011) of the IEEE CASS Board-of-Governors. He is the Co-Organizer of the GOLD/Technology Management Special Session in ISCAS'09. He was the Secretary of Macau CAS/COM Joint Chapter (2005–2008) (nominated for the 2009 CASS World Chapter-of-the-Year Award).



Rui Martins (M'88–SM'99–F'08) was born on April 30, 1957. He received the B.S., M.S., and Ph.D. degrees and the *Habilitation* for Full-Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), Technical University of Lisbon (TUL), Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

Since 1992, he has been on leave from IST, TUL, and is also with the Electrical and Electronics Engineering Department, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he has been a Full Professor since 1998. At FST, he was the Dean of the Faculty from 1994 to 1997 and he has been the Vice-Rector (Research) of UM since 1997. Since September 2008, after the reform of the UM Charter, he was nominated after open international recruitment as Vice-Rector (Research) until August 31, 2013. Within the scope of his teaching and research activity, he has taught 20 bachelor and master's courses and has supervised 21 theses (nine Ph.D. and 12 master's). He has published 13 books, coauthoring three and coediting 10, plus five book chapters, 160 refereed papers (29 in scientific journals and 131 in conference proceedings), as well as 70 other academic works, totalling 246 publications, in the areas of microelectronics, electrical and electronics engineering, engineering, and university education. He has coauthored seven submitted U.S. patents (one approved and issued in 2009, one classified as patent pending, and five still in the process of application). He has founded the Analog and Mixed-Signal VLSI Research Laboratory of UM (http://www.fst.umac.mo/en/lab/ans_vlsi/).

Prof. Martins was the Founding Chairman of the IEEE Macau Section from 2003 to 2005 and of the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications (COM) from 2005 to 2008 [nominated for the World Chapter of the Year 2009 from the IEEE Circuits and Systems Society (CASS)]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on Circuits and Systems—APCCAS 2008 and was elected Vice-President for Region 10 (Asia, Australia, and the Pacific) of the IEEE CASS for 2009–2010. He was the recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999 and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001.