A 5.1-to-7.3 mW, 2.4-to-5 GHz Class-C Mode-Switching Single-Ended-Complementary VCO Achieving >190 dBc/Hz FoM

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***Abstract*—This brief reports a class-C mode-switching single-ended-complementary (MS-SEC) VCO for wideband operation. Unlike the existing wideband VCOs that utilize nMOS-only $-g_m$ transistors operating in the class-B mode to maximize the oscillation amplitude, our MS-SEC VCO combines the advantages of class-C mode, which delivers a tall current pulse, together with current-reuse to maximize the current efficiency while lowering the phase noise (PN). The $-g_m$ transistors are preserved within the saturation region to avoid the inherent trade-off between PN and power consumption for a wideband VCO, as well as the reliability concerns. The VCO prototyped in 130-nm CMOS occupies a die area of 0.33 mm^2 and consumes 5.1-to-7.3 mW at 1.2 V, while covering 2.4-to-5 GHz and meeting the stringent PN specification of the GSM standard with no SAW filter. The results correspond to a figure-of-merit of >190 dBc/Hz throughout the tuning range.**

***Index Terms*—Mode switching, CMOS, class-C, current-reuse, voltage-controlled oscillator (VCO), phase noise (PN), single-ended complementary (SEC), wideband.**

I. Introduction

THE DESIGN of voltage controlled oscillators (VCOs) with a wide tuning range (TR) and low power consumption, while meeting the stringent phase noise (PN) specifications of modern wireless standards, is a challenging task, yet its successful implementation is a critical enabler of realizing the low-cost low-power software-defined radios (SDRs) [1], [2].

Dual-core VCOs are found suitable for wideband operation. With the 8-shaped inductors [3], the magnetic pulling between the VCOs and other blocks is alleviated, but at the cost of a deteriorated Q factor. Recent works in the core mode-switching (MS) technique proves effective in facilitating the trade-off between TR and PN [4]–[6]. Specifically, in [4], using a PMOS cross-coupled pair results in current leakage for the mode switches. In [5], as a very low and non-standard supply is used, an extra supply regulator is essential for high supply-rejection ratio. For [6], 2 and 4 cross-shaped inductors connected in parallel are tried, but this could take up large amount of chip area. Nevertheless, the aforesaid techniques share a similarity: they are all operated in the class-B mode (Fig. 1), which heavily relies on a large oscillation amplitude to improve the PN, but consuming substantial amount of power. Moreover, if the oscillation amplitude is as large as V_{DD}, it could drive the $-g_m$ transistors into the deep triode region. Its low on-resistance (R_{ON}) penalizes the Q of the LC tank, so as the PN.

This brief reports a Class-C mode-switching single-ended-complementary (MS-SEC) VCO realized in 130-nm CMOS. It achieves a constantly high FoM of >190 dBc/Hz across >70% TR, while dissipating <9 mW of power. The key techniques are: 1) to split a complementary cross-coupled $-g_m$ pair into two single-ended ones, thus reusing the current from V_{DD} to ground through both PMOS and NMOS, and 2) to enforce the MS-SEC VCO in the class-C mode to further enhance the DC-to-RF conversion efficiency, while lowering the noise contribution of the $-g_m$ transistors.

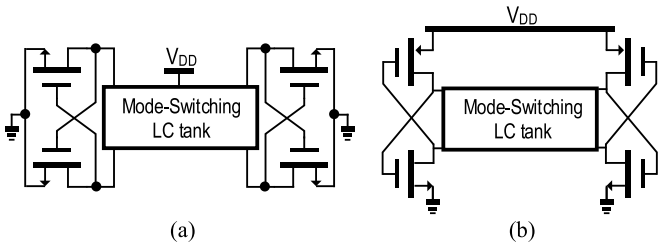

Fig. 1. Conceptual diagram of a wideband VCO with (a) NMOS-only $-g_m$ transistors, and (b) single-ended-complementary $-g_m$ transistors (right).

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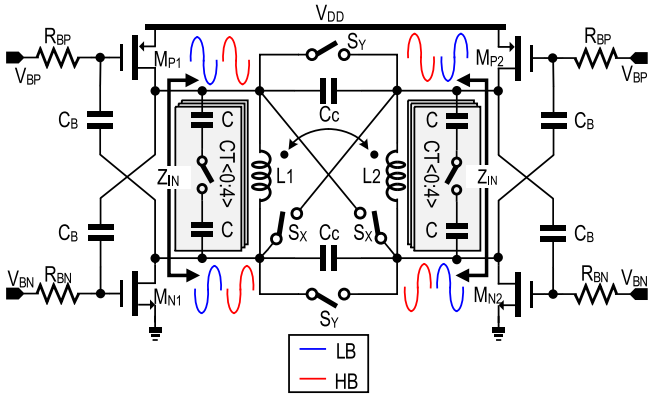

Fig. 2. Proposed Class-C MS-SEC VCO.

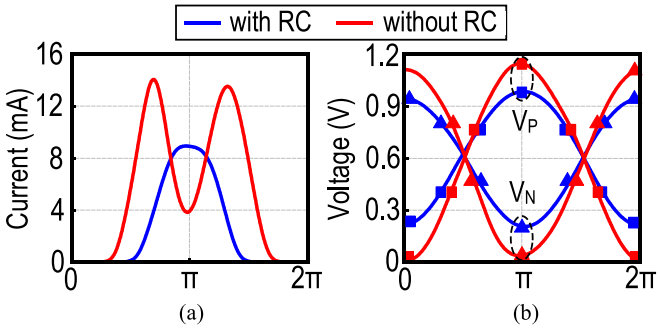

Fig. 3. Comparison of (a) Current, and (b) voltage waveform with and without RC network.

II. Design of a Wideband Class-C MS-SEC VCO

A. Circuit Topology

Fig. 2 depicts the proposed Class-C MS-SEC VCO. The tank is a symmetric 4th-order system, with a pair of equivalent LC resonators coupled both inductively and capacitively (via C_C). They can be switched by the NMOS switches S_X and S_Y. For the input impedance of the resonator looking at either side, its exact expression is shown in (1), as shown at the bottom of the next page, where L is the inductance of the two coils (L_1 and L_2), assuming $L_1 = L_2 = L$ and k_m is the coupling coefficient of the two inductors. When S_X is switched on and S_Y is off, C_C loads the LC tank as they see a differential voltage drop and the transformer is coupled positively, resulting in a low band (LB) frequency $f_{LB} = 1/2\pi\sqrt{(C + C_C)(L + M)}$ where $M = k_m L$ is the mutual inductance. Conversely, when S_Y is switched on and S_X is off, C_C observes a 0 voltage drop, and the transformer is coupled negatively, resulting in a high band (HB) frequency $f_{HB} = 1/2\pi\sqrt{C(L - M)}$. The loss of the resonator is compensated by stacking PMOS and NMOS transistors, thus reusing the current from V_{DD} to ground across a period. To further increase the current efficiency, we insert an additional RC network between the gate and drain, forcing the VCO cores to operate in the class-C mode by delivering a tall current pulse as shown in Fig. 3(a).

B. Design Considerations of the RC Network

To investigate the design trade-off of the RC network, let us consider the single-sided small-signal model shown in Fig. 4. To ensure an adequate loop gain for startup, the RC time constant has to satisfy $-A_v g_m/2 \cdot (R_{EF} \parallel R_P) > 1$, where A_v is the gain of the transistor from the drain to gate nodes, assuming $A_{v,n} = A_{v,p} = A_v$ where $A_{v,n} = v_{gn}/v_n$ and $A_{v,p} = v_{gp}/v_p$, $v_{n(p)}$ and $v_{gn(p)}$ are the voltage at drain and gate of NMOS (PMOS) respectively. A_v is given by

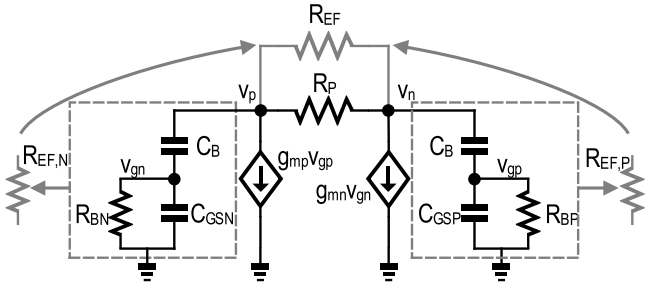

Fig. 4. Small-signal equivalent model of the MS-SEC VCO.

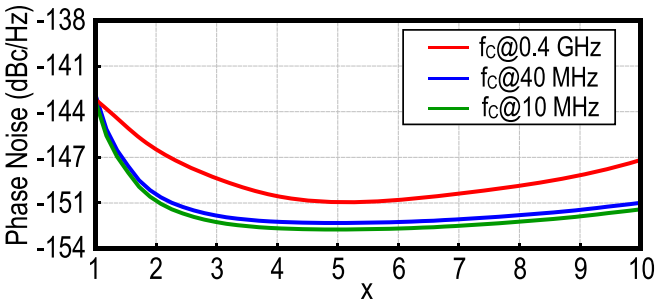

Fig. 5. Simulated PN against x factor of the RC network for different cutoff frequency f_C.

$$A_v = \frac{1}{\frac{C_{GSN(P)}}{C_B} + 1 + \frac{1}{\omega R_{BN(P)} C_B}} \tag{2}$$

where $C_{GSN(P)}$ models all the parasitic capacitance of the switched capacitors, -g_m transistors and a test buffer (as output load). R_{EF} is the equivalent resistance due to $R_{BN}C_B$ and $R_{BP}C_B$. We also can have $g_{mp} = g_{mn} = g_m$ by sizing the transistor properly. Assuming $R_{EF} = R_{EF,n} + R_{EF,p}$, this results in $R_{EF} \approx 2R_{BN(P)}[(2C_{GSN(P)}/C_B) + 1]$. Since the RC network acts as a high-pass filter, its cutoff frequency $f_C << f_{MIN}$ is required as obvious from (2). To gain more insight, we let $C_B = 0.4x$ pF and $R_B = 10/x$ kΩ so that $f_C = 40$ MHz (well below f_{MIN}), and we sweep the x factor when the VCO is oscillating at $f_{MIN} = 2.4$ GHz as revealed in Fig. 5. When x is small, a large R_B contributes more the thermal noise, and a small C_B reduces the coupling capability, penalizing the oscillation amplitude and thereby PN. Conversely, a small R_B loads down the Q of the LC tank, calling for a large C_B which could contribute with parasitic capacitance to the gate and drain of the $-g_m$ transistors. To balance the performance, we select $x = 4$ to yield $R_B = 2.2$ kΩ and $C_B = 1.6$ pF. When considering area constraint, first, if $f_C = 10$ MHz, there is only a negligible improvement in PN. Second, to make the design more robust, a common-mode (CM) feedback operational amplifier [7] followed by a large RC filter with low f_C in the range of Hz are required, which is not feasible in practical design.

C. Core Mismatches

The proposed MS-SEC VCO can be viewed as 2 separated VCO cores coupled and injection-locked together [8]. Since C_C and M are relatively fixed to ensure $f_{MAX,LB}$ and $f_{MIN,HB}$ are overlapped with margin, the core coupling strength is also determined by the mode switches S_X and S_Y. Besides, they

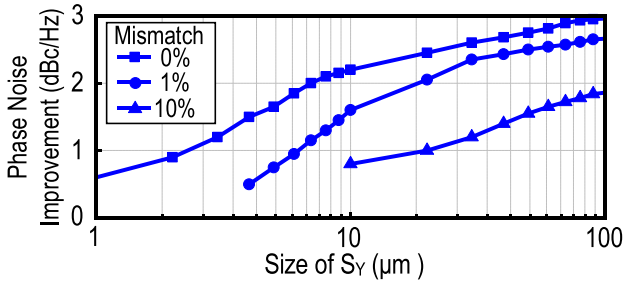

Fig. 6. Effect of the size of S_Y on the PN improvement for different core mismatches.

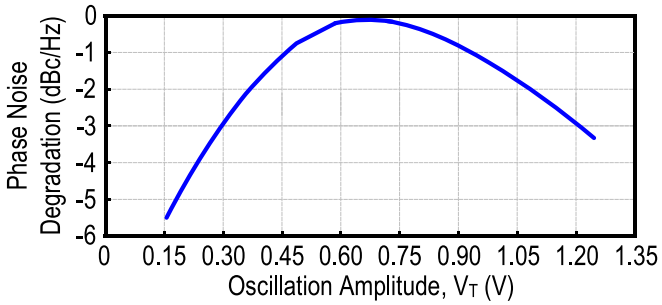

Fig. 7. Simulated PN against the amplitude across the tank V_T at 5 GHz.

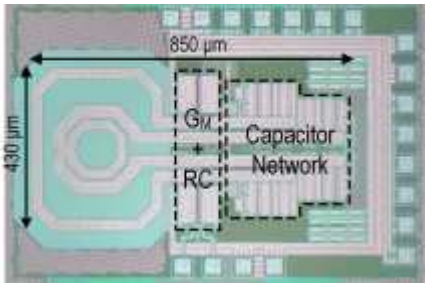

Fig. 8. Chip photo of the fabricated MS-SEC VCO in 130-nm CMOS.

induce no loss to the resonator because they sustain a CM voltage when their corresponding mode is enabled. As stated in [9], the coupling impedance Z_C should be minimized to achieve maximum PN reduction, and to suppress the undesired oscillation modes by the mutual inductance M, coupling capacitor C_C and conductance of the mode switches G_X and G_Y. Specifically, when LB is enabled,

$$Z_{C,LB} = j2\pi f \cdot \frac{L(L+M)}{M} \parallel \frac{C+C_C}{j2\pi f C C_C} \parallel \frac{1}{G_X} \tag{3}$$

On the other hand, when HB is enabled,

$$Z_{C,HB} = j2\pi f \cdot \frac{L^2-M^2}{M^2} \parallel \frac{1}{j2\pi f C} \parallel \frac{1}{G_Y} \tag{4}$$

As suggested by (3) and (4), S_Y requires a bigger switch to reduce the coupling impedance in the HB mode. For 0% mismatch between the two cores, simulation reveals that the minimum $R_{ON,Y}$ is 1.49 kΩ for a 0.6-dB PN improvement. The PN improves to 2.9 dB if S_Y are sized such that $R_{ON,Y}$ is less than 70 Ω, but at the cost of enlarged parasitic capacitance limiting the TR.

In fact, any mismatch between the two VCO cores can cause their respective resonant frequency to vary, leading to injection pulling and thus producing undesirable spurs [8]. As such, the coupling strength has to be increased by oversizing the switches to compensate for the core mismatch. As shown in Fig. 6, the minimum size required for S_Y in locking condition for 0%, 1% and 10% mismatches in the tank capacitor C is 1, 4.6 and 10 μm, respectively. Even for 1% mismatch, the PN improvement still attains a value as high as 2.3 dB for 35 μm.

D. Maximum Oscillation Amplitude

Following the analysis in [10], if the oscillation amplitude is large enough to drive both PMOS and NMOS transistors into the triode region, the PN performance degrades significantly due to the presence of single-ended parasitic capacitance, and low R_{ON} of the transistors appearing in parallel with the LC tank, thus degrading the tank's Q. Besides that, amplitude imbalance becomes severe due to the inherent sensitivity of the topology to the peak dynamic current. In the worst case, a voltage drop may appear across C_C, partially loading the tank and adding losses to the switches S_Y when they are on (HB mode), offsetting the benefits of the MS technique. Thus, it is necessary to ensure that the transistors are kept within the saturation region when they are conducting simultaneously, preventing the single-ended capacitors from being discharged via the PMOS.

To estimate the maximum oscillation amplitude at the drain of the transistors, we consider HB for M_{N1} and M_{P1} as shown in Fig. 2. For the saturation condition, both PMOS and NMOS have to satisfy $V_{D,p} \le V_{G,p} - V_{TH,p}$ and $V_{D,n} \ge V_{G,n} - V_{TH,n}$ respectively, leading to

$$\frac{V_T}{2} \le \frac{V_{BP} - V_{CM} + V_{TH,p}}{1 + A_{V,p}} \tag{5}$$

$$\frac{V_T}{2} \le \frac{-V_{BN} + V_{CM} + V_{TH,n}}{1 + A_{V,n}} \tag{6}$$

where V_T is the differential oscillation voltage across the tank, V_{CM} is the drain DC common-mode voltage. Hence, the bias voltage at the gate V_{BP} (V_{BN}) should be set higher (lower) than V_{CM} to allow a reasonable voltage swing, while ensuring the transistors do not enter the triode region [11]. From simulations, as shown in Fig. 7, an excessive V_T(> 1.1 V) is undesired as it will degrade the PN by 3 dB at the highest frequency f_{max}. The voltage waveform is shown in Fig. 3(b).

E. Phase Noise (PN)

Using the linear time-variant model [12], the PN of a LC oscillator at an offset frequency Δf from the oscillation

$$Z_{IN} = \frac{sLR_P[s^2L(1+k_m)R_P(C+C_C) + sL(1+k_m) + R_P]}{s^4L^2(1+k_m)^2R_P^2(C+C_C)^2 + s^3L^2(1+k_m)^2R_P(2C_C+2C-R_PC_C) + s^2L(1+k_m)[2R_P^2(C+C_C)+L(1+k_m)] + s2L(1+k_m)R_P + R_P^2} \tag{1}$$

TABLE I
NOISE FACTOR COMPARISON BETWEEN NMOS-ONLY CLASS-B AND CLASS-C MS-SEC VCO

	MS-Class-B VCO	MS-SEC VCO
F_T	0.5	0.5
F_{GM}	0.89	0.64
F_{GDS}	0.27	0.019
$\sum F$ (dB)	2.2	0.64

frequency f_o can be expressed as

$$L(\Delta f) = 10\log_{10}\left(\frac{2KT}{V_T^2}\cdot\frac{|Z_{IN,eq}|^2}{R_P}\cdot\sum_i F_i\right) \quad (7)$$

where $|Z_{IN,eq}|$ is the effective impedance of the tank by taking the coupling impedance Z_C into account, defined as

$$|Z_{IN,eq}|^2 = \frac{1}{2}\cdot|Z_T|^2\cdot\frac{2|Z_T|^2+|Z_C|^2}{2|Z_T|^2+\frac{1}{2}|Z_C|^2} \quad (8)$$

The impedance of an individual LC tank at each side can be approximated as

$$|Z_T| = \left|\frac{1}{2}\cdot\frac{R_P}{Q_T}\cdot\frac{f_o}{\Delta f}\right| \quad (9)$$

Q_T is the tank's effective Q. The noise factor contributed by ith noise source, F_i is defined by

$$F_i = N\cdot\frac{R_P}{4KT}\cdot\frac{1}{2\pi}\int_0^{2\pi}\Gamma_i^2(\emptyset)\cdot\overline{i_{n,i}^2(\emptyset)}\;d\emptyset \quad (10)$$

where $\Gamma_i(t)$ is the impulse sensitivity function (ISF) of the ith noise source, and $\overline{i_{n,i}^2(t)}$ is their corresponding noise power.

Since the output is sinusoidal, its tank ISF is in quadrature with the output, such that $\Gamma_T(\emptyset) = \cos(\emptyset)/N$ and N corresponds to the number of oscillators. Since $N = 2$ in the proposed design, the coupling between two identical oscillators results in a 3-dB PN improvement (ideally). F consists of noise contributed by the tank and the transistor, in which the noise factor of the tank is defined by

$$F_T = \frac{N}{\pi}\int_0^{2\pi}\Gamma_T^2(\emptyset)d\emptyset = \frac{2\Gamma_{T,rms}^2}{N} = 0.5 \quad (11)$$

When the transistors are in saturation region, noise is dominated by the transconductance (G_M), in which its noise contribution is defined by

$$F_{GM} = \frac{N}{\pi}\int_0^{2\pi}\Gamma_{MOS}^2(\emptyset)\cdot G_M(\emptyset)R_P\gamma\,d\emptyset \quad (12)$$

However, if the output swing is high enough to drive the transistors into triode region, its channel conductance (G_{DS}) also contributes noise, defined by

$$F_{GDS} = \frac{N}{\pi}\int_0^{2\pi}\Gamma_{MOS}^2(\emptyset)\cdot G_{DS}(\emptyset)R_P d\emptyset \quad (13)$$

Note that $\Gamma_T(\emptyset) = \Gamma_{MOS}(\emptyset)$ due to the absence of the tail current source, such that their directions of current impulse is injected from the source (ground) to the drain (LC tank).

Table I shows the comparison of the simulated noise factor between NMOS-only Class-B VCO and the proposed Class-C MS-SEC VCO. Since the output waveform is not harmonically shaped, class-B and SEC architecture exhibit identical F_T. Yet, for class-B, the noise due to G_M increases since the transistor has to overcome both the tank loss and its G_{DS} when operating in the triode region for a fraction of period (when $V_{DS} < V_{GS} - V_{TH}$), leading to increased noise due to G_{DS}.

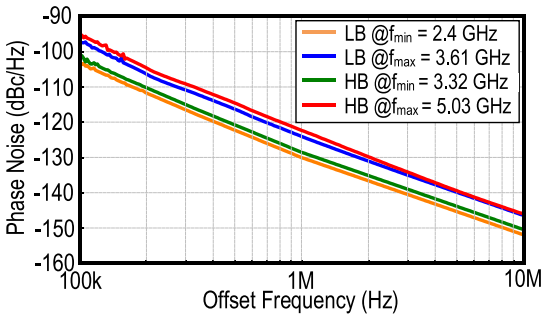

Fig. 9. Measured PN profile.

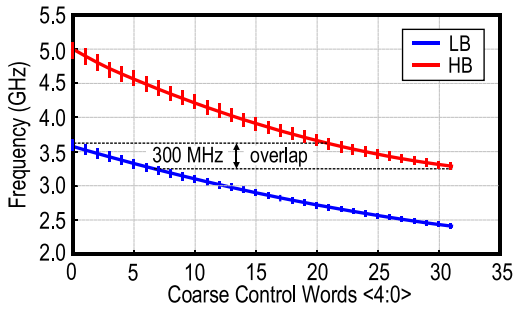

Fig. 10. Measured TR against tuning words of the switched capacitor.

III. MEASUREMENT RESULTS

The MS-SEC VCO prototyped in 130-nm CMOS with a 3.0 μm thick-top metal, occupies a 0.33-mm^2 die area (Fig. 8). Open drain buffer is used for measurement with an estimated capacitance of 17 fF. The long interconnect between the transformer and the capacitor array aids the capacitance tank boosting, i.e., raise the effective C when the switched capacitor is on. The width of the metal trace is maximized to reduce the tank loss. To guarantee a relatively weak coupling ($k_m = 0.21$) between the two inductors with the same inductance (ideally), we designed and simulated a 1-to-2-turn transformer using Sonnet EM with $L_1 = 0.81$ nH ($L_2 = 0.828$ nH) and $Q_1 = 23.7$ ($Q_2 = 19.5$) at 3 GHz. The measurement results are summarized as follows.

Fig. 9 plots the PN performances of the VCO. At 10 MHz offset, the PN for HB at 3.32 GHz is –150.4 dBc/Hz and for LB at 3.61 GHz is –146 dBc/Hz. By extrapolating the results to 20 MHz offset and normalizing to the 915-MHz carrier, the PN is –168.5 dBc/Hz (–164.1 dBc/Hz), meeting the stringent GSM specification by a 1.5-dB margin (i.e., 2.1 dB for a SAW-less transmitter), while drawing only 7.1 mA (3.76 mA) at 1.2 V.

As shown in Fig. 10, the VCO employs a 5-bit switched MOM capacitor array and a varactor for fine tuning, and is tunable from 2.4-to-3.61 GHz (40.2% TR) in LB mode, and 3.32-to-5.03 GHz (41%) in HB mode, corresponding to an effective TR of 70.6% with a 300-MHz overlap margin between the two modes. The vertical line in each control word corresponds to the varactor tunability.

TABLE II
PERFORMANCE BENCHMARK WITH THE STATE-OF-THE-ART

		This Work		[13] TCAS1' 17		[6] ISSCC' 14		[3] ISSCC' 14		[5] JSSC' 12	
Frequency Range (GHz)		**2.4 – 5.0**		3.37 – 5.96		3.24 – 8.45		2.4 – 5.3		2.5 – 5.6	
Tuning Range (%)		**70.6**		55.5		89.1		75.3		76.5	
V_{DD} (V)		1.2		1		0.8		0.4		0.6	
CMOS Technology		130 nm		40 nm		40 nm		65 nm		65 nm	
Area (mm^2)		0.33		0.12		0.43		0.25		0.29	
Frequency (GHz)		**2.4**	**5**	3.37	5.96	3.24	8.45	2.4	5.3	2.5	5.6
Power (mW)		**7.3**	**5.1**	16	12.5	16.5	14	6	4.4	14.2	9.9
PN (dBc/Hz)	1 MHz	**-130**	**-122.3**	126.9	-116	-129	-120	-126	-114	-128.6	-121.3
	10 MHz	**-151.9**	**-146**	-149.7	-137.8	-150	-142	-149	-139	-151.9	-145.8
FoM [1] (dBc/Hz)	1 MHz	**188.9**	**189.2**	185.4	180.5	187	187.1	185.8	182.1	185	186.3
	10 MHz	**190.9**	**192.9**	188.2	182.3	188	189.1	188.8	187.1	188.3	190.8
FoM_T [2] (dBc/Hz)	1 MHz	**205.9**	**206.2**	200.2	195.4	206	206.1	203.3	199.6	202.7	204
	10MHz	**207.9**	**209.9**	203.1	197.2	207	208.1	206.3	204.6	206	208.47
Meeting GSM spec.?		**Yes**		No		Yes		No		Yes	

1: $\mathrm{FoM} = -\mathrm{PN} + 20\log_{10}(f_0/\Delta f) - 10\log_{10}(P_{DC}/1\mathrm{mW})$ 2: $\mathrm{FoM_T} = \mathrm{FoM} + 20\log_{10}(\mathrm{TR}\%/10)$

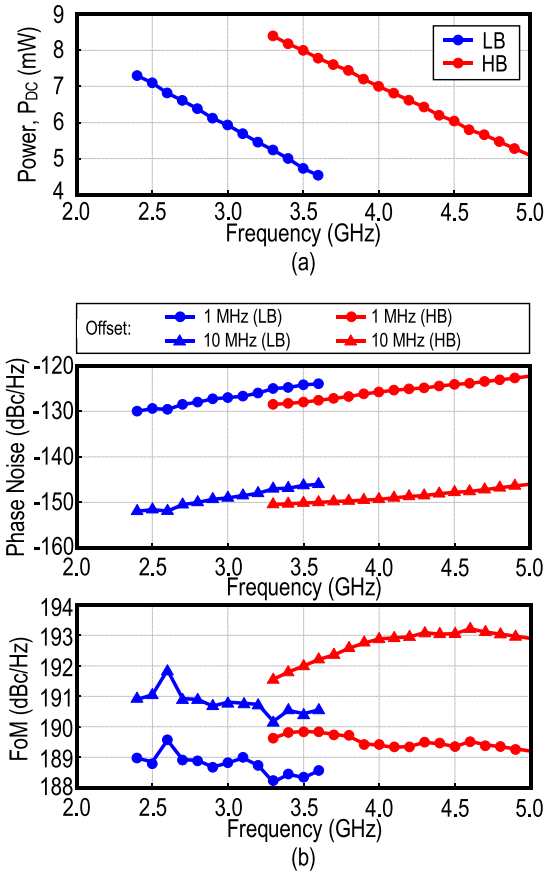

Fig. 11. Measured (a) power consumption against frequency and (b) PN (upper) and FoM (lower) against frequency.

The measured power consumption is kept <9 mW to achieve an excellent PN performance, with a variation between 4.54 to 7.3 mW (5.1 to 8.4 mW) in LB (HB) as Fig. 11(a) illustrates. Fig. 11(b) presents the PN and FoM variations against the frequency. The FoM is well >190 dBc/Hz at the thermal noise region, and its peak is at 193 dBc/Hz.

Table II benchmarks this brief with the state-of-the-art. Our VCO succeeds in extending the TR (>70%), while maintaining a high FoM, and fulfilling the stringent PN requirement of the SAW-less cellular transmitter (GSM).

IV. CONCLUSION

The design and implementation of a 130-nm CMOS Class-C MS-SEC VCO have been reported. By merging the advantages of wideband MS LC resonators, current-reuse $-g_m$ transistors and Class-C operation, a wide TR is achieved without sacrificing the PN performances. The experimental VCO prototype exhibits a high FoM >190 dBc/Hz across a TR >70%.

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