A 0.5-V 0.4-to-1.6-GHz 8-Phase Bootstrap Ring-VCO Using Inherent Non-Overlapping Clocks Achieving a 162.2-dBc/Hz FoM

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***Abstract*—An ultra-low-voltage 8-phase bootstrap (BT) ring-voltage-controlled oscillator (RVCO) exhibiting an improved figure of merit up to 165.2 dBc/Hz is reported. Unlike the existing RVCOs that use single-ended BT inverters with conventional clocks, our RVCO benefits from the inherent non-overlapping clocks of pseudo-differential BT inverters to reduce the charge loss due to asynchronous charge-pump operation, and the phase sensitivity to the transistor noise. They together result in higher oscillation frequency and output swing, while lowering the phase noise. Fabricated in 65-nm CMOS, the BT RVCO measures a phase noise of −93.7 to −92.6 dBc/Hz at a 1-MHz offset from 0.4 to 1.6 GHz, while dissipating 47.4 to 280 μW at 0.5 V.**

***Index Terms*—Ring voltage-controlled oscillator (RVCO), low voltage, bootstrap (BT), non-overlapping clock, phase noise.**

I. Introduction

ULTRA-LOW-VOLTAGE circuits offer the prospective towards self-powering ultra-low-power systems [1], [2] by energy harvesting, avoiding or reducing the loss of the boost converter that can have a limited power efficiency (<74% [3]). Still, constrained by the environments, energy sources like solar and thermoelectric sometimes only can output a small voltage as low as the transistor's threshold voltage. This brief investigates the bootstrap (BT) ring-VCO (RVCO) for a better performance under a 0.5-V supply. RVCO has the benefits of tiny area, wide frequency tuning range and immunity to magnetic pulling. Recent efforts on the system level have demonstrated the potential of RVCO to replace the bulky LC-VCO even for GHz-range wireless radios [4], [5].

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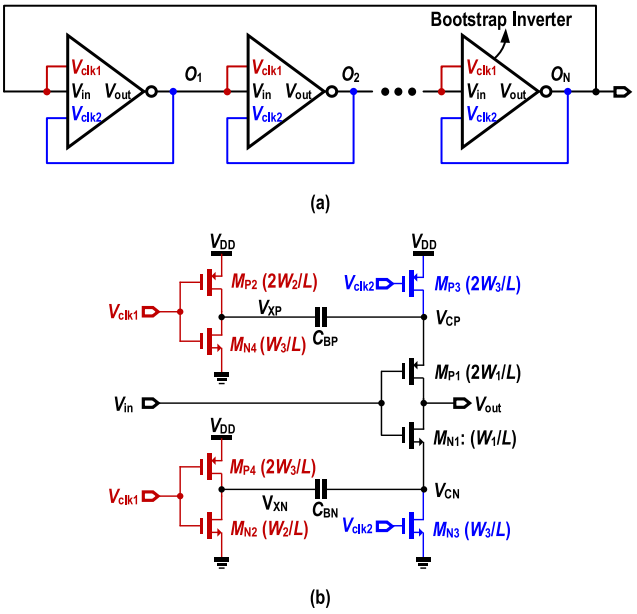

Fig. 1. (a) Single-ended BT RVCO and (b) schematic of the BT inverter.

For a typical RVCO using inverter-like delay elements, both its oscillation frequency and output drivability are low when the supply voltage is close to or below the transistor's threshold voltage. Also, the oscillation frequency becomes strongly nonlinear with the supply voltage. In [6] and [7], the BT RVCO is developed to take advantages of the built-in charge pump to boost the output swing of the delay element, e.g., the inverter in Fig. 1. Two embedded charge pumps (M_{N2-N3}, M_{P4}, C_{BN} and M_{P2-P3}, M_{N4}, C_{BP}) are switched by the inherent clock signals ($V_{clk1,2}$) of the RVCO. This BT technique succeeds in extending the internal supply voltages (V_{CP} and V_{CN}) of the inverted- based delay elements (M_{P1}, M_{N1}) to $(1+\beta)V_{DD}$ and $-\beta V_{DD}$; it implies an enlarged output swing by $\sim(1+2\beta)\times$, where β is a scaling factor <1 due to the charge loss under asynchronous charge pump clocking, and the charge sharing between C_{BN} and C_{BP} with the parasitic/load capacitors.

From Fig. 1(b), non-overlapping V_{clk1} and V_{clk2} are preferred to prevent M_{N2} and M_{N3} or M_{P2} and M_{P3} from switching on simultaneously. Regrettably, the single-ended configuration [6], [7] does not inherently feature such non-overlapping clocks. As a compromise, V_{clk1} and V_{clk2} are connected to V_{in} and V_{out}, respectively. If V_{clk1} is low while V_{clk2} is high, M_{N3} and M_{P4} in the bottom charge pump

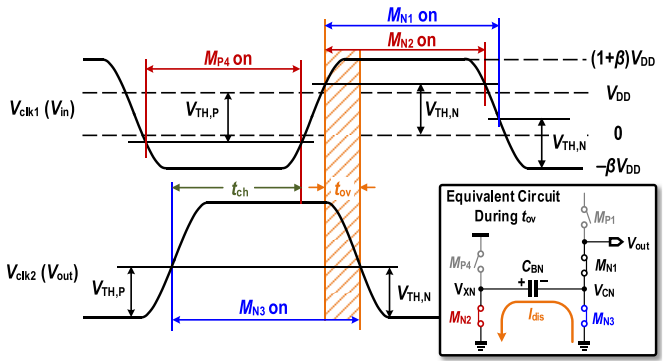

Fig. 2. Timing diagram of the $V_{clk1,2}$ in the single-ended BT RVCO and the states of the transistors in the bottom charge pump during the time interval t_{ov}. This defines the conventional clocks under low-voltage supply.

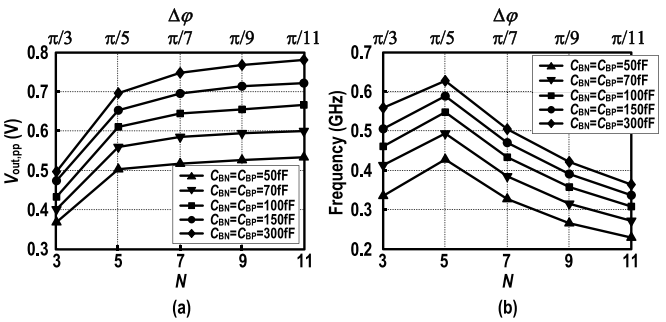

Fig. 3. Simulated (a) output swing and (b) oscillation frequency against the number of stage N and $\Delta\varphi$ for a single-ended BT RVCO. (V_{DD} = 0.3V, $W_1 = 0.3$ μm, $W_2 = 1$ μm, $W_3 = 0.75$ μm).

will be turned on, and the BT capacitor C_{BN} will be gradually charged to $\Delta V_{CBN} = V_{XN} - V_{CN} \approx V_{DD}$ during the capacitor charging period t_{ch} (or φ_{ch} in the phase domain) as shown in Fig. 2. During the period that V_{clk1} transits from $-\beta V_{DD}$ to $(1+\beta)V_{DD}$, M_{N1} and M_{N2} will be turned on when $V_{clk1} > V_{TH,N}$, which will discharge V_{out} from $(1+\beta)V_{DD}$ to $-\beta V_{DD}$. In fact, M_{N3} and M_{P4} should be turned off to prevent the charge loss during such period. Under a low-voltage supply (i.e., $V_{DD} < V_{TH,N} + V_{TH,P}$), M_{P4} controlled by V_{clk1} will always be turned off before M_{N1} and M_{N2} are turned on (Fig. 2). Yet, since V_{clk2} is connected to V_{out}, M_{N3} is still on for a long time t_{ov} (or φ_{ov} in the phase domain) as shown in Fig. 2 until V_{clk2} reaches $V_{TH,N} - \beta V_{DD}$. During t_{ov}, C_{BN} is discharged through M_{N2} and M_{N3}, resulting in the decrease of ΔV_{CBN}. A similar condition happens for the upper charge pump when V_{in} transits from high to low.

The loss of charge in M_{N3}/M_{P3} will degrade both the output swing and oscillation frequency, especially when $\varphi_{ov}/\varphi_{ch}$ is large. For an N-stage single-ended BT RVCO, the phase delay of the BT inverter is $\pi + \Delta\varphi$ where $\Delta\varphi = \pi/N$, and φ_{ch} and φ_{ov} can be approximated by π and $\Delta\varphi$, respectively. Thus $\varphi_{ov}/\varphi_{ch} \approx 1/N$, which implies severe output swing and frequency degradation at a small N. Fig. 3(a) plots the output swing versus N and $\Delta\varphi$ at different C_{BN}/C_{BP} when V_{DD} = 0.3 V, and the load capacitance C_L of each stage is ~8.4 fF. Here we choose the size of each PMOS transistor twice of that of the corresponding NMOS transistor to balance their conductance [Fig. 1(b)]. The sizes of M_{N3} and M_{N4} are kept the same since $C_{BN} = C_{BP}$. The minimum length (L = 60 nm) is chosen for each transistor to boost the oscillation frequency at low supply voltage. It is observed that the output swing is degraded especially when $N = 3$. For

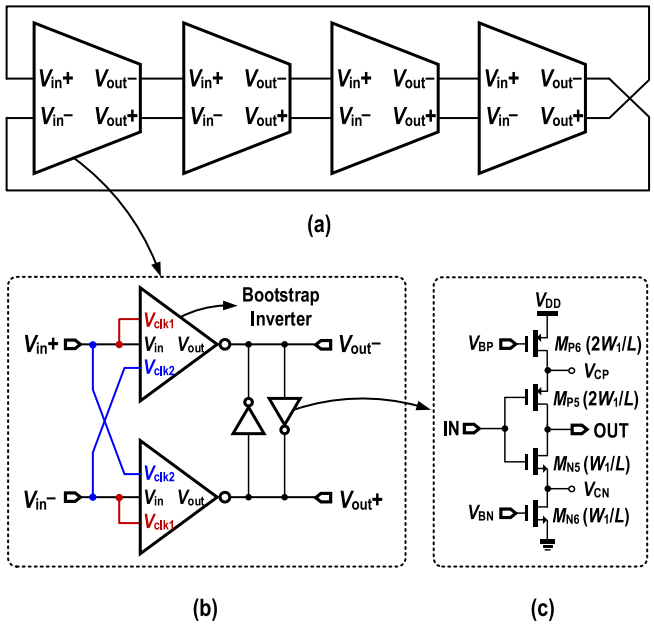

Fig. 4. (a) Block diagram of the proposed 8-phase BT RVCO core using non-overlapping clocks and (b) its pseudo-differential delay element. (c) Schematic of the cross-coupled inverter with auxiliary startup transistors.

a larger N, the increase of output swing becomes flat, since the charge loss of the parasitic capacitors becomes dominant. Fig. 3(a) shows that choosing a large C_{BN}/C_{BP} can raise the total charge stored on the BT capacitor increasing the output swing, but at the expense of chip area. For a RVCO using the same delay element, the oscillation frequency should be inversely proportional to N for the same output swing target. Yet, for the single-ended BT RVCO [Fig. 3(b)], the oscillation frequency at $N = 3$ is lower than that at $N = 5$, owing to the fact that a smaller output swing at $N = 3$ prolongs the delay in each stage.

The overlapping time t_{ov} between V_{clk1} and V_{clk2} will also degrade the phase noise of the BT RVCO, to be detailed in Section II. Although raising N can reduce t_{ov}, the oscillation frequency will inevitably decrease [Fig. 3(b)] as a tradeoff.

In this brief, we propose an 8-phase BT RVCO to deliver a pair of differential clocks for V_{clk1} and V_{clk2}, which eliminate the overlapping time between V_{clk1} and V_{clk2} at low-voltage supply, and thus boost the output swing and oscillation frequency while reducing the phase noise. Also, the pseudo-differential configuration is capable of offering a set of output signals with even number phases, which can be employed to support harmonic-rejection mixers [8] widely used in modern wideband RF transceivers.

II. Proposed 8-Phase BT-RVCO With Inherent Non-Overlapping Clocks

To eliminate the overlapping time t_{ov} between V_{clk1} and V_{clk2}, M_{P3} and M_{N3} [Fig. 1(b)] should be controlled by the differential version of V_{in} which is inherent in our BT RVCO with an even number of stages. Fig. 4 shows the 8-phase version of it. The BT inverters in Fig. 4(b) employ the same schematic as that in Fig. 1(b). Since the V_{clk1}/V_{clk2} is now controlled by $V_{in}+/V_{in}-$ ($V_{in}-/V_{in}+$), they can be non-overlapping ($t_{ov} = 0$) under $V_{DD} < 2V_{TH}/(1+\beta)$ where $V_{TH} = \max\{V_{TH,N}, |V_{TH,P}|\}$, assuming that the rising and falling edges are symmetric (Fig. 5).

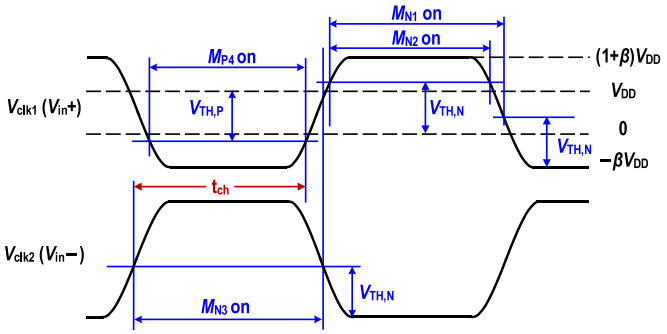

Fig. 5. Timing diagram of the clock signals in the 8-phase BT RVCO using non-overlapping clocks.

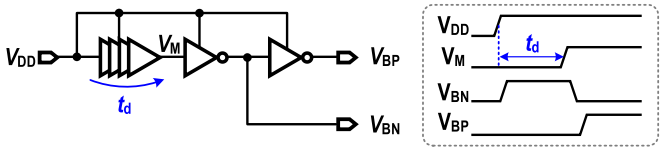

Fig. 6. Startup signal generation circuit.

To ensure the oscillation of a RVCO with an even number of stages, cross-coupled inverters must be added at the outputs of the pseudo-differential delay elements [9] as shown in Fig. 4(b). The supply and ground of the inverter (M_{N5}/M_{P5}) in Fig. 4(c) should be also connected to the boosted internal supply and ground V_{CP}/V_{CN} of the BT inverter, so that the boosted output swing will not be impaired. The proposed BT RVCO only can startup when the cross-coupled inverters work properly. Yet, the supply and ground voltages V_{CP}/V_{CN} of the cross-coupled inverters cannot be properly defined if the BT RVCO does not startup. Thus, the embedded charge pumps in the BT inverters will malfunction, since their clocks come from the outputs of the BT RVCO. Here, for startup robustness, we add the auxiliary transistors M_{N6}/M_{P6} to the cross-coupled inverter [Fig. 4(c)] to facilitate the startup of the BT RVCO. The control signals V_{BN}/V_{BP} for M_{N6}/M_{P6} are generated by a startup circuit (Fig. 6). Right after the V_{DD} ramps up, V_{BN}/V_{BP} will stay high/low for a reasonable time period of $t_d \approx 25$ μs, to turn on M_{N6}/M_{P6}, and the inverter (M_{N5}/M_{P5}) can be connected between V_{DD} and ground. When the oscillation is building up steadily and V_{CP}/V_{CN} are well defined, V_{BN}/V_{BP} can be changed to turn off M_{N6}/M_{P6} in order that the entire operation can achieve the desired output swing of $(1 + 2\beta)V_{DD}$.

To design the 8-phase RVCO using non-overlapping clocks, we use a small $W_1 = 0.3$ μm for the core inverter and sweep the sizes of the transistors in the charge pump, i.e., W_2 and W_3. The load capacitor C_L is also scaled with the transistor width. The output swing depends on the voltage on the BT capacitors and the charge sharing between the BT capacitors and C_L. A small W_3 degrades the voltage on the BT capacitors while a large W_3 will increase the C_L. Thus the output swing reaches its maximum at $W_3 = 0.75$ μm as shown in Fig. 7(a). The current consumption is determined by the sizes of transistors $M_{N1,N2}$ and $M_{P1,P2}$ as well as the output swing. Thus the current consumption changes in a similar way as the output swing when W_3 increases. When $W_3 > 0.75$ μm, the frequency drops fast due to the quick increase of the load capacitor. The phase noise improvement when W_3 increases from 0.5 to 0.75 μm is mainly due to the increase of output swing. As W_3 further increases, the phase noise reduction is mainly due to the frequency drop.

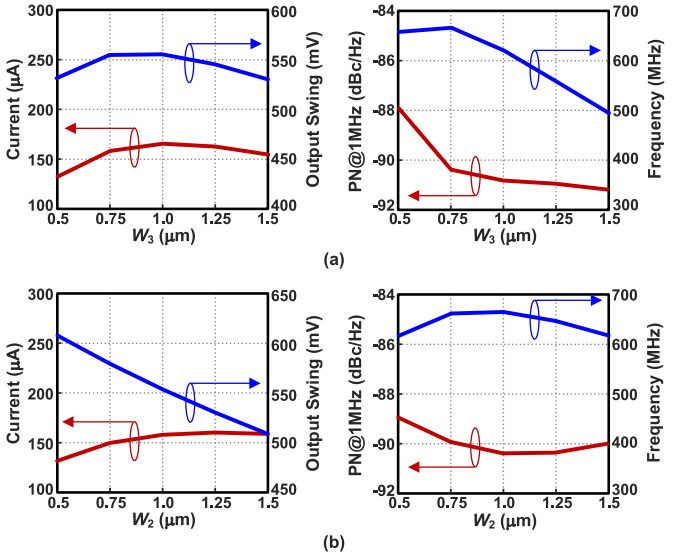

Fig. 7. Simulated current, output swing, oscillation frequency and phase noise of the 8-phase BT RVCO using non-overlapping clocks versus (a) W_3 ($W_2 = 1$ μm) and (b) W_2 ($W_3 = 0.75$ μm). ($V_{DD} = 0.3$V, $W_1 = 0.3$ μm, $C_{BN} = C_{BP} = 70$ fF).

As shown in Fig. 7(b), when W_2 increases, the output swing continuously decreases due to the increased C_L. When W_2 is comparable with W_1, the current can be increased by enlarging W_2, but will finally saturate when W_2 becomes much larger than W_1. As W_2 increases, the frequency will rise firstly due to the increased current and then decreases when the current saturates due to the increased C_L. According to Fig. 7(b), we can choose $W_2 = 1$ μm and $W_3 = 0.75$ μm to achieve high oscillation frequency and low phase noise.

The performance of the proposed 8-phase BT RVCO using non-overlapping clocks can be compared with itself under the conventional clocks, i.e., connecting V_{clk2} of the BT inverter to V_{out} in Fig. 4(b). For the 8-phase RVCO, the phase delay of the BT inverter becomes $\pi + \Delta\varphi$ where $\Delta\varphi = \pi/4$. According to Fig. 3, the RVCO using conventional clocks will suffer from noticeable output swing and oscillation frequency degradation due to this large $\Delta\varphi$. Fig. 8 compares the simulated performance of the 8-phase BT RVCOs using non-overlapping clocks and conventional clocks as well as the 5-stage single-ended BT RVCO which shows the highest oscillation frequency for the single-ended topology [Fig. 3(b)]. All the three designs employ the BT inverters with the same transistor sizes as $W_1 = (0.3 \times M)$ μm, $W_2 = (1 \times M)$ μm and $W_3 = (0.75 \times M)$ μm. The transistor sizes can be scaled up by increasing M. The 8-phase BT RVCO using non-overlapping clocks can achieve a higher frequency than both the 8-phase BT RVCO using conventional clocks and 5-stage single-ended BT RVCO when M increases from 1 to 8. In both the single-ended BT RVCO and the 8-phase BT RVCO using conventional clocks, M_{N3} and M_{P3} are turned on for quite a long time (t_{ov}) when the output transits (Fig. 2), which adds substantial noise contributions. In the proposed 8-phase BT RVCO using non-overlapping clocks, the phase noise contribution from M_{N3} and M_{P3} are significantly reduced by eliminating the overlapping time t_{ov} between V_{clk1} and V_{clk2}, resulting in a lower phase noise than the other two VCOs even operating at a higher frequency [Fig. 8(c)]. According to the simulated FoMs of the three VCOs in Fig. 8(d), the 8-phase BT RVCO using non-overlapping clocks can achieve a 3.3- and 3.0-dB better FoM than the 8-phase BT RVCO using

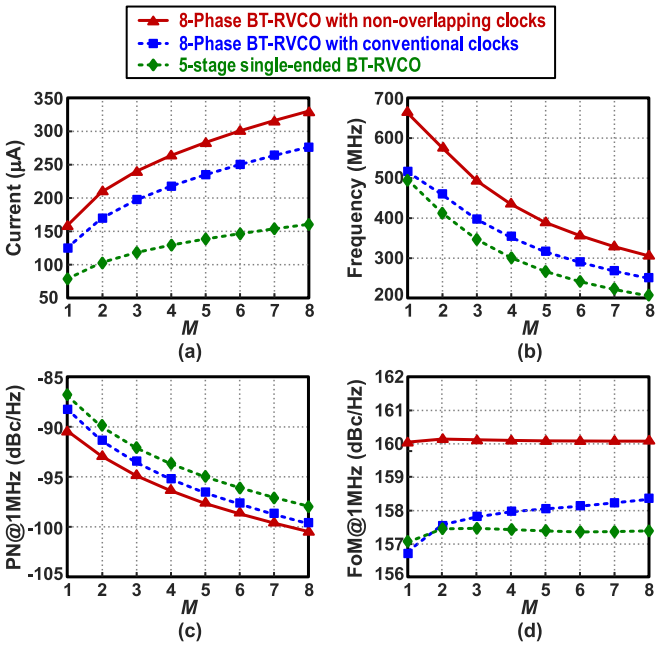

Fig. 8. Comparison of simulated (a) current, (b) oscillation frequency, (c) phase noise and (d) FoM for the 8-phase BT RVCOs using non-overlapping clocks and conventional clocks and 5-stage single-ended BT RVCO. ($V_{DD} = 0.3$ V, $W_2 = 1$ μm, $W_3 = 0.75$ μm).

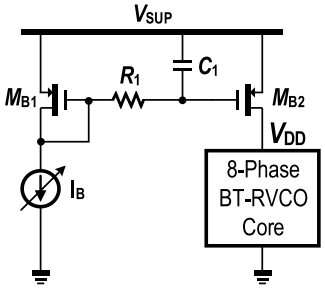

Fig. 9. Frequency tuning scheme for the proposed 8-phase BT RVCO.

conventional clocks and 5-stage single-ended BT RVCO at $M = 1$, respectively. At a large $M = 8$, the FoM improvement decreases to 1.8 and 2.7 dB mainly due to the reduced flicker noise contribution from M_{N3} and M_{P3} when their sizes become larger. Particularly, when operating at a similar frequency of 400 MHz, the 8-phase BT RVCO using non-overlapping clocks can achieve a 2.3- and 2.7-dB higher FoM than the other two RVCOs.

The frequency tuning of the proposed 8-phase BT RVCO is achieved by changing its current as Fig. 9 shows. The use of the current mirror improves the frequency pulling against supply variation. The lowpass filter (R_1 and C_1) is to suppress the noise contribution from M_{B1}.

III. Measurement Results

Two prototypes were fabricated in 65-nm CMOS (Fig. 10) for comparison: 8-phase BT RVCOs under non-overlapping clocks and conventional clocks. We chose $C_{BN} = C_{BP} = 70$ fF to ensure a small core area (0.0033 mm^2) and $W_1 = 0.3$μm, $W_2 = 1$ μm and $W_3 = 0.5$ μm to achieve a high frequency while still keeping low power consumption. Both prototypes occupy the same total area of ~0.01 mm^2 with the current mirror as the main contributor for this value.

TABLE I
Comparison Between Simulation and Measurement Result

	Freq. (GHz)	Current (μA)	PN@1MHz (dBc/Hz)	FoM@1MHz (dBc/Hz)
Simulation (Proposed)	1.41	472	−90.2	159.5
Measurement (Proposed)	1.40	455	−92.0	161.4
Simulation (Conventional)	1.35	480	−88.1	156.9
Measurement (Conventional)	1.36	512	−90.2	158.8

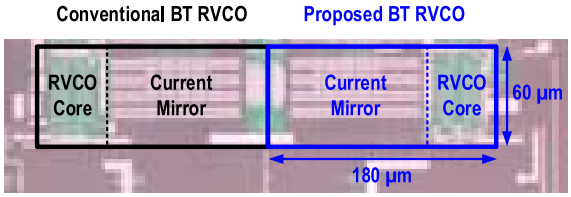

Fig. 10. Chip photo of the two fabricated BT RVCOs in 65-nm CMOS.

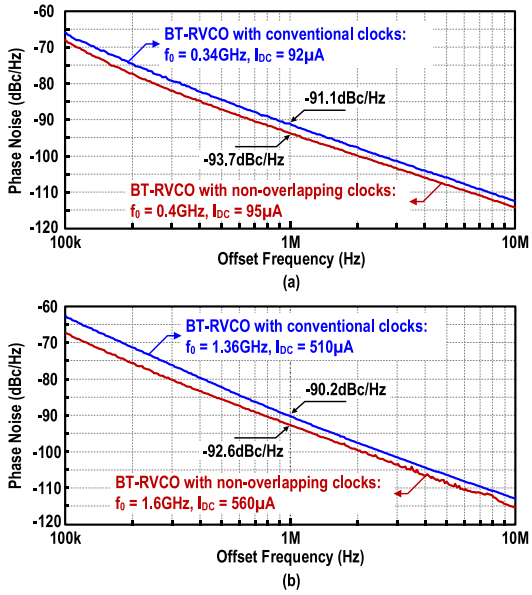

Fig. 11. Measured phase noise of the BT RVCOs using non-overlapping and conventional clocks at the (a) lowest and (b) highest frequencies.

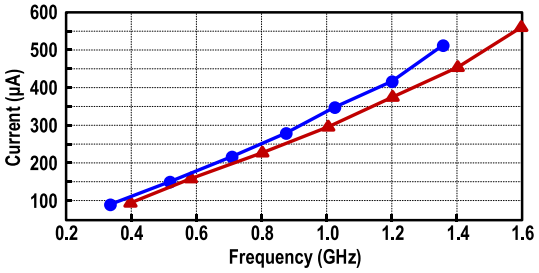

Fig. 12. Measured current consumptions of the two BT RVCOs with non-overlapping clocks (triangle symbols) and conventional clocks (circle symbols) versus the oscillation frequency.

We fixed the supply voltage at 0.5 V and tuned the frequency by changing the bias current I_B (Fig. 9).

Fig. 11 illustrates the phase noises at offset frequencies from 100 kHz to 10 MHz measured by Keysight E5052B Signal

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	This work				TCAS-II'15 [11]	JSSC'13 [7]	TCAS-I'11 [12]	TCAS-II'09 [13]
Topology	BT RVCO using non-overlapping clocks		BT RVCO using conventional clocks		Relaxation DCO with Adaptive Threshold Calibration	BT RVCO using conventional clocks	Bulk-Driven RVCO	Bulk-Driven RVCO
Supply Voltage (V)	0.5				0.5	0.2-0.6*	0.5	0.5
Frequency Range (GHz)	0.4 – 1.6 (120%)		0.34 – 1.36 (120%)		0.0435 – 0.152 (111%)	0.04 – 0.771 (180%)	0.16 – 2.5 (175.9%)	0.306 – 0.725 (81.3%)
Carrier (GHz)	0.4	1.6	0.34	1.36	0.1	0.771	2.24	0.55
Power (μW)	47.4	280	45.7	260	59	87.6	1157	210
PN @ 1MHz (dBc/Hz)	−93.7	−92.6	−91.1	−90.2	−103.4	−89	−87	−95
FoM @ 1MHz (dBc/Hz)	**159.0**	**162.2**	155.1	158.7	155.7	157.3	153.4	156.6
No. of Output Phases	**8**		8		2	5	8	3
Core Area (mm^2)	0.0108		0.0108		0.0362	0.0019	0.0017	0.017
CMOS Technology	65nm				65nm	90nm	90nm	0.13μm

* Frequency tuning through changing V_{DD}.

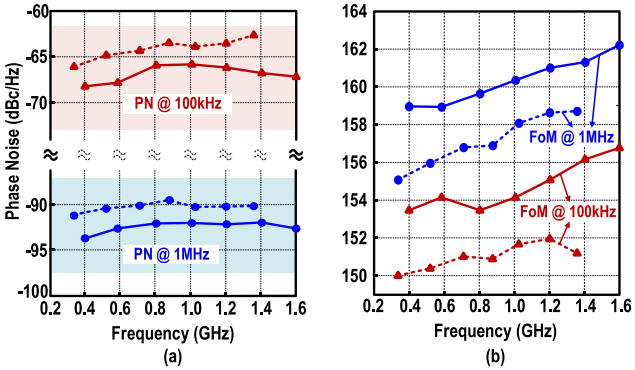

Fig. 13. Measured (a) phase noise and (b) FoM of the two BT RVCOs with non-overlapping clocks (solid lines) and conventional clocks (dashed lines) versus the oscillation frequency.

Source Analyzer. At 1-MHz offset, the phase noise of the proposed BT RVCO is 2.4/2.6 dB better at the lowest/highest frequencies when compared with those of the conventional BT RVCO. As Fig. 12 exhibits, the proposed BT RVCO also shows a higher oscillation frequency under the same current due to the increased output swing. Table I compares the simulated and measured BT-RVCO performance. The measured FoM improvement at 1-MHz offset is 2.6 dB which is close to that of the simulation results. The discrepancies on the absolute values of phase noise and FoM between simulation and measurement are likely caused by the inaccurate device model and the exclusion of the bondwire effect in the simulation.

Fig. 13 compares the phase noise and FoM between the BT RVCOs under non-overlapping and conventional clocks. The former shows better results from 100 kHz to 10 MHz offsets, and extends the highest oscillation frequency from 1.36 to 1.6 GHz.

Table II summarizes the performance and comparison with other similar circuit structures. Benchmarking with the BT RVCO under the conventional clocks, this brief shows an improved FoM up to 3.9 dB at 1-MHz frequency offsets. Likewise, when contrasted with other recently published VCO/DCOs with a low supply voltage, this brief inherently provides an 8-phase output, and shows a higher FoM at 1-MHz frequency offsets. The relatively large chip area is mainly due to the current mirror employed for frequency tuning.

IV. CONCLUSION

An 8-phase BT RVCO using the inherent non-overlapping clocks is proposed. The new clocking scheme aids to reduce the charge loss from the embedded charge pump, and reduces the phase sensitivity to the transistor noise, resulting in boosted output swing and oscillation frequency and reduced phase noise. The proposed techniques can be applied to other BT RVCOs with even number of delay stages.

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