

A Wideband Inductorless dB-Linear Automatic Gain Control Amplifier Using a Single-Branch Negative Exponential Generator for Wireline Applications

Lingshan Kong, Yong Chen¹, *Member, IEEE*, Chirn Chye Boon, *Senior Member, IEEE*,
Pui-In Mak², *Senior Member, IEEE*, and Rui P. Martins, *Fellow IEEE*

Abstract—This paper reports a wideband inductorless automatic gain control (AGC) amplifier for wireline applications. To realize a dB-linear AGC range, a pseudo-folded Gilbert cell driven by a single-branch negative exponential generator (NEG) is proposed as the core variable-gain amplifier. The NEG features a composite of dual Taylor series to extend the AGC approximation range without sacrificing the precision. Fabricated in 65-nm CMOS, the AGC amplifier occupies a tiny die area of 0.045 mm² and consumes 28 mW at 1.2 V. Measured over a dB-linear gain range of ~40 dB, ± 1 dB gain error is achieved and the 3-dB bandwidth stays roughly constant at 7 GHz. For the closed-loop AGC measurement, the input dynamic range is ~40 dB (10 mV_{pp} to 1 V_{pp}) for a BER <math><10^{-12}</math> under a 2⁷ – 1 PRBS data at 10 Gb/s. The achieved figure-of-merit (FOM) of 2.8 pJ/bit compares favorably with state-of-the-art.

Index Terms—Automatic gain control (AGC) amplifier, negative exponential generator (NEG), dB-linear, CMOS, Taylor series, dynamic range, rational approximation, pseudo-exponential function, bipolar junction transistors (BJTs).

I. INTRODUCTION

FOR various wireline channels in the flexible-reach wireline [1] and optical [2] receivers, an automatic gain control (AGC) amplifier plays a key role to accommodate

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L. Kong and C. C. Boon are with Nanyang Technological University, Singapore 639798 (e-mail: lkong2@e.ntu.edu.sg; eccboon@ntu.edu.sg).

Y. Chen is with the State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau 999078, China (e-mail: ychen@umac.mo).

P.-I. Mak is with the State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau 999078, China, and also with the Faculty of Science and Technology, Department of ECE, University of Macau, Macau 999078, China (e-mail: pimak@umac.mo).

R. P. Martins is with the State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau 999078, China, also with the Faculty of Science and Technology, Department of ECE, University of Macau, Macau 999078, China, and the Instituto Superior Técnico, Universidade de Lisboa, 1049-001 Lisboa, Portugal (e-mail: rmartins@umac.mo).

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the input-swing variation at the analog front-end. In addition to the obvious goals of low power, compactness and wide bandwidth (BW), the desired AGC amplifier should support a wide input dynamic range while preserving a constant BW. The dB-linear gain characteristic can be provided by an exponential generator, which converts the control signal from linear to exponential. Although such feature can be obtained from the intrinsic exponential relationship (e^x) of BJT [3] in BiCMOS, parasitic BJT [4], or subthreshold-biased MOSFET [5] in CMOS, they are not favored for their limited input swing, speed and matching accuracy, as well as large noise contribution [4].

With the absence of effective e^x in CMOS, recent works [6]–[9] focus on multi-function approximation to extend the finite range of the exponential feature with an acceptable gain error. One possible way to fulfill it is to incorporate switching circuits as part of the exponential generator, while choosing the corresponding numerator and denominator of the rational equation for different control regions [7]–[9]. This approach, however, increases the complexity of the exponential generator, and introduces unreliability and errors into the loop. As a result, in [9], the input dynamic range is limited to 24 dB over a 40-dB linear AGC range.

This paper introduces a circuit technique to approximate the exponential function with a single-branch negative exponential generator (NEG), where different operating regions of the MOSFETs are fully utilized, such that a wide dB-linear AGC range can be achieved with minimum hardware. Fabricated in 65-nm CMOS, the inductorless AGC amplifier with the proposed NEG exhibits an input dynamic range of ~40 dB for a BER <math><10^{-12}</math> while amplifying a 10-Gb/s PRBS data input with ± 1 dB gain error. The power consumption is 28 mW at 1.2 V, and the active area is just 0.045 mm².

This paper is organized as follows: Section II overviews the existing e^x approximation and implementation techniques. The mathematical mechanism and implementation of the NEG are detailed in Section III. Section IV describes the complete AGC amplifier. The measurement results are summarized in Section V, and finally the conclusions are drawn in Section VI.

TABLE I
SUMMARY OF THE EXISTING AND PROPOSED EXPONENTIAL GENERATOR TOPOLOGIES

Exponential approx. methods	No. of devices in references	Equation	x for error $\leq 5.5\%$ / x range	x for error ≤ 1 dB / x range	Need extra switching logic
Taylor series	23 MOSFETs* + 1 CS** + 1 R*** [14]	$1+x+\frac{1}{2}x^2$	-0.6 < x < 0.85 / 1.45	-0.75 < x < 1.15 / 1.9	No
Pseudo exponential	12 MOSFETs + 1 CS [11]	$(1+\frac{1}{2}x)/(1-\frac{1}{2}x)$	-0.85 < x < 0.83 / 1.68	-1.05 < x < 1.05 / 2.1	No
Linear equation multiplication	24 MOSFETs [6]	$(1+\frac{x}{3})^3$	-0.55 < x < 0.62 / 1.17	-0.75 < x < 0.9 / 1.65	No
Dual Taylor series	3 MOSFETs [This work]	$G_{1s}(x)$ or $G_{2s}(x)$	-1.15 < x < 1.12 / 2.27	-1.85 < x < 1.67 / 3.53	No
Rational approx. (1 st -order)	70 MOSFETs + 14 CSs [7]	$(1+\frac{15}{16}x)/(1-\frac{5}{16}x)$ or $(1+\frac{5}{16}x)/(1-\frac{15}{16}x)$	-2.1 < x < 2.1 / 4.2	-2.3 < x < 2.3 / 4.6	Yes
Rational approx. (2 nd -order)	38 MOSFETs [8]	$f(x)=\frac{x^2+6x+12}{x^2-6x+12}$	-2 < x < 2 / 4	-2.3 < x < 2.3 / 4.6	Yes
Enhancement rational approx. (2 nd -order)	84 MOSFETs [9]	$e^{-2f(x+2)}$ or $e^{2f(x-2)}$	-4 < x < 4 / 8	-4.6 < x < 4.6 / 9.2	Yes
Parasitic BJT	3 MOSFETs + 2 BJT + 2 Rs [4]	e^x	$-\infty < x < \infty$ / ∞	$-\infty < x < \infty$ / ∞	No

* MOSFET is a metal-oxide-semiconductor field-effect transistor. ** CS is a current source. *** R is a resistor.

II. OVERVIEW OF e^x APPROXIMATION AND IMPLEMENTATION

This section briefly reviews the existing e^x approximation and implementation techniques in CMOS technologies. Due to the absence of intrinsic e^x CMOS devices operating in the saturation region, one possible way to generate it is to use a pseudo-exponential generator [10], [11]. The pseudo-exponential function (Table I) offers an accurate approximation of $\leq 5.5\%$ error with $-0.85 < x < 0.83$, or ≤ 1 dB error with an x range of 2.1. For the conventional designs [10], [11], the input differential pair and diode-connected load pair share a constant current, so that the resultant exponential approximation term is under a square root. Consequently, the tuning range is limited to half of the available range. Although cascading two such stages can double the tuning range, it implies extra power and area. The BW limit and variation under different gain settings are also matters of concern, as parasitic capacitances are accumulated at the output node.

Alternatively, the 2nd-order Taylor series expansion [12]–[14] can also be used for e^x approximation (Table I). Theoretically, the approximation error is $\leq 5.5\%$ for $-0.6 < x < 0.85$, or ≤ 1 dB error with an x range of 1.9. Its voltage-mode implementation, however, suffers from severe nonlinearity due to the mobility degradation and mismatch effect (especially for short-channel devices), while the constraint on the operating region also limits its approximation range [12]. On the other hand, the current-mode implementations [12], [13] usually require a number of current mirrors, multipliers or squarers, demanding ~ 20 MOSFETs.

Practically, a V-I converter is required to generate a linear current output with respect to the input control voltage, which is then injected to the current square circuit to create the 2nd-order term [14]. The resultant current is then summed by a certain dc current and used to control the linear VGA blocks. Because a total of 25 devices (Table I) are involved to achieve an overall exponential current, the chip area and power consumption are penalized.

Driven by the limited accuracy (x range <2) of the above single piece approximation functions, other works employing multi-function approximation have also been reported [6]–[9], in order to enlarge the approximation range to approach the ideal e^x [4]. A new approximation function based on the limit definition of the exponential function (Table I) was proposed in [6]. Three identical stages are cascaded to verify the idea, each of which uses two parallel transistors with different oxide thickness and sizes, as the source-degeneration resistors to realize dB-linear gain control. As a result, both gain-variation range and gain error ($< \pm 0.5$ dB) are improved. Nevertheless, its BW limitation resulting from the parasitic capacitance is severe, while non-standard CMOS process exacerbates the cost of implementation. The pseudo-exponential function can be further extended to complicated rational approximations [7]–[9], which are shifted and scaled to the adjacent regions to fit the same exponential curve. The accurate x range is extended to >4 , but it demands extra blocks such as a current-ratio generator and switching logics, resulting in an increase of hardware to >80 devices (Table I), and even instability of the AGC loop.

III. PROPOSED NEGATIVE EXPONENTIAL GENERATION (NEG)

Although combined approximation functions, and successive approximation by shifting and scaling, work effectively to enlarge the dB-linear gain range, this work aims to design a simple circuit without compromise on the gain variation range, and yet being dB-linear-accurate by taking the advantage of dynamic operating regions of the MOSFETs.

A. Mathematical Approximation

The proposed negative exponential approximation is based on the following general function $g_n(x)$,

$$g_n(x) = a_n + b_n x + c_n \sqrt{d_n + e_n x + f_n x^2} \quad (1)$$

where x is an independent variable, and coefficients a_n to f_n are determined by the following calculations in Section III-B. At $x = 0$, the Taylor series expansion up to the 2nd-order is used for the last term in (1) leading to

$$\sqrt{d_n + e_n x + f_n x^2} \approx \sqrt{d_n} + \frac{e_n}{2\sqrt{d_n}}x + \frac{d_n f_n - \frac{e_n^2}{4}}{2d_n^{3/2}}x^2 \quad (2)$$

Thus, we can rearrange (1) as

$$\begin{aligned} g_n(x) &\approx \left(a_n + c_n \sqrt{d_n}\right) + \left(b_n + \frac{c_n e_n}{2\sqrt{d_n}}\right)x + c_n \frac{d_n f_n - \frac{e_n^2}{4}}{2d_n^{3/2}}x^2 \\ &= O_n + P_n x + Q_n x^2 \end{aligned} \quad (3)$$

Assuming $-P_n/O_n = \sqrt{2Q_n/O_n} = K_n$, where $P_n < 0$, the proposed exponential approximation is expressed as

$$g_n(x) \approx O_n e^{-K_n x} \quad (4)$$

To give a fair mathematical comparison in Table I, equation (1) is normalized to

$$G_n(x) = A_n + B_n x + C_n \sqrt{D_n + E_n x + F_n x^2} \approx e^{-x} \quad (5)$$

where A_n to F_n are the normalized coefficients. Thereafter, by adjusting the different groups of the normalized coefficients (A_1 to F_1) and (A_2 to F_2), one concave function $G_1(x)$ and the other convex function $G_2(x)$ can be obtained to approximate the same ideal e^{-x} around the origin [Fig. 1(a)]. Their approximation regions may vary slightly, but both approximation errors decrease as x approaches “0”.

To increase both the available control input and the dB-linear gain range, two shifted single functions, $G_{1s}(x)$ and $G_{2s}(x)$, are combined as a dual Taylor series approximation at the reference point [$x = 0$ in Fig. 1(b)]. We shift $G_1(x)$ toward the $-x$ direction by an amount equal to ΔX_1 , and then move upward $G_1(x + \Delta X_1)$ by ΔY_1 in y direction. $G_{1s}(x)$ is achieved and plotted in Fig. 1(b), which remains the concave feature over region I. Inversely, $G_2(x)$ is shifted by ΔX_2 in $+x$ direction, and $G_2(x + \Delta X_2)$ is moved down by ΔY_2 vertically. We obtain $G_{2s}(x)$ [Fig. 1(b)] which is a convex function over region II. The Taylor series of $G_{1s}(x)$ and $G_{2s}(x)$ are both parallel with the ideal exponential line [Fig. 1(b)], and the entire curve that we proposed is constructed within a certain gain error, called an “inverse S-shaped curve”, which is optimized by the following transistorized implementation.

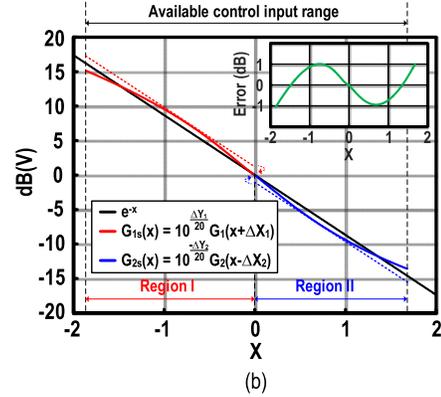
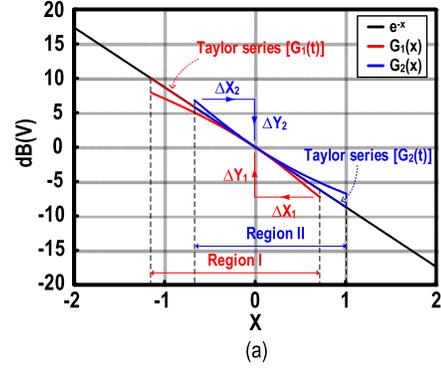


Fig. 1. The mathematical steps of the proposed negative exponential approximation: (a) single-function generation and (b) combined response of the two single-function approximations.

B. Circuit Implementation

Figure 2(a) describes the schematic of the proposed NEG, consisting of only three MOSFETs, which realizes a dB-linear characteristic between the differential control voltage ($V_{yx} = V_y - V_x$) and the single-ended control input voltage (V_{ctrl}). As V_{ctrl} increases to the transition voltage (V_m), the bias transistor (M_1), whose gate voltage is fixed, is maintained in triode-region operation, while the control transistor (M_2) enters the saturation region [Fig. 2(b)]. We define this operating condition as “region I”. When V_{ctrl} is continually increased beyond V_m , namely “region II”, M_1 enters into the saturation region and M_2 switches to the triode region. In both regions I and II, the diode-connected transistor (M_3) remains in the saturation region. Interestingly, a transition between regions I and II exists around V_m , i.e. “region III”, where both M_1 and M_2 are operated in the saturation region. As such, the relation between V_{yx} and V_{ctrl} is purely linear, instead of dB-linear. Thus, we should avoid the occurrence of region III, or narrow it. Assuming M_1 switches from triode region to saturation at a control voltage V_{ctrl1} , while M_2 switches from saturation region to triode at another control voltage V_{ctrl2} , at the point of switching, we have

$$V_{DS1} = V_{GS1} - V_{TH1} \Rightarrow V_x = V_{bias} - V_{TH1} \quad (6)$$

$$V_{DS2} = V_{GS2} - V_{TH2} \Rightarrow V_y = V_{ctrl2} - V_{TH2} \quad (7)$$

where V_{DSx} , V_{GSx} and V_{THx} are the drain-source voltage, gate-source voltage and threshold voltage of transistors, respectively. Fig. 2(c) introduces the optimization procedure of eliminating region III [16]. If V_{bias} is increased, the current

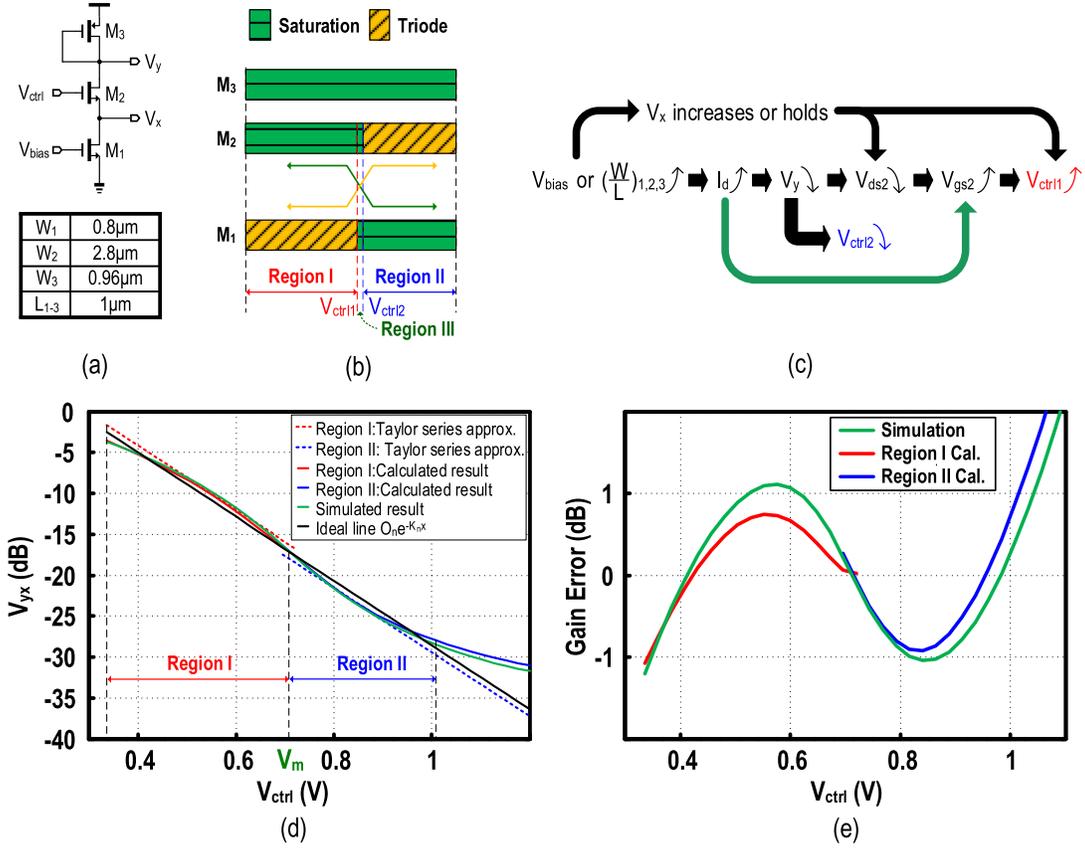


Fig. 2. (a) Schematic of the proposed NEG. (b) The different operating regions of (a). (c) Optimization procedure of eliminating region III. (d) Simulated and calculated (V_{yx}) curves versus V_{ctrl} . (e) Simulated and calculated gain errors versus V_{ctrl} .

flowing through the NEG is increased, leading to a decrease of V_y . According to (7), V_{ctrl2} shall have a lower value and move towards left in Fig. 2(b). On the other hand, V_x is also increased with V_{bias} given by (6), together with the decrease in V_y , resulting in a drop of the drain-source voltage across M_2 . The gate-source voltage of M_2 , therefore, must be larger to produce the increased current, indicating a right shift of V_{ctrl1} in Fig. 2(b). Increasing the aspect ratio of each transistor has the same effect in a similar manner, since it also increases the current flowing through this single-branch in the NEG, making the switching behavior of M_1 to occur later while M_2 sooner. The simulated inverse S-shaped curve, which is the composite of dual Taylor series, approximates the ideal exponential line and the gain error is $< \pm 1$ dB, as plotted in Fig. 2(d) and (e), respectively.

We start to derive the relation between V_{yx} and V_{ctrl} for both regions I and II, recurring to the basic I-V characteristics of MOSFETs in different operating regions. In region I, the I-V equations of M_i ($i = 1, 2$ and 3) are given by

$$I_{d11} = K_1 \left[(V_{bias} - V_{th1}) \cdot V_x - \frac{1}{2} V_x^2 \right] \quad (8)$$

$$I_{d21} = \alpha_1 K_2 (V_{ctrl} - V_x - V_{thf} + \beta_1 V_{th2})^2 \quad (9)$$

$$I_{d31} = \frac{1}{2} K_3 (V_{DD} - V_y - |V_{th3}|)^2 \quad (10)$$

where $K_i = \mu_{ni} C_{oxi} W_i / L_i$ and $V_{thf} = V_{th2} + kV_x$ is the threshold voltage with substrate bias present. μ_{ni} is the charge-carrier effective mobility; C_{oxi} is the gate oxide

capacitance per unit area; W_i / L_i is the aspect ratio of M_i and V_{thi} is the zero- V_{SB} value of threshold voltage of the i^{th} MOSFET. The body effect parameter (k) of 0.09 is extracted from the simulation. α_1 and β_1 are the corrected coefficients in the proposed corrected equation (9) compared with the traditional square-law model in the saturation region [15, eq. (2.13)]. If $I_{d11} = I_{d21} = I_{d31}$, we achieve

$$V_{yx1} = a_1 + b_1 x_1 + c_1 \sqrt{d_1 + e_1 x_1 + f_1 x_1^2} \quad (11)$$

The coefficients and x_1 of (11) are derived as

$$\left\{ \begin{array}{l} a_1 = V_{DD} - |V_{th3}| + \frac{(m\sqrt{K_2'/K_3} - 1)(V_{bias} - V_{th1})}{1 + m^2(K_2'/K_1)} \\ \quad - \frac{\sqrt{K_2'/K_3} + m(K_2'/K_1)}{1 + m^2(K_2'/K_1)} V_{01} \\ b_1 = -\frac{\sqrt{K_2'/K_3} + m(K_2'/K_1)}{1 + m^2(K_2'/K_1)} \\ c_1 = -\frac{m\sqrt{K_2'/K_3} - 1}{1 + m^2(K_2'/K_1)} \\ d_1 = (V_{bias} - V_{th1})^2 + 2m(K_2'/K_1)(V_{bias} - V_{th1})V_{01} \\ \quad - (K_2'/K_1)V_{01}^2 \\ e_1 = 2m(K_2'/K_1)(V_{bias} - V_{th1}) - 2(K_2'/K_1)V_{01} \\ f_1 = -K_2'/K_1 \\ x_1 = V_{ctrl} - (1 - \beta_1)V_{th2} - V_{01} \end{array} \right. \quad (12)$$

where $K'_2 = \alpha_1 K_2$ and $m = 1 + k = 1.09$. To precisely fit the simulated I-V curve of M_2 in the saturation, the corrected coefficients (α_1 and β_1) are found to be 0.25 and 0.28, respectively. V_{01} is a purely-mathematical coefficient for shifting the single point on the calculated result [equation (11)], where the Taylor series is conducted in region I. The calculated value of (11) and its corresponding gain error in region I are plotted in Fig. 2(d) and (e). At $V_{ctrl} = 0.59$ ($x_1 = 0$), we expand (11) to approximate $O_1 e^{-K_1 x_1}$ by the 2nd-order Taylor series.

In region II, the I-V equations of M_i ($i = 1, 2$ and 3) are given by

$$I_{d12} = \frac{1}{2} K_1 (V_{bias} - V_{th1})^2 \quad (13)$$

$$I_{d22} = \alpha_2 K_2 \left[\beta_2 (V_{ctrl} - V_x - V_{thf} + \gamma V_{th2}) (V_y - V_x) - \frac{1}{2} (V_y - V_x)^2 \right] \quad (14)$$

$$I_{d32} = \frac{1}{2} K_3 (V_{DD} - V_y - |V_{th3}|)^2 \quad (15)$$

where α_2 , β_2 and γ are the corrected coefficients in the proposed corrected equation (14) compared with the traditional model in the triode region [15, eq. (2.8)]. Setting $I_{d12} = I_{d22} = I_{d32}$, we obtain

$$V_{yx11} = a_2 + b_2 x_2 + c_2 \sqrt{d_2 + e_2 x_2 + f_2 x_2^2} \quad (16)$$

where

$$\left\{ \begin{array}{l} a_2 = -\frac{\beta_2}{2\beta_2(k+1)-1} [V_{02} - (1-\gamma)V_{th2} - (k+1)V_y] \\ b_2 = -\frac{\beta_2}{2\beta_2(k+1)-1} \\ c_2 = 1 \\ d_2 = \frac{2I_{d1}}{\alpha_2 K_2 [2\beta_2(k+1)-1]} \\ + \left(\frac{\beta_2}{2\beta_2(k+1)-1} [V_{02} - (1-\gamma)V_{th2} - (k+1)V_y] \right)^2 \\ e_2 = \frac{2\beta_2^2}{[2\beta_2(k+1)-1]^2} [V_{02} - (1-\gamma)V_{th2} - (k+1)V_y] \\ f_2 = \frac{\beta_2^2}{[2\beta_2(k+1)-1]^2} \\ x_2 = V_{ctrl} - V_{02} \end{array} \right. \quad (17)$$

To precisely fit the simulated I-V curve of M_2 in the triode region, the corrected coefficients (α_2 , β_2 and γ) are found to be 0.77, 0.97 and 0.16, respectively. V_{02} is a purely-mathematical coefficient for shifting the single point on the calculated result [eq. (16)], where the Taylor series is conducted in region II. Again, as shown in Fig. 2(d) and (e), the calculated V_{yx11} and gain error in region II, together with the calculated results in region I, match with the simulated inverse S-shaped curve. By using the 2nd-order Taylor series, equation (16) is expanded to approximate $O_2 e^{-K_2 x_2}$ at $V_{ctrl} = 0.85$ ($x_2 = 0$). To guarantee the parallel relationship between the two Taylor series

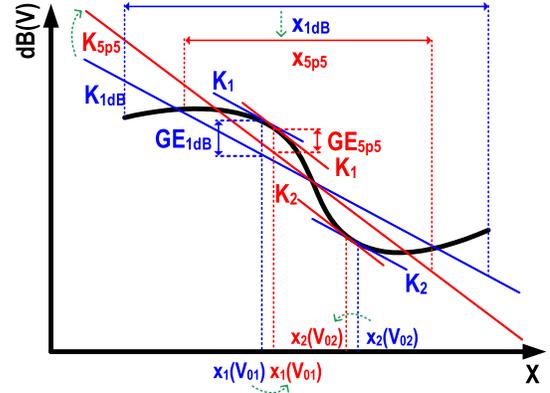


Fig. 3. Different gain errors versus x range.

TABLE II
COEFFICIENTS OF $G_n(x)$

Coefficient	$G_1(x)$	$G_2(x)$
A_n	1.8	-1.95
B_n	-1.15	-2.74
C_n	-1	1
D_n	0.64	8.73
E_n	-0.22	10.2
F_n	-0.37	7.6

approximation lines [dash lines in Fig. 2(d)], $K_1 = K_2$ must be satisfied. Given different requirements of gain errors, the slope of the ideal line varies, and the same goes with K_1 and K_2 , as shown in Fig. 3. If a more precise approximation is desired, the slope of these lines must be steeper while each approximation region is closer to the center. For instance, if the gain error is desired to be reduced from 1 dB to 5.5%, as quoted in Table I, the ideal line is rotated clockwise with its slope changed from K_{1dB} to K_{5p5} . The dual Taylor series approximation lines, therefore, must be altered accordingly (from blue to red as illustrated in Fig. 3), leading to a narrower deviation from the one-piece ideal line, as well as a reduction of maximum gain error from GE_{1dB} to GE_{5p5} . To achieve this movement, $x_1(V_{01})$ and $x_2(V_{02})$, at which points the Taylor series is expanded for each region, need to be moved towards the center, indicated by the arrow in Fig. 3.

To compare fairly with the prior exponential approximations in Table I, two equations (11) and (16) are normalized to (5). The two groups of the coefficients (A_1 to F_1) and (A_2 to F_2) in $G_1(x)$ and $G_2(x)$ are listed in Table II. To get the x ranges under the different gain errors, the shifting and scaling behaviors of $G_1(x)$ and $G_2(x)$ observed in Fig. 1 are repeated. We preset the gain error of $\leq 5.5\%$, with horizontal shift and vertical scale values ($\Delta X_1, \Delta Y_1$) and ($\Delta X_2, \Delta Y_2$) being (0.42, 4.117) and (0.44, 4.328), respectively. An overall x range of 2.27 (-1.15 to 1.12) is achieved (Table I). The movement values ($\Delta X_1, \Delta Y_1$) = (0.72, 7.257) and ($\Delta X_2, \Delta Y_2$) = (0.67, 6.807) will restrict the relative gain error at the origin

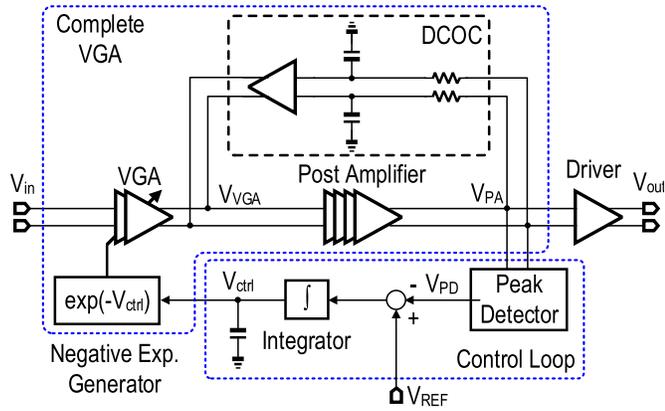


Fig. 4. Proposed complete AGC amplifier.

below 1 dB, and therefore yield an x range of 3.53 (−1.85 to 1.67) in Table I. Within a certain gain error, the available x range and dB-linear gain range are extended effectively due to the combination of the concave and convex functions.

IV. COMPLETE AGC AMPLIFIER

Figure 4 depicts the complete AGC amplifier including a feedforward VGA, a NEG and a feedback control loop. The VGA stage whose gain is controlled by a pre-distorted signal (V_{ctrl}) provides a constant output swing (V_{VGA}) for the following stages. The signal is then amplified to a desired amplitude by the post-amplifiers (PAs). Non-linearity and saturation must be minimized in order to fulfill the purpose of an AGC amplifier. The BW is another challenge of the PAs since any BW limitation brings inter-symbol interference and data-dependent jitter [17], [18]. A driver is built at the end of the AGC amplifier to drive the 50- Ω input impedance of the equipment.

The feedback control loop senses V_{PA} by a peak detector (PD), and compares its output (V_{PD}) with a predefined reference voltage (V_{REF}). The difference is then amplified and accumulated by the off-chip capacitor to generate the control voltage (V_{ctrl}), which is fed to the NEG to complete the loop. The charging and discharging process of the capacitor will only stop itself when the output of peak detector is identical to the reference voltage, leading to a constant output power regardless of the incoming signal strength.

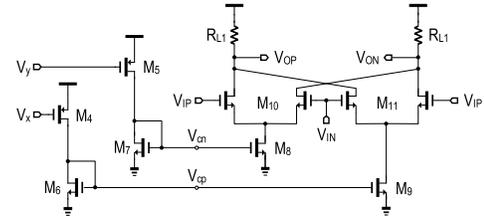
A. VGA

Figure 5(a) depicts the schematic of VGA which is connected to the NEG. A pseudo-folded Gilbert cell is introduced to further reduce the number of devices. Two single branches (M_4 - M_7) work as level shifters, transferring the exponential relationship from V_{yx} to ($V_{cpn} = V_{cp} - V_{cn}$), and then controlling the gain cell. Because all transistors work in the saturation region, we have

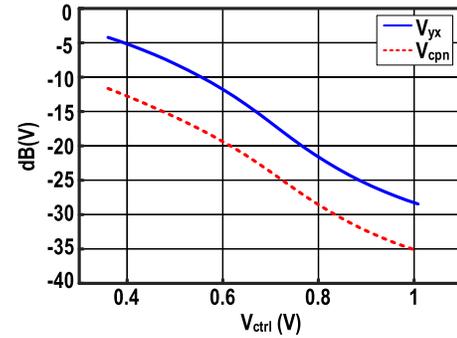
$$V_{cp,cn} = \sqrt{2I_{6,7}/K_{6,7}} + V_{th6,7} \quad (18)$$

where

$$I_{6,7} = I_{4,5} = \frac{1}{2}K_{4,5} (|V_{x,y} - V_{DD}| - |V_{th4,5}|)^2 \quad (19)$$



(a)



(b)

Fig. 5. (a) Pseudo-folded Gilbert cell. (b) The differential control voltages (V_{yx} and V_{cpn}) versus V_{ctrl} .

Since the two branches are identical to each other, it becomes

$$V_{cpn} = \sqrt{K_{4,5}/K_{6,7}}V_{yx} \quad (20)$$

If converted to the logarithm domain, i.e.

$$V_{cpn,dB} = 20 \log \sqrt{K_{4,5}/K_{6,7}} + V_{yx,dB} \quad (21)$$

which indicates that $V_{cpn,dB}$ persists a constant difference from $V_{yx,dB}$ and varies linearly with respect to V_{ctrl} in dB scale, as shown in Fig. 5(b).

The gain of the VGA cell is given by

$$A_v = -(g_{m10} - g_{m11})R_L \quad (22)$$

where

$$g_{m10,11} = \sqrt{\frac{1}{2}K_{10,11}K_{8,9}(V_{cn,cp} - V_{th8,9})} \quad (23)$$

Therefore,

$$A_v = \sqrt{\frac{1}{2}K_{10,11}K_{8,9}R_L V_{cpn}} \quad (24)$$

The above equation (24) proves a linear transfer between the voltage difference in the current tails and the differential gain of the VGA. From equations (20) and (24), it is obvious that the gain of the amplifier varies linearly with V_{yx} . Given that V_{yx} changes exponentially, the gain of the amplifier follows the same equation. Moreover, since small changes are observed in the total current of M_8 and M_9 , the impact on the output common-mode voltage is negligible even with the utilization of a pseudo-folded Gilbert cell. By cascading two identical gain cells, a doubled gain variation range of more than 40 dB could be achieved.

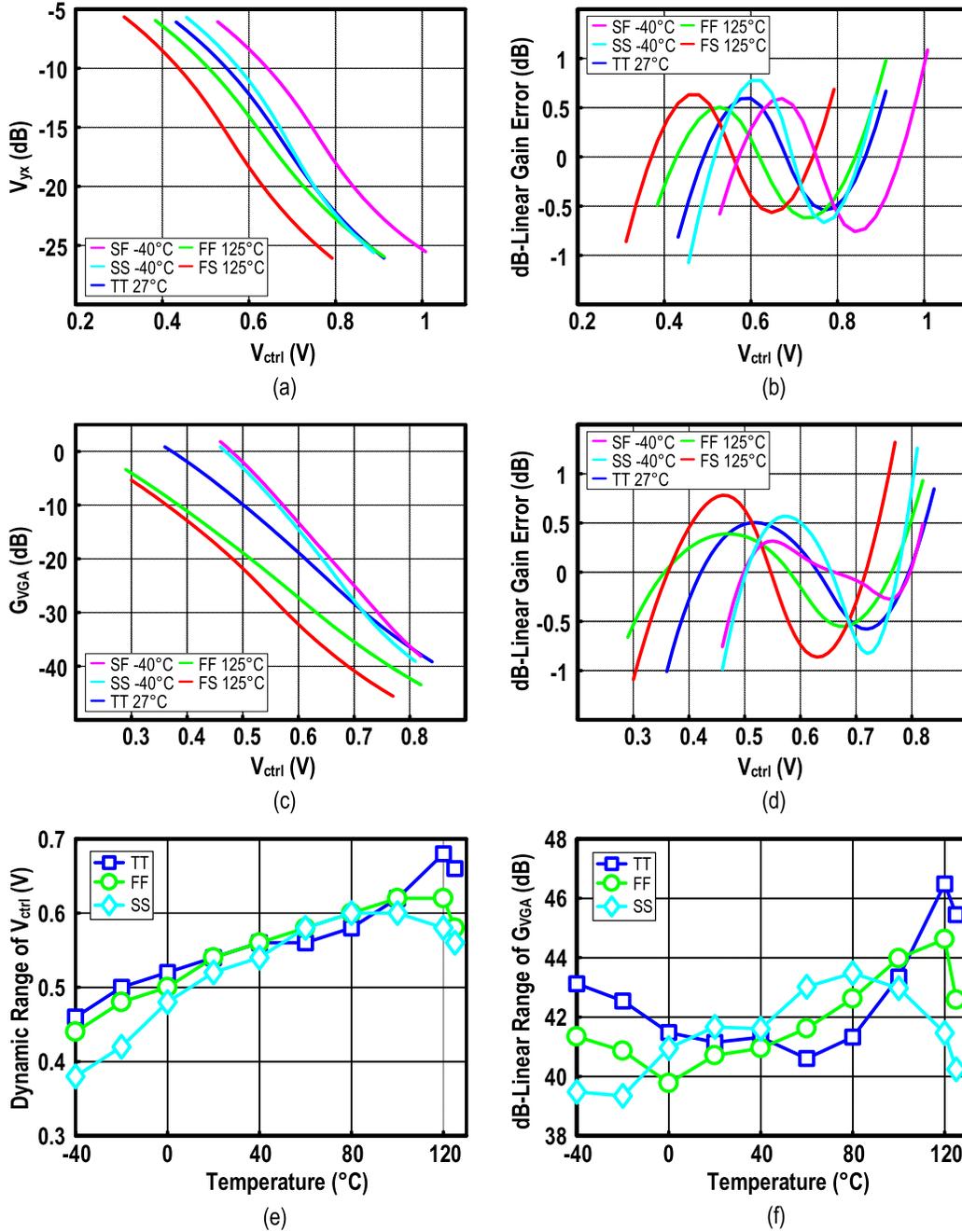


Fig. 6. Simulation results versus V_{ctrl} under different process corners and temperatures: (a) V_{yx} (V_{yx} in Fig. 2) showing dB-linearity, (b) gain error of (a), (c) G_{VGA} (at V_{VGA} in Fig. 4) showing dB-linearity and (d) gain error of (c). Simulation results versus temperature under different process corners: (e) dynamic range of V_{ctrl} and (f) dB-linear range of G_{VGA} with ± 1 dB gain error.

B. Post Amplifier (PA)

Since the VGA stage cannot provide an adequate gain without degrading its BW, the PAs are cascaded to raise the total gain by a fixed value under different gain settings. The PAs consist of eight identical cells as a compromise among gain, BW and power consumption. Each cell adopts a common-source amplifier with RC-degeneration. Capacitive degeneration helps increasing the effective transconductance (G_m) of the differential pair at high frequencies, to compensate the gain roll-off resulting from the pole at the output node, while the linearity of the amplifier is improved by resistive degeneration.

With the same effect on gain reduction as decreasing the load resistance, the input capacitance of a single cell is neutralized by the degenerated capacitor, thereby making cascading multiple stages possible. Furthermore, an active feedback topology is employed to enlarge BW. The feedback factor is chosen such that peaking is well controlled at high frequency range. DC-offset cancellation (DCOC) shown in Fig. 4 is implemented as a low-pass filter followed by a G_m stage, maintaining the lower cut-off frequency below 150 kHz to avoid any dc wandering. The overall PA consumes 20 mW of power and provides a gain of 23 dB up to 10 GHz.

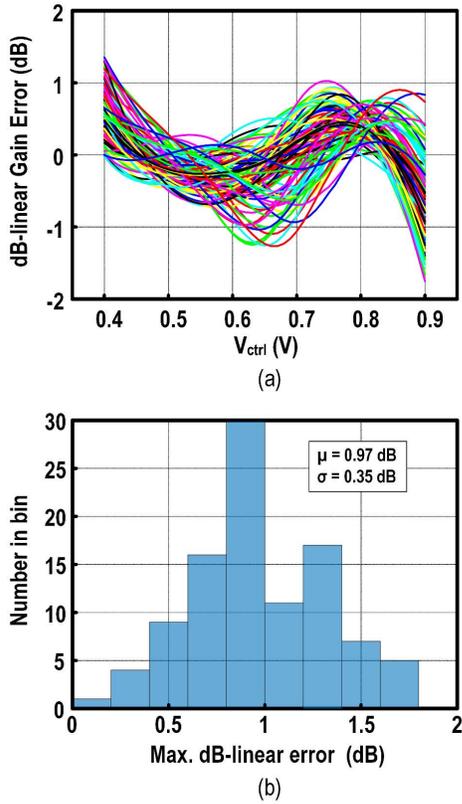


Fig. 7. Monte-Carlo simulation results versus V_{ctrl} : (a) gain error of V_{VGA} and (b) maximum dB-linear error histogram (100 Monte-Carlo simulation results).

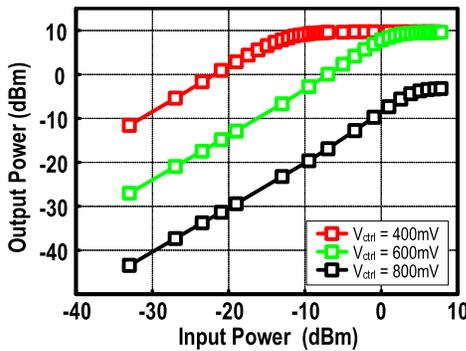


Fig. 8. Simulated compression behavior of the AGC amplifier under different V_{ctrl} . A data rate of 10-Gb/s $2^7 - 1$ PRBS signal is used as input.

C. Feedback Control Loop

To establish a feedback control voltage that forces the final output swing of the PAs equal to a fixed value, this output swing must be detected and monitored, thereby adjusting the gain of VGA accordingly. A source-coupled pair is utilized as a PD since its drain voltage increases almost linearly with the input swing. After smoothing by the low pass filter, V_{PD} is compared with V_{REF} , which is set according to the transfer characteristic of the PD. The difference is amplified by an integrator, leading to a charge or discharge of the capacitor. Cross-coupled regenerative load in the integrator is designed to reduce the comparison error and possess a fast transition.

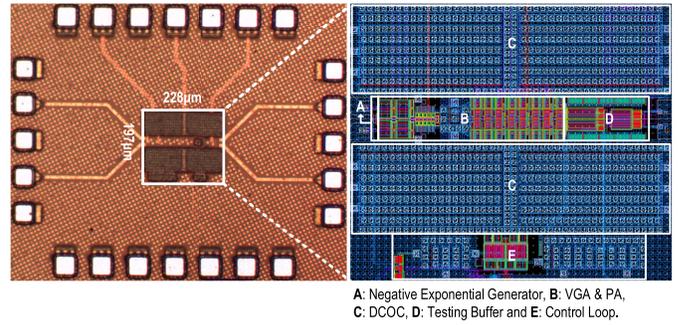


Fig. 9. Die photo of the AGC amplifier (left), and its zoomed-in layout (right).

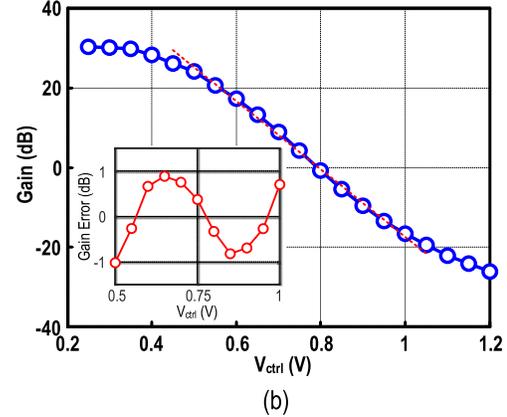
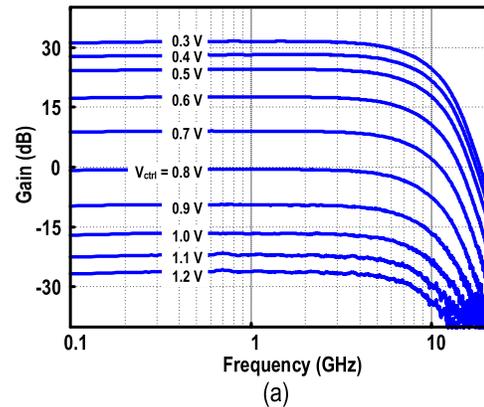


Fig. 10. (a) Measured frequency response of the VGA. (b) Measured gain and dB-linear error versus control voltage (V_{ctrl}) at 300 MHz in (a).

The capacitor accumulates the error until the output of PD is identical to V_{REF} , and stores the correct voltage to control the NEG.

D. Simulation Results

To evaluate the robustness of the NEG and VGA, their performance under various process corners and temperatures are simulated. By applying a properly-designed constant- G_m biasing to the bias transistor of the NEG, it is verified that the dB-linear characteristic is well maintained. Figs. 6(a) and (b) plot the simulated dB-linear performance and dB-linear gain error of the NEG, respectively, under typical condition and worst case scenarios. The same variation range from

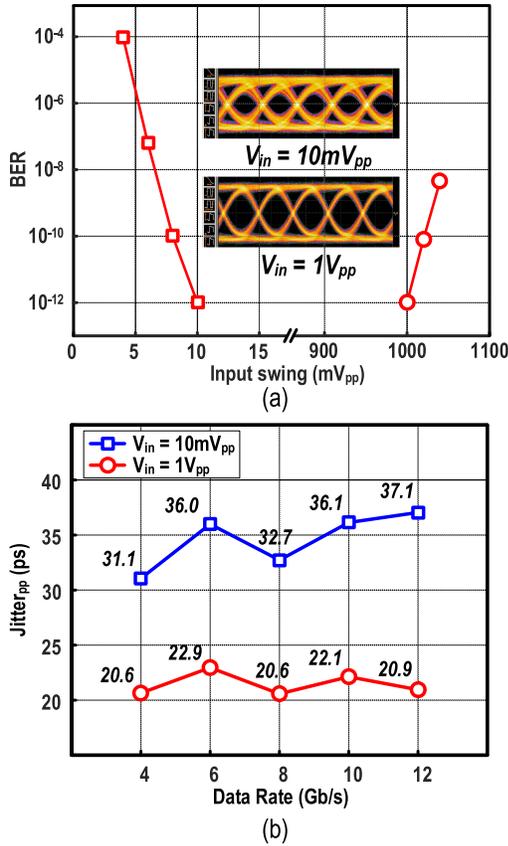


Fig. 11. (a) Measured BER versus input swing rate under 10-Gb/s, PRBS $2^7 - 1$ input. (b) Measured peak-to-peak jitter versus data.

–5.5 to –25.5 dB can be achieved with a shifted control range and the worst gain error is kept ~ 1 dB. Together with the VGA, the dB-linear gain characteristic (G_{VGA}) and gain error are plotted in Fig. 6(c) and (d), respectively, with the same operating conditions as the NEG. It is found that deviations exist among different scenarios, which may result from the variation of absolute gain provided by the Gilbert cells. Nevertheless, a dB-linear gain range of 40 dB is still achievable under all operating conditions, with a maximum gain error ~ 1.6 dB. It is worth to note that the inverse S-shape of the gain curves under different scenarios are well maintained, half of which are convex while the other half are concave. This can also be proven from the gain error curves, where three intercept points exist between each simulation line and its corresponding idea line, indicating the homogeneous effect on both region I and region II. Impacts on dynamic range of V_{ctrl} and dB-linear range of G_{VGA} over temperature ($^{\circ}C$) are plotted in Fig. 6(e) and (f). The deviations under different temperatures and process corners are within acceptable ranges.

Monte-Carlo simulation is conducted to further verify the effect of process variation and mismatch. Figs. 7(a) and (b) present the gain curves and maximum dB-linear gain errors distribution for 100 Monte-Carlo simulations, respectively. The standard deviation of the gain curves is found to be 1.55; the mean value of the maximum dB-linear gain error is 0.97 with a standard deviation of 0.35.

TABLE III
PERFORMANCE SUMMARY AND BENCHMARK
WITH THE STATE-OF-THE-ART

Parameters	This Work	JSSC'16 [9]	ISSCC'06 [4]
Technology	65nm CMOS	130nm CMOS	180nm CMOS
Data rate (Gb/s)	10	10	10
Inductors	No	No	Yes
Jitter (ps)	< 37.1	< 44	< 25
PRBS	2^7-1	$2^{31}-1$	2^7-1
BW (GHz)	0.0001 to 7.0	0.0001 to 5.0	N/A
In-band gain peaking (dB)	0	0	N/A
Exponential generator	Negative (e^{-x})	Positive (e^x)	Positive (e^x)
	Dual Taylor Series	Rational Approximation	Parasitic BJT
	3 MOSFETs	84 MOSFETs	3 MOSFETs + 2 BJTs + 2 Rs
Gain range (dB)	57 (-26 to 31)	40 (-15 to 25)	58 (-37 to 21)
dB-linear gain range / error	40 dB / ± 1 dB	40 dB / ± 1 dB	45 dB / ± 1 dB
AGC dynamic range at BER< 10^{-12}	40	24	35
Power (mW)	28	50	54
Energy efficiency	2.8 pJ/bit	5.0 pJ/bit	5.4 pJ/bit
Active area (mm ²)	0.045	0.4	1.32

The dynamic range of the AGC amplifier is determined not only by the gain variation range, but also the inband input-referred noise (IRN) and P_{1dB} . The IRN is found to be $4.26 \text{ nV}/\sqrt{\text{Hz}}$ when the overall gain is equal to 30 dB at $V_{ctrl} = 250 \text{ mV}$. The linearity of the AGC amplifier under different gain settings is studied by using pseudo-random binary sequence (PRBS) input in the time domain [18], as shown in Fig. 8. When the amplifier provides a high gain, saturation occurs at the output nodes. In contrast, input saturation occurs first when the gain is low and input signal is large. By choosing a moderate level of the desired V_{PD} , which is around -6 dBm in our case, an extended dynamic range can be achieved. As a result, linear amplification is provided over most of the operating range and the VGA acts as a limiting amplifier when saturated.

V. MEASUREMENT RESULTS

The complete AGC amplifier (Fig. 4) was fabricated in 65-nm CMOS. The die photograph (Fig. 9) shows a tiny active area of 0.045 mm^2 by avoiding any passive inductors. The prototype excluding the driver (Fig. 4) consumes 28 mW at 1.2 V. The frequency response [Fig. 10(a)] under various control voltages is measured by the Keysight Network Analyzer (N5247A), indicating a flat in-band gain and a constant 3-dB BW of $\sim 7 \text{ GHz}$. The total gain range is 57 dB (–26 to 31 dB). Fig. 10(b) shows that the dB-linear range is 40 dB, with ± 1 dB gain error when the control voltage V_{ctrl} is varied from 0.5 to 1 V. The measured gain error of the

inverse S-shaped curve is consistent with that of the calculated [Fig. 1(b)] and simulated [Fig. 2(e)] results.

The time-domain AGC closed-loop measurement was conducted using the Agilent Pattern Generator (J-BERT N4903B) and the Keysight real-time Oscilloscope (DSO91304-A). Fig. 11(a) plots the measured bit error rate (BER) for different input swings under a 10-Gb/s PRBS input of $2^7 - 1$. When the output swing of the overall PA is set at 300 mV_{pp}, the minimum input sensitivity and the input overload swing at BER of 10^{-12} are 10 mV_{pp} and 1 V_{pp}, respectively. Thus, the input dynamic range is 40 dB at BER of $<10^{-12}$. The measured peak-to-peak jitters [Fig. 11(b)] are <22.9 ps for 1 V_{pp} input swing, and <37.1 ps for 10 mV_{pp} input swing covering the data rate from 4 to 12 Gb/s, respectively.

Table III shows the performance summary and benchmarks this work with the similar prior works operating at the 10-Gb/s data rate [4], [7].

VI. CONCLUSIONS

A wideband inductorless dB-linear AGC amplifier with a novel technique to approximate the exponential function has been introduced. The architecture realizes multi-function approximation without any extra control circuitry such as switching circuits. The performance is verified by prototyping a 10-Gb/s AGC amplifier utilizing the proposed NEG as the VGA control. Fabricated in 65-nm CMOS, a dB-linear gain variation range of 40 dB is achieved, with an acceptable gain error of $< \pm 1$ dB, while the entire gain tuning range is up to 57 dB. The AGC provides a wide dynamic range of 40 dB, with a BER $<10^{-12}$ and a worst-case peak-to-peak jitter of 37.1 ps. Taking into consideration the high energy efficiency and small chip area, our AGC amplifier demonstrates its suitability for low-cost high-speed wireline applications.

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Lingshan Kong received the B.Eng. degree in electrical and electronic engineering from Nanyang Technological University, Singapore, in 2014, where she is currently pursuing the Ph.D. degree.

Her research interests are focused on analog baseband design and wireline backplane transceiver design.



Yong Chen (S'10–M'11) received the B.Eng. degree in electronic and information engineering from the Communication University of China, Beijing, China, in 2005, and the Ph.D. (Eng.) degree in microelectronics and solid-state electronics from the Institute of Microelectronics of Chinese Academy of Sciences, Beijing, in 2010.

From 2010 to 2013, he was a Post-Doctoral Researcher with the Institute of Microelectronics, Tsinghua University, Beijing. From 2013 to 2016, he was a Research Fellow with the Nanyang Technological University, Singapore, where he was responsible for high-speed (40+Gb/s) wireline communication and low energy electronic systems project under the Singapore–MIT Alliance for Research and Technology on RF CMOS transceiver in VIRTUS/EEE. He has been an Assistant Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China, since 2016.

His research interests include analog/biomedical detection and RF integrated circuit, mm-wave system and circuit, high-speed on-chip, and chip-to-chip electrical/optical interconnects.



Chirn Chye Boon (M'09–SM'10) received the B.E. degree (Hons.) and the Ph.D. degree in electrical engineering from Nanyang Technological University (NTU), Singapore, in 2000 and 2004, respectively.

He was with Advanced RFIC, NTU, as a Senior Engineer. Since 2005, he has been with NTU, where he is currently an Associate Professor. Since 2010, he has been the Program Director of RF and mm-wave research in the S\$50 million Research Center Of Excellence, VIRTUS, NTU. He is the Principal Investigator for Industry/Government Research Grants of S\$8,646,178.22. He has authored over 100 refereed publications in the fields of RF and mm-wave. He has authored the book *Design of CMOS RF Integrated Circuits and Systems*. He is involved in radio frequency and mm-wave circuits and systems design for biomedical and communications applications. He has conceptualized, designed, and silicon-verified 80 circuits/chips for biomedical and communication applications.

Dr. Boon was a recipient of the two-year Teaching Excellence Award and the Commendation Award for Excellent Teaching Performance from the School of Electrical and Electronic Engineering, NTU. He serves as a committee member for various conferences. He is an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS and a Golden Reviewer of the IEEE ELECTRON DEVICES LETTERS.



Pui-In Mak (S'00–M'08–SM'11) received the Ph.D. degree from University of Macau (UM), Macau, China, in 2006. He is currently a Full Professor with the Faculty of Science and Technology (ECE), UM, and an Associate Director (Research) with the State Key Laboratory of Analog and Mixed-Signal VLSI, UM. His research interests are on analog and radio-frequency circuits and systems for wireless and multidisciplinary innovations.

Dr. Mak was on the IEEE as an Editorial Board Member of the IEEE Press from 2014 to 2016, a member of Board-of-Governors of the IEEE Circuits and Systems Society from 2009 to 2011, a Senior Editor of the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS from 2014 to 2015, a Guest Editor of the IEEE RFIC VIRTUAL JOURNAL, in 2014, and the IEEE JOURNAL OF SOLID-STATE CIRCUITS, in 2018, and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I from 2010 to 2011 and from 2014 to 2015 and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 2010 to 2013. He was a Distinguished Lecturer of the IEEE Circuits and Systems Society from 2014 to 2015 and the IEEE Solid-State Circuits Society from 2017 to 2018. He was a TPC Vice Co-Chair of ASP-DAC 2016, a TPC Member of A-SSCC from 2013 to 2016. He has been a TPC Member of ESSCIRC since 2016 and ISSCC since 2016.

Dr. Mak co-received the DAC/ISSCC the Student Paper Award 2005, the CASS Outstanding Young Author Award 2010, the National Scientific and Technological Progress Award 2011, the Best Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II (2012–2013), the A-SSCC Distinguished Design Award in 2015, and the ISSCC Silkroad Award 2016. In 2005, he was a recipient of the Honorary Title of Value for scientific merits by the Macau Government.



Rui P. Martins (M'88–SM'99–F'08) was born in 1957. He received the bachelor's degree (five years), the master's, Ph.D. degrees, and the Habilitation degree for Full-Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively. He has been with the Department of Electrical and Computer Engineering, IST, TU of Lisbon, since 1980.

Since 1992, he has been on leave from IST, TU of Lisbon (now University of Lisbon since 2013), and also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he has been a Chair-Professor since 2013. In FST, he was the Dean of the Faculty from 1994 to 1997, where he has been a Vice-Rector of the University of Macau since 1997. From 2008, after the reform of the UM Charter, he was nominated after open international recruitment, and reappointed in 2013 as a Vice-Rector (Research) until 2018. Within the scope of his teaching and research activities he has taught 21 bachelor and master courses in UM, has supervised (or co-supervised) 40 theses, Ph.D. (19), master's (21), co-authored six books and nine book chapters, 18 patents, USA (16) and Taiwan (2), 377 papers, in scientific journals (111) and in conference proceedings (266), other 60 academic works, in a total of 470 publications. He was a Co-Founder of Chipidea Microelectronics, Macao (now Synopsys in 2001/2002, and in 2003, he created the Analog and Mixed-Signal VLSI Research Laboratory, UM, was elevated to State Key Laboratory of China in 2011 (the First in engineering in Macau), being its Founding Director.

Dr. Martins was a member of the IEEE CASS Fellow Evaluation Committee (2013 and 2014), a CAS Society Representative in the Nominating Committee, for the election in 2014, the Division I (CASS/EDS/SSCS), and the Director of the IEEE. He was a Nominations Committee Member in 2016. He was the Founding Chairman of the IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications from 2005 to 2008, the World Chapter of the Year of the IEEE CAS Society in 2009. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on CAS APCCAS 2008 and the Vice-President for Region ten (Asia, Australia, and the Pacific) of the IEEE CASS (2009–2011). Since 2011, he has been the Vice-President of (World) Regional Activities and Membership of the IEEE CASS (2012–2013), an Associate Editor of the IEEE TRANSACTIONS ON CAS II: Express Briefs (2010–2013), and nominated the Best Associate Editor of the IEEE TRANSACTIONS ON CAS II from 2012 to 2013. He was the recipient of two government decorations—the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference 2016. He is currently the Chair of the IEEE Fellow Evaluation Committee (class of 2018), both of IEEE CASS. In 2010, he was elected, unanimously, as a Corresponding Member of the Portuguese Academy of Sciences, in Lisbon, being the only Portuguese Academician living in Asia.