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1.2-V, 10-bit, 60–360 MS/s time-interleaved pipelined analog-to-digital converter in 0.18 μm CMOS with minimised supply headroom

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Abstract: A low-voltage 1.2-V, 10-bit, 60–360 MS/s six channels time-interleaved reset-opamp pipelined ADC is designed and implemented in a 0.18-μm CMOS ($V_{THN}/V_{THP} = 0.63$ V/−0.65 V for mid-supply floating switches). Without using on-chip high-voltage and low-V_T options, the proposed ADC employs low-voltage resistive-demultiplexing techniques, low-voltage gain-and-offset compensation, feedback current biasing to reduce the sensitivity of the bias current over process variations and current-mode sub-ADCs with static current sharing for a low-voltage time-interleaved implementation. Speed options of 60–360 MS/s are available with scalable power and they can be obtained by automatic selection of the number of time-interleaved channels. The chip measurement results show that the ADC exhibits a differential non-linearity (DNL)/integral non-linearity (INL) better than 0.9/1.2 LSB and a peak SNDR above 54 dB, for all speed options, while consuming 85 mW at 60 MS/s and 426 mW at 360 MS/s. The active die area is 13.2 mm^2.

1 Introduction

The continuous down-scaling of deep-submicron CMOS technology, as well as the demand for low-power battery-operated devices, imply even greater challenges on the design of low-voltage analog circuits. On the other hand, the implementation of high-speed switched-capacitor (SC) analog-to-digital converters (ADCs) becomes a harder task because of the need of floating switches [1–3]. To avoid using on-chip high voltages as well as special low-V_T options, reset-opamp techniques [1, 2] can be used in a low-voltage environment to achieve basic functions of SC circuits. However, low-voltage reset-opamp designs are still challenging, especially when the required supply voltage is lower than the nominal core voltage at a specific technology node [1–3] (e.g. 1.2 V at 0.18 μm CMOS for low-cost reasons) as imposed by low-power battery operated devices. The main difficulties encountered are related with reduced overdrive voltage (with severe speed penalties) and the design of low-voltage high-gain opamps [1, 4]. In addition, many useful special circuit techniques, such as double-sampling [5], opamp sharing [6] and correlated-double-sampling (CDS) [7], cannot be utilised because of the low-voltage floating switches.

The possibility of having switchable speed/power options in a single ADC design is also important for various applications that require varying speed, such as in multi-standard transceivers or in various video and imaging applications. This characteristic permits to obtain a good compromise in terms of speed-per-power over various speed requirements [8].

This paper proposes a 1.2 V, 10-bit, 60–360 MS/s time-interleaved reset-opamp pipelined ADC implemented in

0.18 μm CMOS technology ($V_{THN}/V_{THP} = 0.63$ V/ −0.65 V for mid-supply floating-switches) with metal–insulator–metal (MiM) capacitor option. The key features employed in the ADC include:

1. Six time-interleaved channels applying a 'front-end resistive-demultiplexing technique' implemented in a low-voltage environment.

2. 'Low-voltage gain-and-offset compensation techniques' to alleviate, simultaneously, the offset-mismatch among the time-interleaved channels, as well as the compensation of non-sufficient gain in a high-speed single-stage opamp and thus ensuring the linearity of the ADC.

3. Several speed options, namely 60, 120, 180, 240 and 360 MS/s with corresponding scaled power consumption obtained through the selection of different number of channels that can be either 1, 2, 3, 4 or 6, respectively.

4. 'Low-voltage current-mode sub-ADCs' that allow current-mirror sharing between the low-voltage comparators thus implying a reduction in static power consumption.

5. 'Feedback current biasing' that ensures the accuracy of the current source biasing over the process variations without the use of a cascode structure in low-voltage environment.

6. 'A programmable timing-skew insensitive clock generator' that alleviates the timing-mismatches among different channels and at the same time provides programmable multi-phase clocks for different speed options. Digital calibration usually reveals itself as a much more complex and costly solution to calibrate the dynamic timing-mismatches, especially in the 0.18 μm CMOS technology node.

All the techniques mentioned above are implemented without using any on-chip high-voltage or special low-V_T options to alleviate floating switch problems. On the other hand, they also exhibit a good potential to be applied in more advanced technology nodes (obtained through continuing deep-submicron CMOS down-scaling), as it is here clearly demonstrated, in particular by the very small headroom between the threshold and supply voltages.

The remaining of the paper is organised as follows: Section 2 presents the overall ADC architecture, with power-down structures that allow efficient speed/power scaling. Section 3 describes the key circuit techniques that allow the realisation of a low-voltage mismatch insensitive time-interleaved ADC. In Section 4 a detailed circuit implementation is presented and the corresponding measurement results are exhibited in Section 5. Finally, the conclusions are drawn in Section 6.

2 Overall ADC architecture

Fig. 1 shows the functional block diagram of the proposed ADC architecture that is composed by six time-interleaved channels. Each channel comprises a 60 MS/s pipelined ADC, as shown in Fig. 2, with a front-end sample-and-hold (S/H) and eight 1.5 b multiplying digital-to-analog converter (MDAC) stages, as well as a final 2 b flash ADC, like in typical 1.5 b/stage architectures. The structure includes built-in digital error correction [9] logic

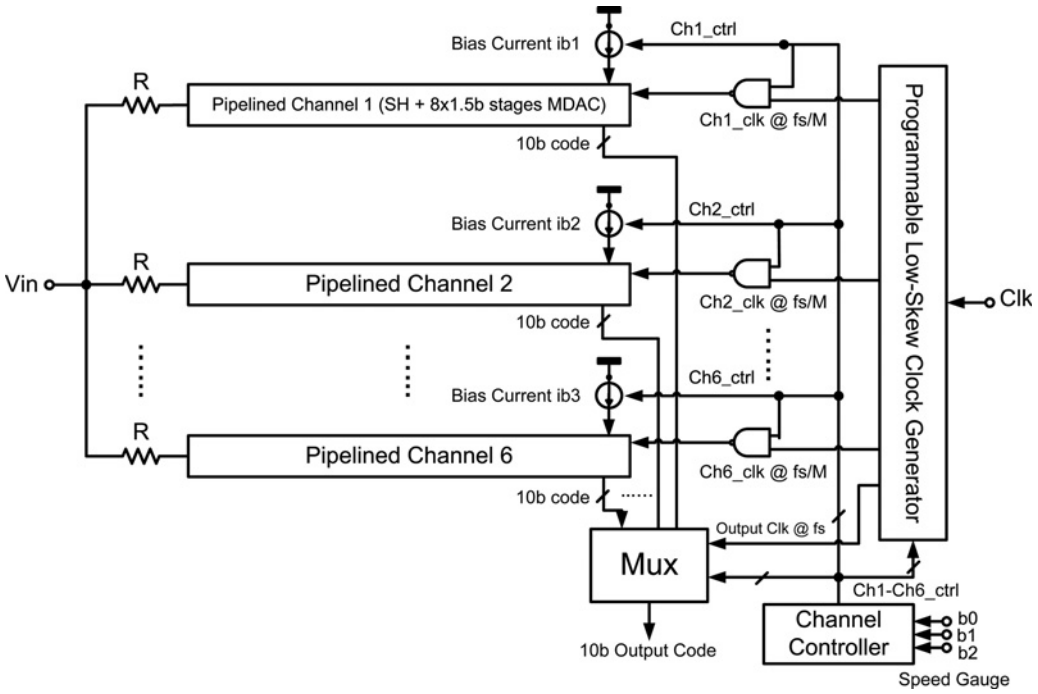

Figure 1 *Proposed six channels time-interleaved ADC architecture with speed-scalable options*

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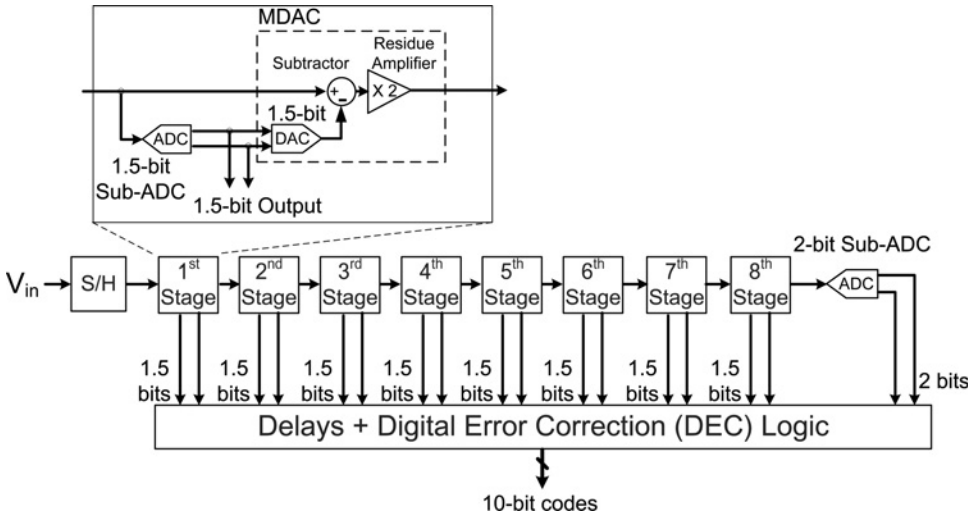

Figure 2 *Pipelined ADC architecture in one channel*

in each channel producing a 10 b digital code that can be eventually combined with the output digital multiplexer (Mux). To implement input demultiplexing in a low-voltage environment, a resistor R is used (before each channel) to interface with the input signal. This, associated with the crossed-coupled S/H (described in next section) will allow demultiplexing the input signal into each channel without signal feedthrough problems.

The power/speed scalable option is implemented by selectively powering-down the unused channels (by switching-off the biasing currents in the opamps) since in a time-interleaved ADC the overall conversion speed is proportional to the number of channels being used. As depicted in Fig. 1, a channel controller is used to activate/deactivate the bias currents of the opamps in various channels, and NAND gates are also utilised before the time-interleaved clocks arrive to the gates of the analog switches in each individual channel to avoid switching operation during power-down. The programmable clock generator (controlled by the channel controller) automatically provides the corresponding clock phases for different speed options, and the 10 b codes from various channels are combined in the final Mux to form a single set of 10 b output codes. The method described achieves very high-speed of operation with power/speed scaling options because of the high-speed nature of time-interleaved ADCs.

3 Proposed circuit techniques

3.1 Low-voltage resistive demultiplexing S/H with offset compensation

Time-interleaved techniques are difficult to be applied in low-voltage environments because of the inherent problems of floating switches [1–3]. Here, a resistive demultiplexing technique is proposed which, if combined with a crossed-coupled reset-opamp S/H [10], can provide input demultiplexing without direct signal-feedthrough problems, as illustrated in Fig. 3. $V_{cm} = 0.9$ V is the dc common-mode voltage for level shifting and the S/H is designed with output common-mode (in phase 2) at mid-supply. In phase 2 switches $S1$ form a voltage divider with resistor R to attenuate the input signal at nodes V_{x+} and V_{x-} and thus allow the discharge of capacitor C_1. However, signal-feedthrough is generated (although attenuated) which can be cancelled by the cross-connected capacitor C_2. As a result the input signal is decoupled between different channels thus allowing the demultiplexing operation. The value of the resistor should be chosen with enough suppression in the signal-feedthrough, but enlarging the resistor will also limit the bandwidth of the sampling front-end thus trade-offs on the resistor value must be made ($R = 1.6$ kΩ is used in this design). In addition, a low-voltage virtual-ground switched-capacitor common-mode feedback (SC-CMFB) technique is also used to alleviate the low-voltage CMFB problem without using any floating switches [4].

In time-interleaved ADCs offset-mismatch among various channels creates fixed offset tones at multiples of f_s/M, with f_s as the overall sampling rate and M as the number of channels [11]. Here, in the S/H a low-voltage offset compensation technique is proposed that is also embedded in the circuit of Fig. 3. To obtain an S/H gain of 1 it would be necessary to have $C_1 = C_2 = C_3 = C$. In phase 1 C_2 is connected between the virtual grounds (V_{g+} and V_{g-} in Fig. 3) in the reset mode, thus equivalently sampling $2V_{OS}$ into C_2, where V_{OS} is the opamp offset voltage. A charge conservation equation (differential) can be written in phase 2

$$C_1\left[(V_{in}[\phi 1] - 0) - \left(\frac{R_{on}}{R + R_{on}} V_{in}[\phi 2] - V_{OS}\right)\right] + C_2\left[(-V_{OS} - V_{OS}) - \left(-\frac{R_{on}}{R + R_{on}} V_{in}[\phi 2] - V_{OS}\right)\right] + C_3[0 - (V_{out}[\phi 2] - V_{OS})] = 0$$

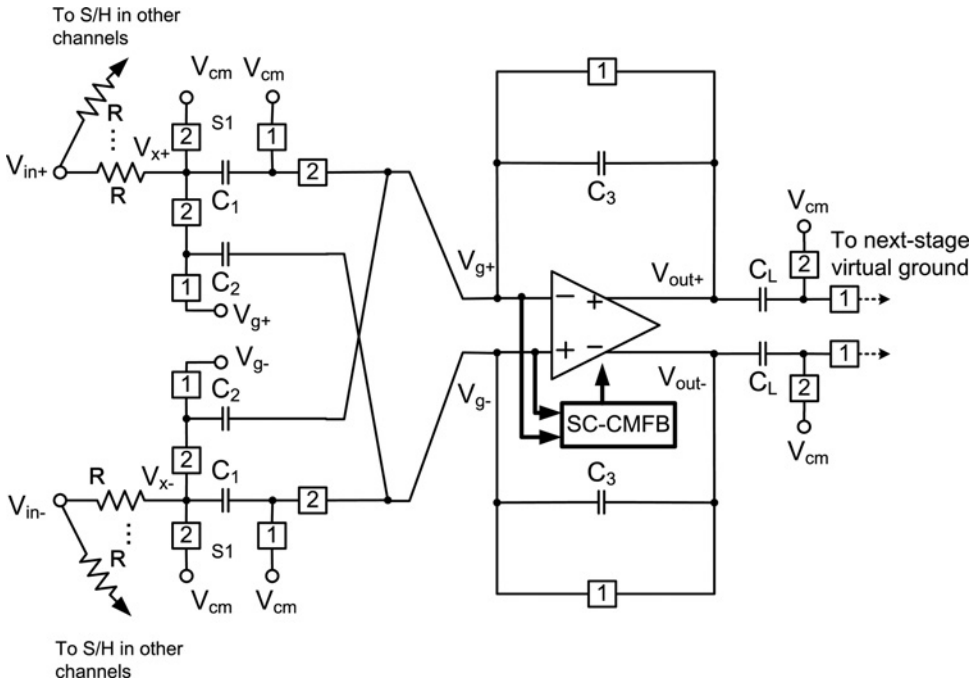

Figure 3 *Offset-compensated crossed-coupled S/H with resistive front-end demultiplexing*

leading to

$$V_{\text{out}}[\phi 2] = V_{\text{in}}[\phi 1] + V_{\text{OS}} \quad (1)$$

However, as derived from the operation of the reset-opamp circuit, the S/H will be reset (to V_{OS}) in phase 1, implying that the charge package discharged to the next-stage virtual ground can be expressed as

$$\Delta q = C_{\text{L}}\{(V_{\text{in}}[\phi 1] + V_{\text{OS}}) - V_{\text{OS}}\} = C_{\text{L}} V_{\text{in}}[\phi 1] \quad (2)$$

showing that the opamp offset voltage is compensated without the use of any floating switches.

3.2 Low-voltage gain-and-offset compensated MDAC

In low-voltage designs the opamps are mainly restricted to traditional two-stage architectures [1, 4] (because of the impossibility of using cascode devices), which by their nature exhibit lower speed (because of the additional high-impedance node needing Miller compensation) and higher power consumption (more current branches). On the other hand, using single-stage opamps with low gain can cause non-linearities in the whole pipelined ADCs. In this design, low-voltage finite-gain compensation is applied [12], thus allowing the utilisation of high-speed single stage opamp in a low-voltage environment, as shown in Fig. 4 (which is an improved version of the technique from [12] by adding a novel offset-compensation scheme as discussed next). It uses an auxiliary amplifier to sense the virtual ground gain-error voltage and then feeding it to the output in order to correct the gain error, without using floating switches (*S*1 is not a floating switch because there is only a small voltage swing presented in the auxiliary amplifier output since this amplifier only processes the gain error from the main amplifier). The effective gain has been boosted by the compensation scheme from A_1 to $\beta A_1 A_2$, where β is the feedback factor ($\beta = 0.2$ in this design and equal in both amplifiers).

For the MDAC of Fig. 4 the reference injection is achieved from the voltage supply by capacitive division $C_{\text{ref}}/C_{\text{f1}}$ and it is split into two branches for codes 10/00 and code 01, respectively, to handle effectively the different common-mode level-shifting requirements of different codes. $V_{\text{cm1}} = 0.3$ V is used as a common-mode voltage injection for code 01 and the differential reference voltage is solely determined by the capacitive division from the supply voltage (which is heavily decoupled by the on-chip decoupling capacitor) as it will be shown in (3) in the next paragraph.

In addition to the gain-compensation also an offset-compensation scheme is proposed in the MDAC to suppress the offset error generated simultaneously by the main and auxiliary amplifiers (shown in Fig. 4). If V_{OS1} and V_{OS2} are the offset of the main and auxiliary amplifiers, respectively, then the main amplifier holds (considering only differential voltages)

$$C_{\text{s1}}[(V_{\text{in}}[\phi 1] - 0) - (0 - V_{\text{OS1}})] + C_{\text{ref}}[(0 - 0) - (mV_{\text{DD}} - V_{\text{OS1}})] + C_{\text{f1}}[0 - (V_{\text{o1}}[\phi 2] - V_{\text{OS1}})] = 0$$

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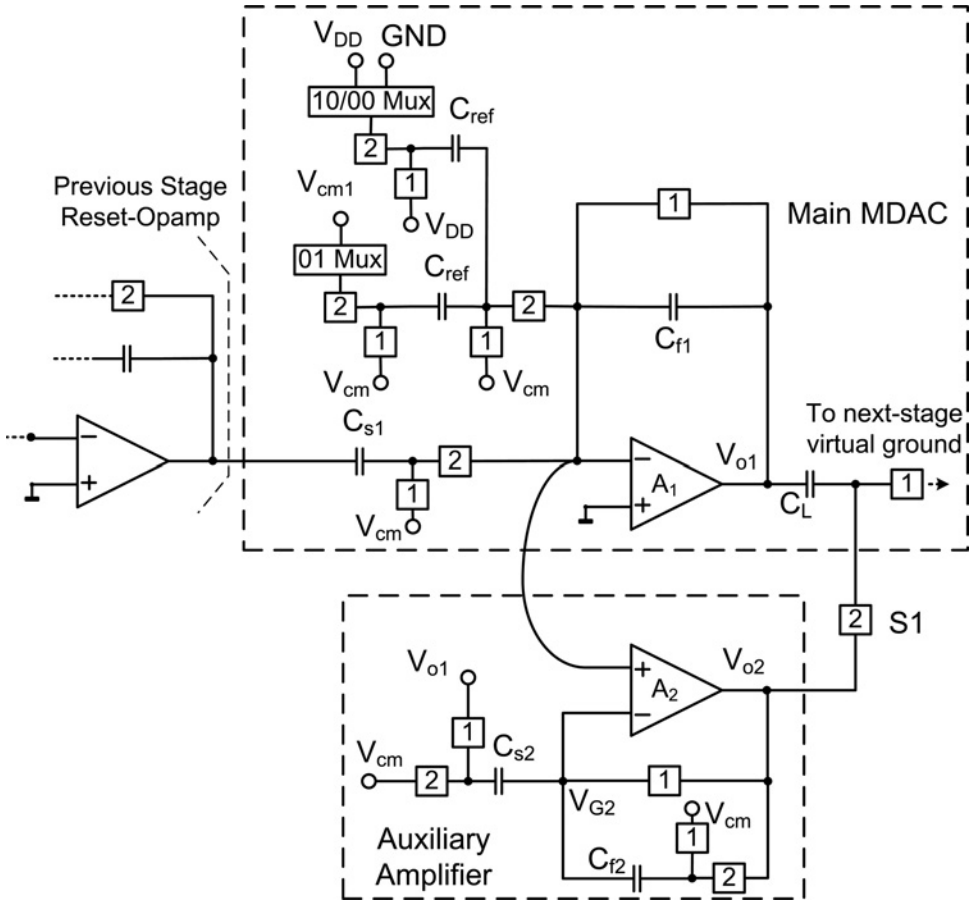

Figure 4 *Low-voltage gain- and offset-compensated MDAC*

that leads to

$$V_{o1}[\phi 2] = \frac{C_{s1}}{C_{f1}} V_{in}[\phi 1] - \frac{C_{ref}}{C_{f1}} mV_{DD} + \frac{C_{s1} + C_{ref} + C_{f1}}{C_{f1}} V_{OS1} \quad (3)$$

where $m = -1, 0, 1$ depends on the sub-ADC decision. Besides, the auxiliary amplifier will process both offsets from the main and the auxiliary amplifiers as follows (with the voltage at the negative terminal of A_2 as $V_{OS1} + V_{OS2}$)

$$C_{s2}\{[(V_{OS1} - (V_{OS1} + V_{OS2})] - [0 - (V_{OS1} + V_{OS2})]\} + C_{f2}\{[(0 - (V_{OS1} + V_{OS2})] - [V_{o2}[\phi 2] - (V_{OS1} + V_{OS2})]\} = 0$$

which can be represented by

$$V_{o2}[\phi 2] = \frac{C_{s2}}{C_{f2}} V_{OS1} \quad (4)$$

For gain compensation, with the same feedback factor in both amplifiers, the following holds

$$\frac{C_{s1} + C_{ref}}{C_{f1}} = \frac{C_{s2}}{C_{f2}} \quad (5)$$

Finally, by combining (3)–(5), the voltage stored in the capacitor C_L during phase 2 can be expressed as

$$(V_{o1} - V_{o2})[\phi 2] = \frac{C_{s1}}{C_{f1}} V_{in}[\phi 1] - \frac{C_{ref}}{C_{f1}} mV_{DD} + V_{OS1} \quad (6)$$

Again the main MDAC will be reset to V_{OS1} in phase 1 to discharge C_L resulting in an offset-free charge transferred to the next stage.

3.3 Feedback current biasing

Fig. 5 shows the circuit diagram of the main opamp, which is implemented in single-stage current-mirror topology for high-speed. On the other hand, to implement the auxiliary amplifier a four-terminal differential-difference opamp should be used in fully differential architecture since the signal is processed by both input terminals of A_2. Fig. 6 shows the current-mirror differential-difference opamp (with two differential-pairs) used in the auxiliary amplifier with symbol and circuit schematic presented in Figs. 6*a* and *b*, respectively. Both the main and auxiliary opamps have dc gains of 49 dB only.

Fig. 5 also presented the proposed feedback current biasing, which can also be applied in the auxiliary differential-difference amplifier. For correct operation the

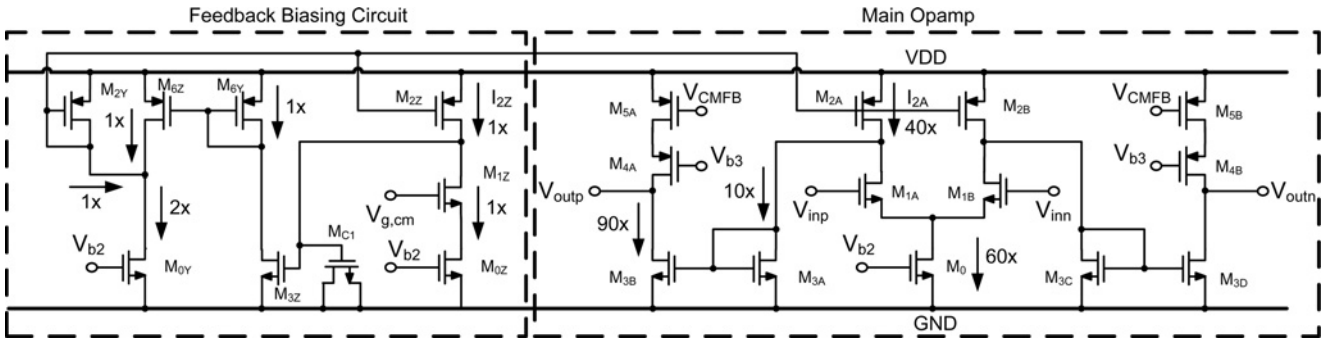

Figure 5 *Current mirror opamps with feedback current biasing*

bias current of M_{3A} is provided by currents' subtraction between M_{2A} and M_{1A}. The bias current of M_{1A} is provided by the tail current source M_0, which can have larger channel length to achieve accurate current matching over process variations (because it is not in the signal path). The channel length of M_{2A} cannot be too large, since the drain junction capacitance of M_{2A} is in the main signal path and the phase margin will be degraded by this parasitic capacitance. This capacitance can be comparable to the gate capacitance of M_{3A} since M_{2A} is a PMOS transistor with large current handling capability. On the other hand, using a smaller channel length in M_{2A} will imply large current spread over process corners because of the channel length modulation effect from the variation of the gate-source voltage V_{GS} in M_{3A}, and as a result it will impose a very large current variation in M_{3A} and the output-stage transistor M_{3B} which could affect the slew rate of the opamp.

This difficulty can be overcome by the proposed biasing circuit in Fig. 5. The biasing circuit will simulate the operating point of the main opamps, that is M_{xZ}, M_{xY} are the corresponding scaled down versions of M_x, $M_{x\mathrm{A}}$–$M_{x\mathrm{D}}$ in the main opamp (e.g. M_{3Z} is a scaled-down version of M_{3A} to M_{3D}). Fig. 5 also exhibits the current relationship allowing a better understanding on how to set the current in the various branches, as well as the W/L ratio of various transistors. The feedback loop composed by M_{3Z}, M_{6Y}, M_{6Z}, M_{2Y} and M_{2Z} ensures identical drain voltages in M_{2Z} and M_{2A}. Since their drain voltages are identical, the current matching between them is accurate over process variations even with small transistor lengths. On the other hand, choosing larger channel lengths for M_{0Z} and M_0 also allows accurate matching between them. Now, since the currents through M_{2Z} and M_{0Z} are identical, this technique guarantees closely tracked currents between M_{2A} and M_{1A}, then minimising M_{3A}'s current variation under small channel length (0.25 μm in this design).

To ensure that the feedback loop is negative, an additional current mirror pair M_{6Y} and M_{6Z} has been added. This feedback loop is a unity-gain feedback and the gain-bandwidth product of the loop gain can be calculated as

$$\mathrm{GBW} = \frac{(W/L)_{6Z}}{(W/L)_{6Y}} \cdot \frac{(W/L)_{2Z}}{(W/L)_{2Y}} g_{m,3Z}/(C_{\mathrm{gs},3Z} + C_{\mathrm{gs,MC1}}) \quad (7)$$

considering that the drain parasitics are not dominant in the biasing circuit. In addition, there are two non-dominant poles

$$p_1 = g_{m,2Y}/(C_{\mathrm{gs},2Y} + C_{\mathrm{gs},2Z} + C_{\mathrm{gs},2A} + C_{\mathrm{gs},2B}) \quad (8)$$

$$p_2 = g_{m,6Y}/(C_{\mathrm{gs},6Y} + C_{\mathrm{gs},6Z}) \quad (9)$$

Due to the large gate capacitance of the transistors M_{2A} and M_{2B} in the main opamp, $p_1 \ll p_2$ and the first non-dominant pole p_1 severely degrades the phase margin of the loop. A large NMOS capacitor M_{C1} is thus added at the gate of M_{3Z} to stabilise the feedback loop.

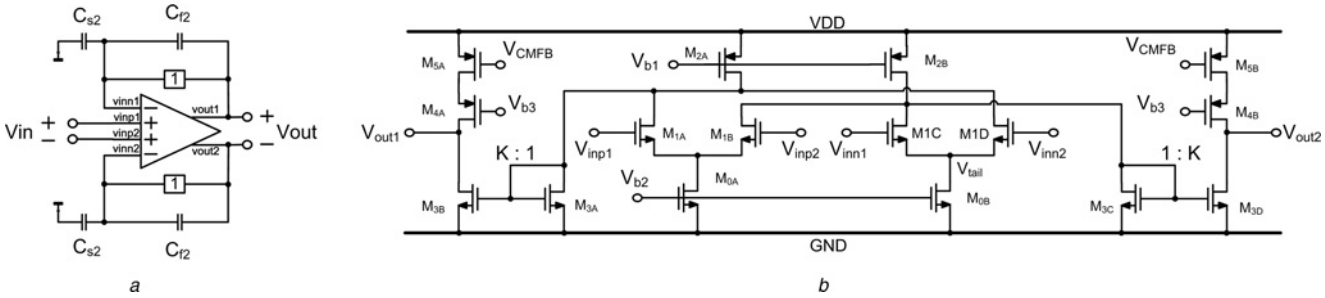

Figure 6 *The Auxiliary Differential-Difference opamp*

a Symbol
b The circuit implementation in *a*

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Table 1 Comparison of conventional biasing scheme over the feedback current biasing techinque

	Case 1	Case 2	Case 3
	Conventional biasing		Proposed
channel length of M2A/B, μm	0.25	0.75	0.25
output-stage current variation	±17%	±3.6%	±1.6%
gain-bandwidth product (ss), GHz	1.35	1.47	1.35
phase margin at phase 2 (ss)	59°	44°	59°

To verify the effectiveness of the technique, simulations have been done for the auxiliary differential-difference amplifier used in the first MDAC. AC analysis shows that the biasing loop achieves an open-loop gain of 27 dB, GBW of 5.4 MHz and phase-margin of 80°. Moreover, corner simulations are performed and the results are shown in three cases, in Table 1. For the first two cases, M_{2A} and M_{2B} are biased using conventional simple current mirror (without cascode), these two cases clearly show the trade-off between the output-stage current (and thus slew-rate) variations and the phase-margin through the selection of channel length of $M_{2A/B}$. Using longer channel length can ensure lesser output-stage current variations (17%–3.6%), with the cost of the reduced phase margin in the main opamp (59°–44°). The last case shows that the proposed technique can achieve simultaneously improved phase margin (59°) and reduced process variations (1.6% only, even better than Case 2).

3.4 Low-voltage current-mode sub-ADC

The 1.5 b sub-ADC contains two comparators whereas the final 2 b sub-ADC contains three. Conventional voltage-mode differential pair architectures cannot be used in low-voltage designs because of large voltage swing and input common-mode range. Also, SC comparators cannot be utilised because of the floating switches. A current-mode comparator [13] will be adopted here based on its low-voltage operation capability and adjustable threshold. It will also exhibit very low kick-back noise from the latch since it is shielded in two steps by the current-mirror and the input resistors. However, because of the operation in current-mode the comparators will draw static power in the current mirrors. To reduce the static power a low-voltage current-mode sub-ADC architecture is proposed, as shown in Fig. 7 in its 2 b version, to share the static current mirror in the sub-ADC. The current mirror voltages V_{binp} and V_{binn} are generated from the input signal V_{inp} and V_{inn}, and on the other hand V_{brefp} and V_{brefn} are generated from the supply rails to produce reference voltages for the comparators. These mirror nodes can be shared among three comparators (Fig. 7) since two of three comparators have identical thresholds with different polarities ($+/-0.5V_{ref}$ comparator thresholds as required in 2 b stages), whereas the zero-reference comparator does not require reference voltages. The zero-crossing points of the

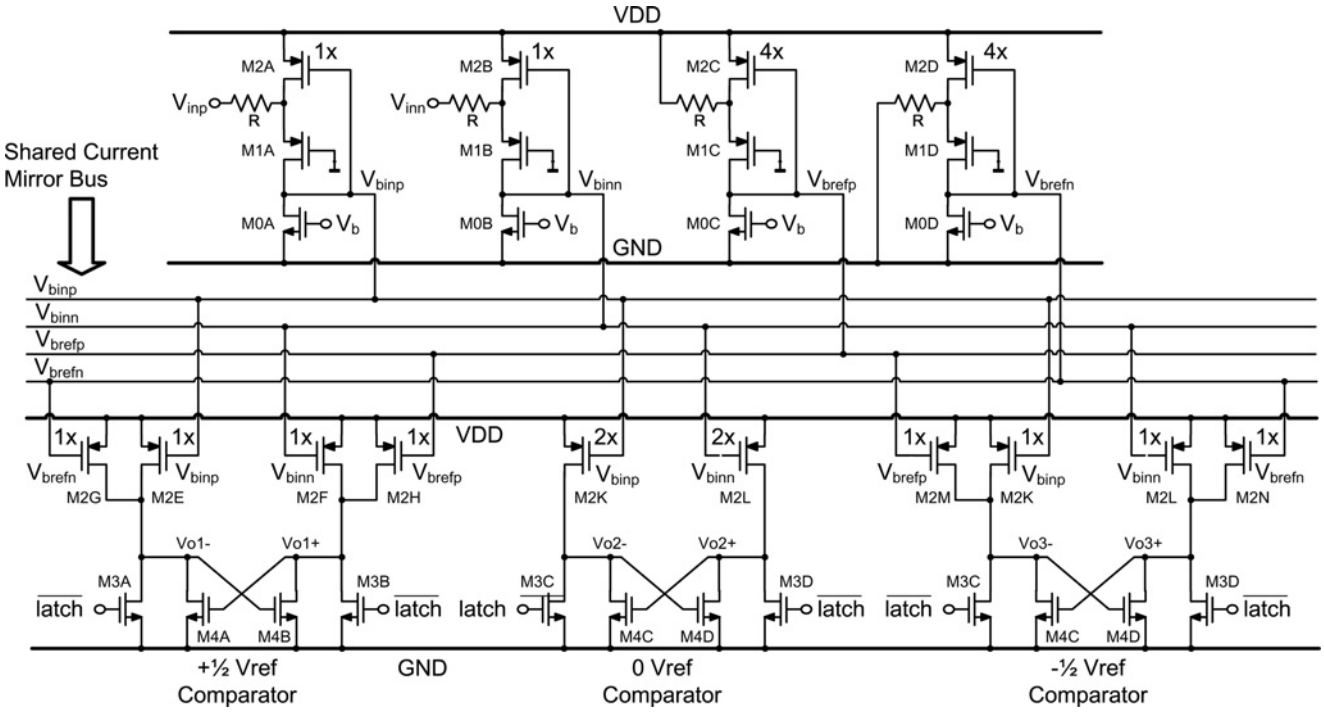

Figure 7 *Low-voltage current-mode 2 b sub-ADC architecture*

$+/-0.5V_{ref}$ comparators are defined as follows

$$V_{inp} - V_{inn} = \pm\frac{1}{4}V_{DD} = \pm\frac{1}{2}V_{ref} \quad (10)$$

The offset of the comparators are easily within the specifications because of the large offset tolerance of the last 2 b flash in 1.5 b/stage. Finally, the 1.5 b sub-ADC exhibits a similar technique with different current mirror ratios for different threshold voltages. In terms of power each 1.5 b sub-ADC consumes 300 μW whereas the whole 2 b sub-ADC draws 600 μW.

4 Detailed circuit implementation

The ADC was fabricated in 0.18 μm CMOS technology with MiM capacitor options. To save power no auxiliary amplifier (and thus no gain-compensation) is used in the S/H as shown in Fig. 3, whereas auxiliary amplifiers are used (Fig. 4) in the first five stages of MDAC to compensate the finite-gain error. This leads to only a larger static gain-error (with an opamp gain of 38 dB) in the pipelined ADC. Such error can be tolerated if only the single-channel pipelined ADC is used. However, mismatches in the DC gains of the opamps among various channels will create static gain-mismatch tones which will degrade the dynamic performance of the ADC. Since the mismatches are static they can be easily calibrated through DSP post-processing. For testing purposes the static gain-mismatches are calibrated using a software method similar to that used in [14]. Also, no offset calibration is performed to verify the proposed offset compensation schemes.

Besides offset- and gain-mismatches, sampling-time mismatches in various time-interleaved channels also create modulated sidebands which will degrade the performance of the ADC [15]. A low-skew clock generator (shown in Fig. 8) is used here to reduce the sensitivity because of the timing-skew effect, which relies on assigning the common master Pre-clk signal for the decision of the sampling instant. This is a modified version from [16] that provides correct clock phases for speed scaling options in which some of the D-flip-flops in the ring counter are bypassed depending on the channel controller output (Fig. 8).

Fig. 9 shows the chip's microphotograph of the whole converter, including the six channels of pipelined ADCs, clock generator, Mux and decimator. The layout of various channels was arranged such that, for example channels 2 and 5 share the same clock bus because they require the

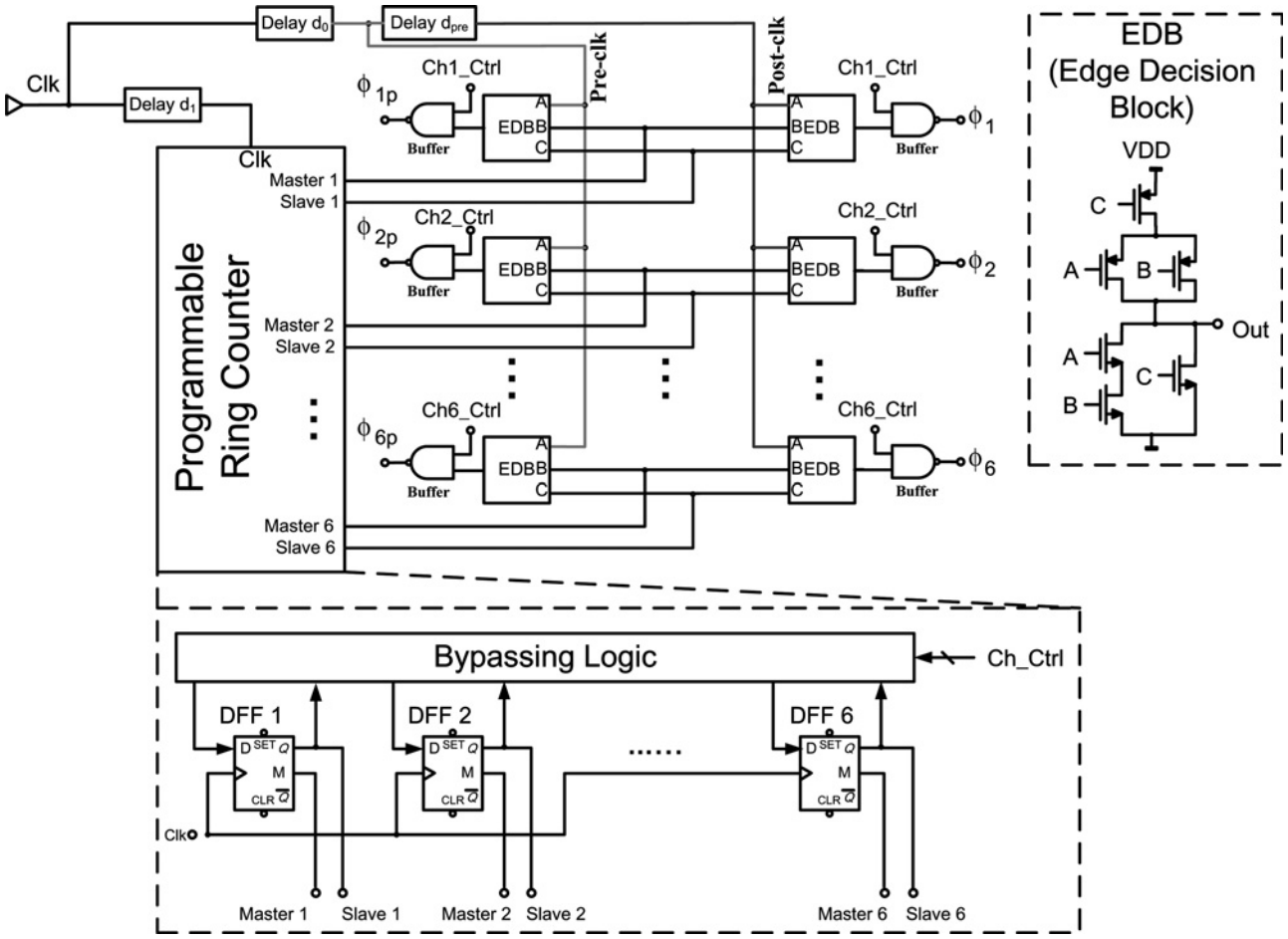

Figure 8 *Programmable low-skew clock generator*

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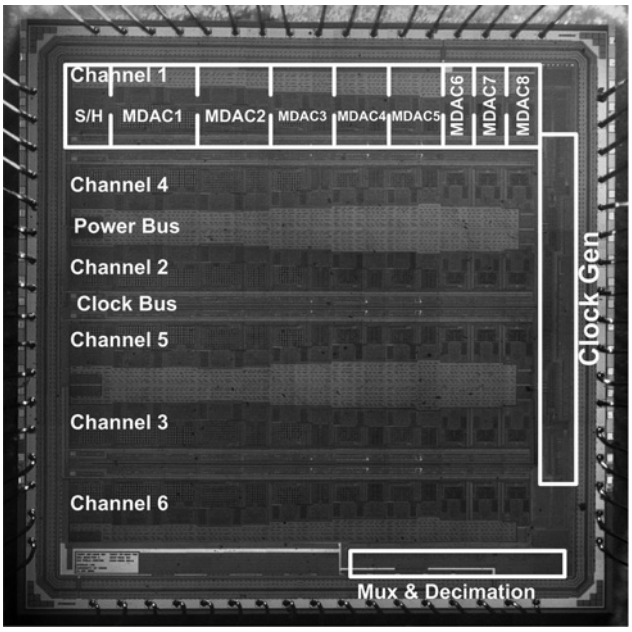

Figure 9 *Chip's microphotograph*

same set of non-overlapping clocks. On chip decoupling MOSCAPs are used to fill in all the unused space to heavily decouple V_{DD} and V_{cm}. The active area is 13.2 mm^2 and it is dominated by the large capacitance value required to suppress the contribution of thermal noise in a low-voltage environment, as well as the large area requirement of the opamps because of the very small overdrive voltage headroom. The capacitors are scaled down along the pipelined, and the areas for the MDAC1/MDAC8 are 0.33 mm^2/0.1 mm^2.

The chip was packaged in a 68-pin CQFP package. The digital output codes are obtained through the standard CMOS I/O drivers. With the highest data rate (360 MHz) the bondwire inductances on the driver and I/O supply pins create supply noise in the I/O supply domain, and affect the quiet analog domain through resistive substrate coupling. To avoid degradation of performance because of I/O supply noise, output data decimation had been used to down-sample the ADC output data for testing purposes only. The decimator's downsampling factors are 1 (i.e. no decimation) and 5 (obtained from a divided-by-5 ring counter). The selection of 5 as downsampling factor avoids a common factor between it and the number of time-interleaved channels (i.e. 1, 2, 3, 4 and 6), such that the decimated data correctly samples all the data points from all channels.

5 Measurement results

The performances of all channel options were measured and are summarised in Table 2. Static performance such as differential non-linearity (DNL) and integral non-linearity (INL) are measured using the traditional sine-wave histogram method [17]. Fig. 10 shows the DNL/INL profile of the ADC with six-channels (360 MS/s) and the results of all other speed options can be compared in Table 2 also. The DNL/INL are both within 0.9/1.2 LSB for all speed options and they are not significantly degraded with the increasing number of time-interleaved channels, since time-interleaving only produces mismatch-type non-idealities that do not affect ADC's static linearity.

Table 2 Performance summary of the ADC

technology	0.18 μm CMOS (*V*THN/*V*THP = 0.63/−0.65 V)				
nominal core voltage, V	1.8				
resolution, b	10				
ADC core area	13.2 mm^2 (2.2 mm^2/channel)				
supply voltage, V	1.2				
full-scale input range	1.2 Vpp differential				
no. of channels	1	2	3	4	6
sampling rate, MS/s	60	120	180	240	360
ADC core power, mW	85.2	144	232	287	426
DNL (LSB)	+0.7/−0.7	+0.9/−0.7	+0.8/−0.7	+0.7/−0.6	+0.8/−0.6
INL (LSB)	+1.2/−1	+0.9/−1	+0.8/−1	+1/−1	+0.7/−1
SNDR at f_{in} = 25.1 MHz, dB	55	54.8	54	54.5	54
ENOB at f_{in} = 25.1 MHz	8.9	8.8	8.7	8.8	8.7
SFDR at f_{in} = 25.1 MHz, dB	72	69	65	68	65
THD at f_{in} = 25.1 MHz, dB	−68	−66	−67	−67	−60

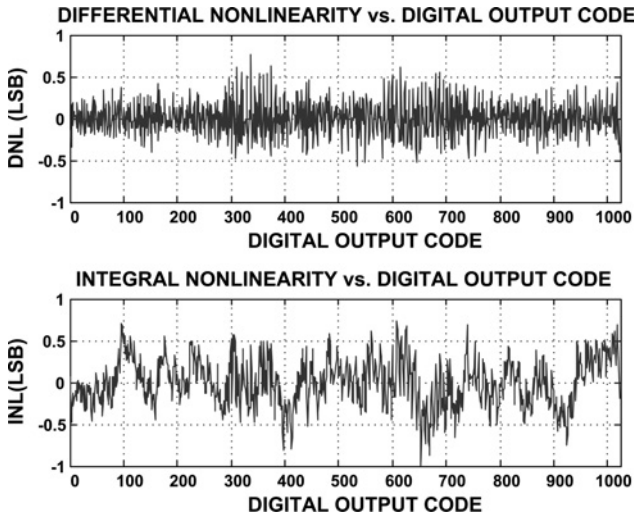

Figure 10 *Measured DNL and INL of the ADC (six channels)*

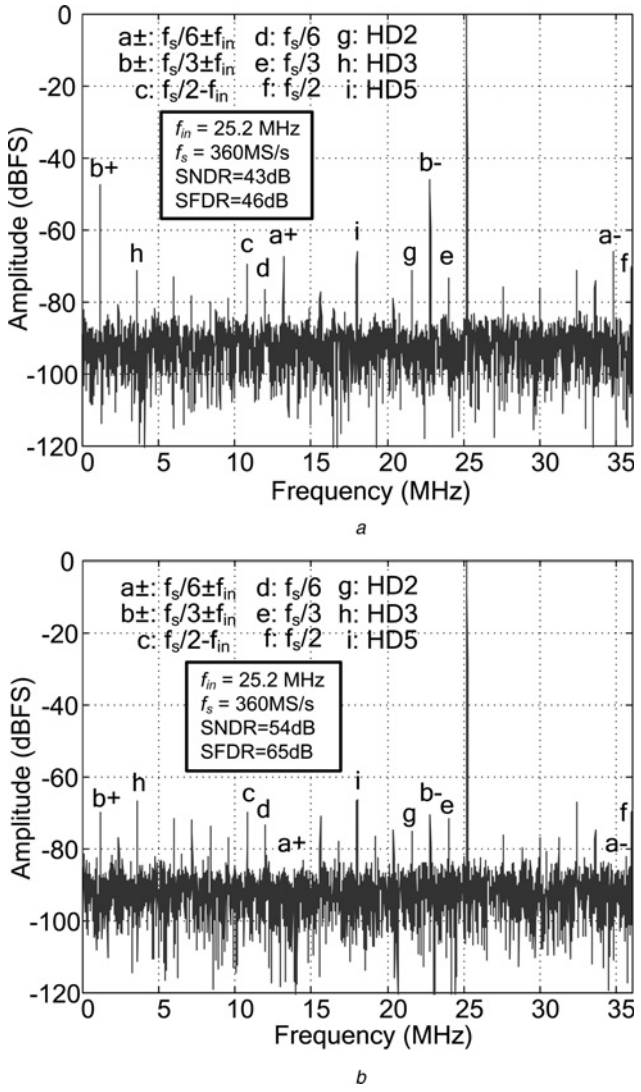

Figure 11 *Measured output spectrum (at $f_s = 360$ MS/s)*

a Without gain mismatch calibration
b With gain mismatch calibration

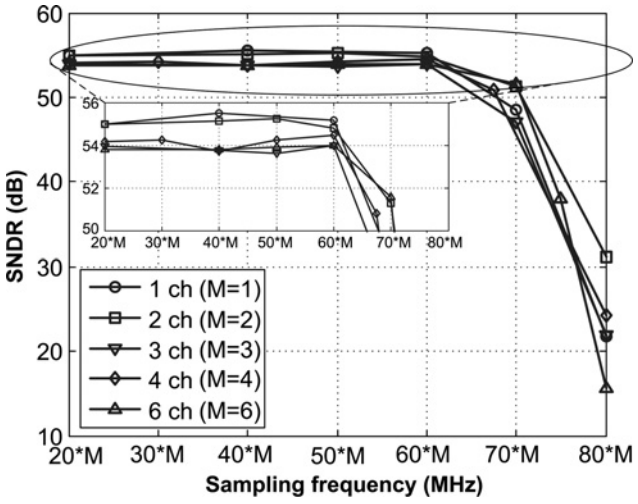

Figure 12 *Plot of SNDR against sampling frequency per channel for all speed options ($f_{in} = 25.1$ MHz)*

Fig. 11 shows the FFT output spectrum of the ADC with sampling frequency $f_s = 360$ MS/s (six channels with a decimation factor of 5) and input frequency $f_{in} = 25.2$ MHz, with and without static gain-mismatch calibration. With calibration the SNDR improves from 43 to 54 dB. The gain-mismatch tones are located at 60 ± 25.2 MHz, 120 ± 25.2 MHz and $180 - 25.2$ MHz, which correspond to 34.8, 85.2, 94.8, 145.2 and 154.8 MHz, respectively. These tones are mapped (and aliased) into the frequencies of 34.8, 13.2, 22.8, 1.2 and 10.8 MHz, respectively, after decimation. Actually, from the ADC's layout (Fig. 9) the channel pairs (1, 4), (2, 5) and (3, 6) are arranged in close proximity to simplify the routing of the clock signals, and as a result the mismatch within a pair is minimised. Consequently, the output spectrum equivalently contains a mismatch pattern that repeats with a period of $3/f_s$, as can be retained from Fig. 11*a* where the most prominent modulation sidebands appear at the frequencies of 120 ± 25.2 MHz before

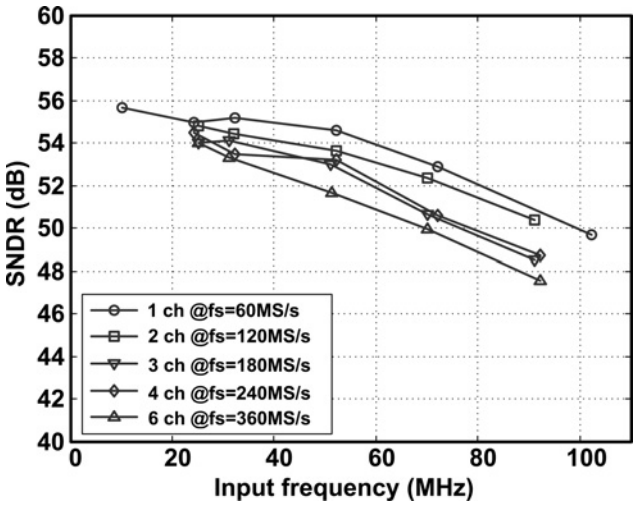

Figure 13 *Plot of SNDR against f_{in} for all speed options ($f_s = 60$ MS/s per channel)*

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Table 3 Performance benchmark with state-of-the-art designs

	This work	[2]	[18]	[19]	[20]	[21]	[8]
technology	0.18 μm CMOS (nominal supply = 1.8 V)						
resolution, b	10	12	8	10	8	8	10
supply voltage, V	1.2	0.9	1	1.8	1.8	1.8	1.8
supply voltage (% of nominal), %	67	50	56	100	100	100	100
full-scale input range, Vpp	1.2	0.5	0.5	1	1.6	0.8	1.6
power/speed scalability	yes	no	no	no	no	no	yes
sampling rate, MS/s	360	5	100	100	150	1.6	50
ADC core power, mW	426	12	30	67	71	774	35
SNDR, dB	54	50	41.5	54	46.8	47.5	55
ENOB	8.7	8	6.6	8.7	7.5	7.6	8.8
FOM (power × VDD/[2ENOB × f_s] pJ.V/conversion step)	3.4	8.4	3.1	2.9	4.7	4.5	2.8

calibration. A simple mathematical deduction that confirms this result is provided in the Appendix. The offset cancellation mechanisms described in Section 3 are also verified by the low offset induced tones at 12, 24 and 36 MHz (60, 120 and 180 MHz before decimation), as illustrated by Fig. 11*b*.

The ADC was also tested in all other speed options in various sampling frequencies. Fig. 12 shows a plot of SNDR against sampling frequency with $f_{in} = 25.1$ MHz. The ADC maintains an SNDR greater than 54 dB (with 8.7 effective-number-of-bit – ENOB) for all speed options up to 60 MS/s per channel. At higher sampling frequencies the settling errors in the MDACs limit the ADC's performance. Fig. 13 shows a plot of SNDR against input frequency at $f_s = 60$ MS/s per channel, which shows that the ADC has an effective resolution bandwidth greater than 66 MHz.

Table 2 summarises the performance of the ADC, showing that the power consumption is linearly scaled with the number of active channels and the power/speed ratio remains approximately constant. The ADC consumes 85.2 mW at 60 MS/s and 426 mW at 360 MS/s. A benchmark of this work with state-of-the-art 8–12 bit designs, within the same technology node, can be extracted from Table 3. The figure-of-merit is defined as follows [22, 23]

$$\text{FOM2} = \frac{\text{power}}{2^{\text{ENOB}} \cdot f_s} V_{\text{DD}} \tag{11}$$

to better reflect the performance of low-voltage designs, since the supply voltage has been lowered the challenge in the optimisation of ADC's performance is vastly increased because of: (i) the limited overdrive voltages of opamps and switches; (ii) the impossibility of applying many special circuit techniques because of the absence of floating switches; (iii) the fact that thermal noise does not decrease with the lowering of the voltage supply. The implemented ADC achieves a FOM of 3.4 pJ·V/step, which is comparable with several 1.8-V designs (i.e. with nominal supply) from Table 3. Low-voltage ADCs (e.g. [2, 18] from Table 3) can not achieve the best performance when compared with nominal-supply designs, indicating a vastly large reduction in different performance characteristics basically inherited from the lower voltage. Table 3 also highlights key features of the proposed ADC, namely: (i) power/speed scalability; (ii) only 67% usage of nominal supply voltage (indicating large headroom for future CMOS technology scaling); (iii) advantages in full-scale input range; (iv) very high-speed of operation with medium resolution.

6 Conclusions

A 1.2 V, 10 b, 60–360 MS/s speed scalable time-interleaved reset-opamp pipelined ADC is presented in 0.18Υμm CMOS. By selectively activating the clocks and bias currents in various channels this ADC features built-in 60, 120, 180, 240 and 360 MS/s speed options. Reset-opamps are used to avoid floating switches and a resistive demultiplexing technique is proposed in the front-end S/H to demultiplex the input to various time-interleaved channels. To alleviate channel mismatches low-voltage offset-and-gain compensation techniques are also proposed for the S/H and MDAC and a feedback current biasing technique is presented to obtain a process-insensitive current biasing of the opamps. Finally, a low-voltage current-mode sub-ADC is presented to reduce the static power consumption in the low-voltage comparators, and also a programming timing-skew-insensitive clock generator is designed to alleviate timing-mismatches. Under the low-voltage environment (1.2 V at 0.18 μm) without on-chip high-voltage or bootstrapped switches, as well as special circuit techniques (e.g. double-sampling or opamp sharing), the ADC exhibits 54 dB SNDR over all

speed options. Moreover, all the proposed techniques are highly scalable and applicable in advanced low-voltage deep-submicron CMOS, as it can be anticipated by the need of a mere 67% of nominal supply voltage.

7 Acknowledgments

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9 Appendix: special case in static gain mismatch

This appendix provides the proof to the observed phenomena measured in the six-channel un-calibrated output spectrum because of a special case of static gain-mismatch highlighted in Section 5. In its general form the output spectrum of the time-interleaved ADC with a sinusoidal input signal under static gain-mismatch can be represented as follows [11]

$$G(\omega) = \frac{1}{T}\sum_{k=-\infty}^{\infty} A(k)\cdot j\pi \times \left[\delta\left(\omega+\omega_{\text{in}}-k\frac{2\pi}{MT}\right)-\delta\left(\omega-\omega_{\text{in}}-k\frac{2\pi}{MT}\right)\right] \tag{12}$$

where

$$A(k) = \frac{1}{M}\sum_{m=0}^{M-1} a_m e^{-jkm(2\pi/M)} \tag{13}$$

are the relative weights of kth modulation sidebands, $G(\omega)$ is the output spectrum, $\omega_{\text{in}} = 2\pi f_{\text{in}}$ is the input angular frequency, M is the number of time-interleaved channels (assuming an even number in this design), $T = 1/f_s$ is the reciprocal of the overall sampling frequency and a_m ($m = 0, 1, \ldots, M-1$) is the static gain in channel m. Under special layout conditions (illustrated in Fig. 9) it can be assumed that

$$a_m = a_{M/2+m} \tag{14}$$

since the static gain mismatch is minimised between the channels in close proximity (for those sharing the same clock buses). The weights in (13) can then be expressed as

$$\begin{aligned} A(k) &= \frac{1}{M}\sum_{m=0}^{M/2-1} a_m\left[e^{-jkm(2\pi/M)} + e^{-jk(M/2+m)2\pi/M}\right] \\ &= \frac{2}{M}\cos\left(\frac{k\pi}{2}\right)e^{jk\pi/2}\sum_{m=0}^{M/2-1} a_m e^{jk\pi/2}e^{-jkm(2\pi/M)} \end{aligned} \tag{15}$$

which is non-zero only for even value of k. If $M = 6$ then $A(k) \neq 0$ for only $k = 0$ (the signal components) and $k = 2$ (the 120 MHz $\pm f_{\text{in}}$ modulation sidebands), which confirms the results reported in Section 5. Also, the component at $k = 4$ is the image component of that of $k = 2$.