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Ambient RF energy harvesting system: a review on integrated circuit design

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Abstract

This paper presents a comprehensive review of ambient RF energy harvester circuitry working on integrated circuits. The review covers 3 main blocks in an RF energy harvesting system implemented on chip. The blocks are the rectifier, impedance matching circuit and power management unit. The review of each block includes its operational principle, reported state-of-the-art circuit enhancement techniques, and design trade-offs. We compare the circuits in each block with respect to the techniques adopted to improve the performances for RF energy harvesting. To identify the benefits and limitations associated with the architecture we discuss the advantages and disadvantages of the circuit topologies in each block of an ambient RF energy harvester.

Keywords Ambient RF energy harvesting · Integrated circuit · Rectifier · Impedance matching network · Power management unit

1 Introduction

Ambient Radio Frequency (RF) energy is an alternative power source in urban and suburban environment for low-power devices such as Wireless Sensor Nodes (WSNs) enabling the Internet of Things (IoT) [1, 2]. The use of wireless communication devices such as mobile phones, tablets and laptops increases the amount of propagated wireless power in a free space environment providing a new source of energy that could be harvested. Ambient RF energy is the residue of the propagated signal from wireless devices during the transmission of electromagnetic information between the devices and communication stations. Measurement and studies have been carried out in various cities and environments to identify the feasibility of utilizing ambient RF energy as an alternative energy source [2–7]. Through the survey undertaken, the density of the measured RF energy level shows promising potential in harvesting the ambient RF energy for low-power devices.

These residues of ambient RF energy constitute a feasible energy source for WSNs in which sensor nodes are deployed in large scale for monitoring applications such as in healthcare [8–11], environment monitoring in smart cities [12, 13], industrial manufacturing [14, 15] and

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biological applications such as detecting pollination patterns of bumblebees [16]. The ability to harvest ambient RF energy provides an alternative and new energy source in charging up the sensor node where battery lifespan is a huge bottleneck in large scale deployment due to the physical size, reliability and maintenance constraint of using Li-ion batteries.

Designing ambient RF energy harvesters using discrete electronics and in a solution of system-on-a-chip (SoC) is still a challenge due to discordancy between the low-power density nature of the RF energy and the threshold voltage (V_{th}) of the transistors (which is the minimum voltage to turn on the transistor); limiting the power conversion efficiency (PCE) of the rectifier. There have been reviews on the scope of ambient RF energy harvesting in the perspective of its design and challenges [17–19] but much of the reviews are highly focused on discrete electronics when compared with integration on chip. This paper seeks to direct the research and development initiatives of ambient RF energy harvesting towards IC integration through system analysis. It is our intention to fill the gap of SoC RF harvesting realization which outlays a comprehensive literature review on ambient RF energy harvesting focusing on IC integration for application such as WSNs.

We derive the review of each block from the harvester consisting of a rectifier, the impedance matching network (IMN) and the power management unit (PMU) to design an improved ambient RF harvesting for low-power devices. Section 2 reviews the general scope of the concept in RF energy harvesting. Sections 3, 4 and 5 analyse and review the rectifier, the IMN and the PMU, respectively. Section 6 provides additional information of other aspects that contributes to the development and performance enhancement of RF energy harvesting. Section 7 draws the conclusions.

2 IC design of RF energy harvester

RF energy harvesting is the concept of scavenging the electromagnetic waves that are propagated in a free space medium and converting them to usable electrical energy for powering up electronic devices or sensor interfaces. RF energy harvesting can be distinctly divided into two types based on the method and density of the RF power, which are the near-field and far-field. Near-field RF energy harvesting (RFEH) which is usually termed as wireless power transfer (WPT) harvests or transfers energy through magnetic-coupling or magnetic resonance of two inductors or antenna coils placed near to each other [20–33]. The RF frequency of the near-field is usually lower with higher power density when compared to the far-field. The near-field RFEH is very much focused towards biomedical application [20, 22, 23, 25, 26, 29, 31] and battery charging [30] in line with the higher density of RF power being harvested.

The far-field RFEH on the other hand is the harvesting of ambient RF energy through a receiving antenna where the RF energy scavenged could be from a dedicated source or residue energy from communication signals in the propagated medium [34]. Unlike certain electronic devices that require constant power, WSN requires very low amount of energy abstaining from constant power and allowing ambient RF energy as a suitable energy source for such devices. Far-field RFEH would be the scope of interest in this review. For simplicity, RFEH will be referred as ambient RF energy harvesting since we only consider far-field RFEH systems reported in IC design.

Figure 1 shows the typical integration of the blocks in the RFEH system. The study of the receiver antenna will be phased out as this review focuses on the circuit elements only. The operation of the system starts at the antenna where it captures the RF energy from the propagated medium. The power received (P_R) at the antenna can be calculated based on Friis free space transmission in (1) [35, 36] given by:

$$P_R = P_T G_R \frac{\lambda^2}{(4\pi R)^2} \tag{1}$$

where P_T is the transmitted RF power signal that is captured by the antenna, G_R is the gain of the receiving antenna, λ is the wavelength of the radio frequency which is the velocity of the wave divided by its frequency and R is the distance of the system from a transmitted RF source. The ac voltage generated by the antenna can be determined by (2) [37, 38]:

$$V_{ANT} = \sqrt{8 \times R_{ANT} \times P_R} \tag{2}$$

where V_{ANT} is the peak input voltage swing at the antenna, R_{ANT} is the radiation resistance of the antenna and P_R is the received power similar in (1).

As the antenna captures the RF power (P_{in}), the signal propagates into the IMN which matches the impedance of the antenna and the load (the impedance seen into the RFEH system) providing maximum power transfer. Still in ac form, the RF power from the IMN will be rectified through the rectifier. The PMU regulates or stores the dc power and we design it to ensure that the converted power

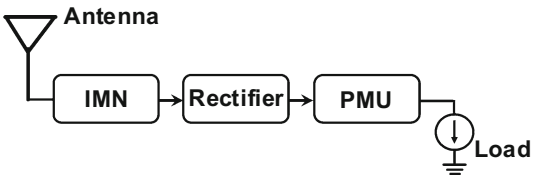


Fig. 1 Typical block in an ambient RFEH system

(P_{out}) is suitable to be sourced to the load. Figure 2 shows the power flow of an RFEH system with the expression for evaluation of the overall system performance denoted by:

$$\eta_{system} = \frac{P_{output,dc}}{P_{input,RF}} = \eta_{IMN} \times \eta_{Rect} \times \eta_{PMU} \quad (3)$$

where η_{system} is the overall efficiency of the system, η_{IMN} is the efficiency of the IMN circuit, η_{Rect} is the efficiency of the rectifier and η_{PMU} is the efficiency of the PMU based on the amount of power the unit consumes. The performance of the system is evaluated mainly by its efficiency in converting the input RF power and its sensitivity which is the lowest input RF power level for the system to start the scavenging process.

3 Rectifier for RF energy harvesting

The rectifier is the main block in an RFEH system which is responsible for converting the harvested input RF energy to a usable electrical output. There are two main rectifier topologies that are widely used for ambient RF energy harvesting. The topologies are the Dickson-type [39–59] and the Cross-Coupled Differential-Drive (CCDD) [34, 60–72] topology. Both topologies differ in the manner how the rectification process is performed but similar performance indicators are used, namely, the PCE and sensitivity. The PCE measures how efficient the harvested power is converted from ac to dc which is determined by the equation:

$$PCE_{Rect} = \frac{P_{out,dc}}{P_{in,RF}} \quad (4)$$

Alternatively, the expression for the sensitivity, P_{dBm} is given by:

$$P_{\mathrm{dBm}} = 10\log_{10}(P_{mW}) \quad (5)$$

The sensitivity is evaluated in dBm as the RF power received is in the range of milli or micro-watts. As RF energy harvesting is an emerging topic, a review of the rectifier topologies overlaps with applications such as in Radio Frequency Identification (RFID) and RF transducers. Though the reported circuits are not of the same application, the rectifier circuits from these applications are well suited for the RFEH system as the work executes the same function with the same performance indicators. This opens up an avenue where the performance of the rectifier design for ambient RFEH in application such as the WSN can be compared due to the similarities in the harvesting level of the input RF power and scavenging frequency.

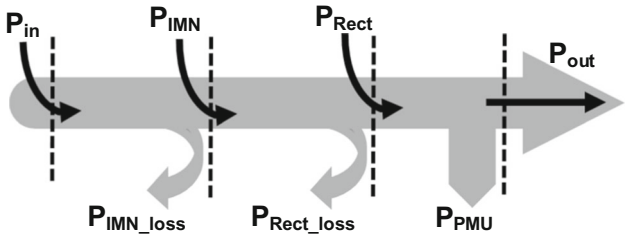


Fig. 2 Power flow of RF harvested energy

The Dickson-type topology was introduced by [39] in a monolithic form on an IC derived from the discrete Cockcroft-Walton voltage multiplier (VM) circuit. It was implemented as a high voltage generator for memory writing and erasing for Transistor–Transistor Logic compatible to non-volatile quad-latch application. A few proposed variations of this topology were reported with the same working principle for RF power rectification [40–55].

In reference to the circuits in Fig. 3, the rectifier is usually stacked or cascaded in a multi-stage configuration where one single stage of the rectifier could be identified by diode-connected transistors M_1 and M_2 with capacitors C_1 and C_2 as shown in Fig. 3. During the negative cycle of the input RF voltage, the diode-connected transistor M_1 is in forward conduction mode while M_2 is turned off due to reverse potential. At this point, capacitor C_1 charges up to $(V_{RF} - V_{th1})$ where V_{th1} is the threshold voltage of the transistor M_1. During the positive half cycle of the input RF voltage, transistor M_2 is now in forward conduction while M_1 is in reverse conduction and is turned off. Capacitor C_2 now is charged to an output voltage described by the equation:

$$V_{out,1} = 2V_{RF} - V_{th1} - V_{th2} \quad (6)$$

where $V_{out,1}$ is the output voltage, V_{RF} in the peak input voltage and V_{th1} and V_{th2} is the threshold voltage of the transistor

M_1 and M_2 respectively.

The topology could be configured in multi stages represented by the intermediate stages as in Fig. 3(a) and (b) to generate a final output voltage, $V_{out,n}$ according to n number of stages. The integration in Fig. 3(a) are stacked where each stage in the circuit receives similar input power level while the configuration shown in Fig. 3(b) shows that the stages are cascaded where the series capacitor (C_1, C_{n+1}) also acts as a dc block providing dc shift for the subsequent stages. Dickson charge-pump is widely implemented due to its suitability for integration applications to overcome bottom plate capacitance of the capacitors and the parasitics of intermediate nodes in the Cockcroft-Walton configuration [73].

As observed in (6), the V_{th} of the transistor contributes to the voltage drop where the elimination of this detrimental loss could reduce the losses due to the forward voltage drop in the circuit and thus increasing the PCE. Various methods have been proposed on this topology to improve its

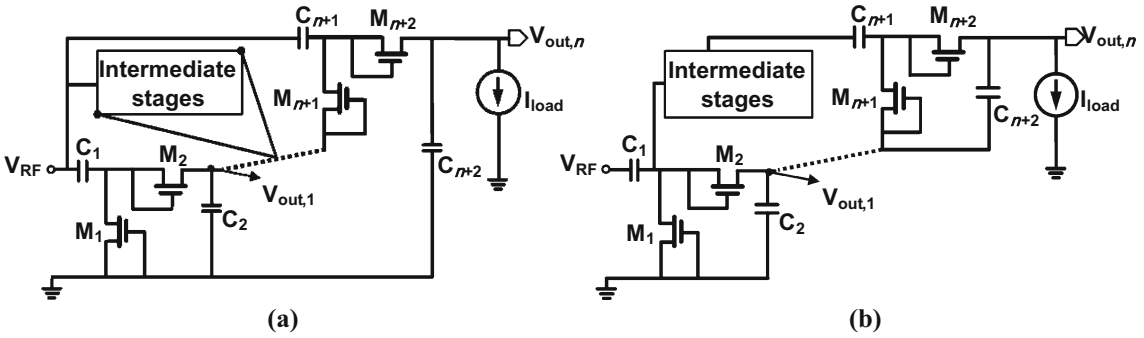


Fig. 3 Voltage multiplier (VM) configuration. **a** Dickson charge-pump. **b** Cockcroft-Walton

performance. One of the main technique is through the cancellation or compensation of the V_{th} of the transistors [40–51, 53, 54, 56, 74]. Figure 4 represents the schematic of this technique in view of a typical rectifier with a compensation voltage (V_C) that provides an addition compensation or cancellation voltage at the gate of the transistor to reduce the V_{th}.

The work in [41] reports a passive-mirror like canceller to cancel the effect of the V_{th} drop in order to increase the efficiency. However, in the mode of cancelling V_{th} completely, trade-off arises where the cancellation increases reverse leakage causing a flow back of the power to the source [42, 43, 49, 51, 54, 55]. This is undesirable in consideration of the average time of power flow which results in less charges flowing to the load, hence, decreasing the efficiency.

To minimize the trade-off between the effect of V_{th} drop and reverse leakage, [40, 42–51, 53, 54] reports various schemes that provides an optimal V_c for the transistors in the rectifier. [40] proposed a bias-voltage generator between the gate and the drain of the transistor to bias a specific V_C level. Another technique includes a floating-gate [42, 44] where the gate of the transistor in the rectifier are dc biased using a complementary metal-oxide semiconductor (CMOS) capacitor with V_C intact to offset its threshold while reducing the effect of reverse leakage.

Besides that, [43, 47, 49, 51] reports compensation schemes where the diode-connected transistors in the Dickson topology are compensated with the gate of the

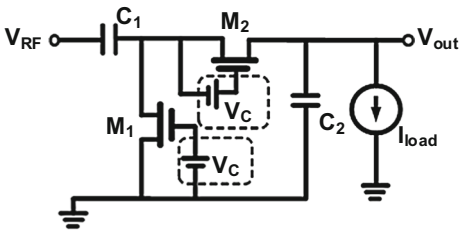


Fig. 4 Dickson rectifier with simplified threshold compensation scheme

transistors shorted to the drain(source) terminals of subsequent transistors in the multi-stage rectifier. Alternatively, [43] reports a scheme using "order" compensation. In a multi-stage rectifier, the dc voltage generated between each transistor can be tap for V_C. When a transistor taps this dc output of the next cascaded stage, it is considered order-1 compensation. Similarly, tapping the dc output of subsequent stages will be order-n compensation depending on the number, n of subsequent stage V_C is being tap.

A more complex scheme to tune the V_C for a transistor is by the ability to change the order of compensation in the rectifier is proposed in [47]. Hameed and Moez [49] further improved this type of compensation scheme with a hybrid-compensation method that provides forward compensation to reduce the detrimental effect of V_{th} and reverse compensation by increasing V_{th} to prevent reverse leakage when required. The work in [51] proposed an adaptive hybrid-compensation with diode-connected transistors in series at the gate to provide the compensation voltage with minimal circuitry. Other compensation methods include additional circuitry to independently generate V_C [53, 54] which increases the complexity of the circuitry.

An alternative methods of improving the performance of this rectifier is through bulk-biasing of the transistors to reduce the V_{th} [52], gate-boosting technique to boost the input RF voltage at the gate [48], cross-coupling scheme adaptation of the rectifier topology to reduce reverse leakage current [45] or the utilization of capacitor integration in the circuit [46, 50, 55]. Capacitor integration could be used to set the gate potential by storing the energy and discharging the voltage to the gate as proposed in [46], adopting capacitor as a pumping storage to cancel the effect of V_{th} [50] or by the placement of the capacitor at the output to decrease the load capacitance during the positive half cycle to reduce leakage current [55].

Other non-circuit technique in improving the performance has been proposed by the use of Schottky diodes or other process implementation in IC [37, 75, 76] which exhibits good performance in low V_{th} drop and low reverse leakage but with a trade-off in higher cost of fabrication

making it an unattractive practical solution to be implemented in IC integration [46, 48, 49].

Similar inclination of improvement is also evident in the CCDD topology shown in Fig. 5. This topology is derived from the diode-bridge rectifier which was first introduced on an IC implementation by [60] as a four-cell rectifier and given the definition of CCDD by [61]. This topology consists of 2 sets of a single NMOS transistor and a single PMOS transistor connected in series. Both sets are symmetrically connected in a cross-coupled configuration where the gates of one set of the series circuit is connected to tap the input which lies between the NMOS and PMOS transistor of the other set as shown in Fig. 5.

During the positive half cycle of the input signal V_{RF}, transistor M_{P2} and M_{N1} are forced to turn off where the gates are driven by positive and negative voltage respectively. Meanwhile transistor M_{P1} and M_{N2} turns on which creates a loop of a complete circuit to the load just like a diode-bridge rectifier. Likewise, during the negative half cycle of the input signal of V_{RF}, M_{P2} and M_{N1} turns on while transistor M_{P1} and M_{N2} are forced to turn off. Other components in this topology includes coupling capacitors, C_C that provides an ac coupling at the input and as a dc block to prevent dc charges to flow back to the source. Capacitor C_L is the smoothing capacitor to smooth out ripple voltage at the output and R_L is the output load.

This topology is capable of achieving a high peak PCE of up to 80% but suffers from reverse leakage at higher input power level [61]. Just like the Dickson-type topology, when the rectifier is connected in a multi-stage configuration the output voltage, V_{out} could become higher than the input RF voltage. When this happens, reverse leakage occurs where the charge will flow from the higher potential at V_{OUT} back to the lower potential of V_{RF} during the rising and falling period of the input RF voltage.

Recent works has reported techniques to reduce the effect of reverse current such as in [64, 69] which employs feedback network to detect V_{out} to control the gate biasing of the PMOS transistors. Simpler methods were incorporated with a resistive element such as a passive resistor or a high V_{th} transistor between the gate and the output [70–72]. This creates a high potential drop when V_{out} is larger than the V_{RF} thus reducing the detrimental effect of the reverse current.

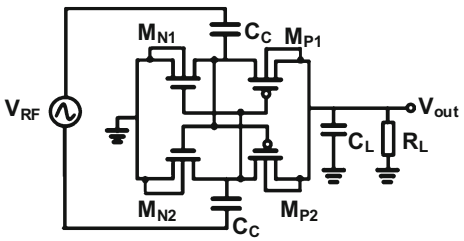


Fig. 5 CCDD rectifier topology

In the work [34], the author utilized the leakage to the advantage with a biasing scheme to enhance the RFEH rectifier as an overvoltage protection scheme. Another work in [65] employs a complementary topology implemented in CMOS and a diode bridge rectifier using Silicon-on-Sapphire (SOS) available in CMOS process to reduce the flow back current via the diode-bridge in SOS and to increase the forward current using the CCDD in CMOS. Other enhancement methods are also proposed such as providing dc biasing at the gate to reduce V_{th} effect using an adaptive threshold scheme similar in producing V_c in the Dickson topology [62]. Another work in [66] developed a hybrid energy harvester of a piezoelectric and RF harvester where the RF harvester uses the harvested energy from the piezoelectric to produce a dc offset. Table 1 summarizes the comparison of recent reported state-of-the-art RF rectifiers.

Selection of a rectifier topology to be used in an RFEH system depends on various trade-offs of the two prominent topologies. One can identify that the first trade-off is in the transistor count where the CCDD requires twice the amount of transistor compared to Dickson which can affect the size constraint in the IC fabrication. Besides that, a self-biasing CCDD topology is capable of achieving the output operating voltage with lesser number of stage of 2 [71, 72], 3 [34, 61, 65] or 5 [38] while the self-compensating Dickson topology usually requires higher number of stages ranging from 7 [48], 12 [47], 17 [42], 20 [44], 24 [49], or even up to 50 [57, 59] to achieve a proportionally output which could be one of the reason for the reported lower efficiency in a Dickson topology. Since the CCDD topology requires lesser number of stage to achieve the same output voltage, the total number of transistors of CCDD may be even lesser, thus having smaller area instead. However, the CCDD requires a differential antenna or PCB balun for the single-ended to differential conversion [51].

Another consideration to take note that the impedance of the rectifier in both topologies changes with input RF power level [37, 38, 45, 60, 77]. Also, the impedance of the rectifier changes with the number of stages and the transistor width [43, 49, 61]. These properties of the rectifier will be looked upon in the next section of the IMN circuits for RFEH system as it relates closely with the design consideration of IMN circuitry.

One last trade-off that exists in both topology is the shift of the PCE curve when the output load changes. Increasing the output load requires more power which reduces the peak PCE and sensitivity. Instead of just focusing in achieving peak PCE performance which has been obtained by many reported works in the CCDD topology, an area of research interest is to widen the high-PCE range of the

Table 1 Comparison of published work on integrated RF rectifier circuit techniques

Refs.	Year	Tech.	Rectifier topology	Enhancement technique	Frequency (MHz)	Peak PCE (% for load at input level)	V_{out}, (Volts)	Lowest reported sensitivity (dBm)	Max tested load, R_L
[40]	2006	300 nm	3-stage, Dickson	Bias-voltage generator	950	11% for no-load @ − 6 dBm	1.5	− 14	n.a.
[41]	2007	350 nm	1-stage, Dickson	Internal-V_{th} cancellation	953	36.6% for 80 µW @ − 6 dBm	3	n.a.	n.a.
[42]	2008	250 nm	16/36-stage, Dickson	Floating-gate transistor	906	60% for 30 µW @ 100 mV	2	− 22.6	0.33 MΩ
[43]	2011	90 nm	17-stage, Dickson	Self-V_{th} compensation	915	11% for 1 MΩ @ − 18.83 dBm	1	− 22.44	0.5 MΩ
[44]	2012	90 nm	20-stage, Dickson	Floating-gate transistor	2450	1% for 1 MΩ @ 125 mV	1.2	− 14.9	0.5 MΩ
[45]	2013	130 nm	2-stage, Dickson	Cross-coupling transistor	868	50% for no-load @ − 17 dBm	2	− 21	n.a.
[46][a]	2013	180 nm & 90 nm	5-stage, Dickson	Storage capacitor	915	11.9% for 1 MΩ @ − 18.2 dBm	1.35	− 20	100 kΩ
[47]	2014	65 nm	12-stage, Dickson	Tunable-V_{th} compensation	904.5	n.a.	1.7	− 20	n.a.
[48]	2014	65 nm	7-stage, Dickson	Gate-boosting	46,000–60,000	20.56% for 10 kΩ @ 7 dBm	4	− 7	1 kΩ
[49]	2014	130 nm	8/12-stage, Dickson	Self-V_{th} compensation	915	22.6% for 1 MΩ @ − 16.8 dBm	2.2	− 24	1 MΩ
[50]	2015	180 nm	n.a, Dickson	Pumping capacitor	433	22% for 10 kΩ @ − 9 dbm	0.8	− 14	10 kΩ
[51]	2015	130 nm	24-stage, Dickson	Adaptive-V_{th} compensation	915	32% for 1 MΩ @ − 15 dBm	3.2	− 20.5	0.5 MΩ
[53]	2017	180 nm	4-stage, Dickson	Independent-V_{th} generator	433	34% for 100 kΩ @ − 17 dBm	1	− 19	10 Ω
[54]	2017	180 nm	3-stage, Dickson	Adaptive-V_{th} compensation	402	31.8% for 30 kΩ @ − 1 dBm	1.38	− 12	30 kΩ
[61]	2009	180 nm	3-stage, CCDD	Differential-drive transistor	953	67.5% for 10 kΩ @ 12.5 dBm	1.8	<− 30	5 kΩ
[62]	2010	130 nm	4-stage, CCDD	Adaptive-V_{th} compensation	135.6, 400	54.9% for 12 µW @ − 6 dBm	1.8	− 10	n.a.
[63]	2011	180 nm	2-stage, CCDD	Dynamic compensation	900	43% for 160 kΩ @ − 17 dBm	0.7	− 24	n.a.
[64]	2011	130 nm	1-stage, CCDD	Gate-biasing	13.56, 860 to 2500	7.5% for 250 kΩ @ 12.5 dBm	1	− 10.3	n.a.
[65]	2012	250 nm + SOS	3-stage, CCDD	Technology complementary	100, 915	67% for 1 MΩ @ − 26.4 dBm 44% for 1 MΩ @ − 26.4 dBm	1	− 40	30 kΩ
[69]	2016	180 nm	1-stage, CCDD	Adaptive self-biasing	100	65% for 100 kΩ @ − 18 dBm	1	− 18	100 kΩ
[70]	2017	180 nm	1-stage, CCDD	Self-biasing	433	65.3% for 50 kΩ @ 15.2 dBm	1	− 17	50 kΩ
[34]	2017	130 nm	3-stage, CCDD	Self-body biasing	953, 2000	73.9% for 2 kΩ @ 4.34 dBm	3.5	− 12	2 kΩ
[71][a] [72][a]	2017	65 nm	2-stage, CCDD	DC-boosted gate bias	2450	59.6% for 29 kΩ @ − 12 dBm	1	− 17	3.5 kΩ

[a]Simulation work

circuit across the input RF power level especially for the CCDD topology [38, 69, 70]. Design methodology to achieve high efficiency for both RF rectifier topologies should be explored to overcome the lengthy task of optimization by executing time consuming simulations [57, 63, 78–80].

Designing the rectifier or any other circuitry on an IC level especially in CMOS has always been a challenge in the concept of realizing small physical form factor circuitry to lower the fabrication cost for mass production [74]. Selection of enhancement technique is considered based on the operation range of the rectifier. Sub-zero dBm input RF power harvesting involves reducing the detrimental effect of the threshold voltage of the transistor. The threshold cancellation, threshold reduction or gate-biasing technique is a well suited choice. Alternatively, the adaptive or dynamic threshold technique can be implemented when the range of input RF power harvesting is large to achieve a balance of threshold cancellation at low input RF voltage and reverse current reduction at high input RF voltage. Achieving high peak value and wide range of high-PCE with respect to the input power along with a greater sensitivity of the rectifier will be the main indicator that sets the benchmark of its performance.

Technology scaling of IC integration could enjoy lower voltage supply which helps to reduce the need for high voltage multiplication ratio, potentially lowering the need for large number of rectifier stages. However, the threshold voltage of the transistor which significantly dictate the performance of the rectifier only reduces slightly in advance CMOS technology which limits its influence to improve the efficiency and sensitivity of the rectifier.

4 Impedance matching network (IMN) for RFEH systems

The next block in an RFEH system is the IMN circuit which is integrated between the antenna and the rectifier. The IMN circuit ensures maximum power transfer of received power at the antenna to the load by the means of conjugate matching of the load impedance to the source impedance. A good matching lowers the reflection of the harvested input RF signal where the performance of the IMN is measured by the reflection coefficient, $S_{11}(dB)$ given by [35]:

$$S_{11}(dB) = \Gamma = \frac{Z_{rect} - Z_{ant}^*}{Z_{rect} + Z_{ant}^*} \tag{7}$$

where Γ is the reflection coefficient, Z_{rect} is the impedance of the rectifier and Z_{ant}^* is the impedance of the antenna. As the rectifier is a nonlinear circuit, Z_{rect} could be approximated as a linear load with a resistor and capacitor in parallel in a Dickson topology [73, 81]. As for the CCDD topology, a series capacitor and resistor with an induced voltage by a voltage source using Thévenin equivalent with a function of radiation resistance approximates Z_{rect} [38, 82].

Referring to (7), when the impedance of the rectifier and antenna are matched, the reflection measures down to zero which minimizes the reflected signal and maximizes the signal transfer from the antenna to the rectifier. Another form of the reflection coefficient equation is the power reflection coefficient, $|\Gamma|^2$ that calculates how much power is being reflected given by:

$$|\Gamma|^2 = \left|\frac{Z_{rect} - Z_{ant}^*}{Z_{rect} + Z_{ant}^*}\right|^2 \tag{8}$$

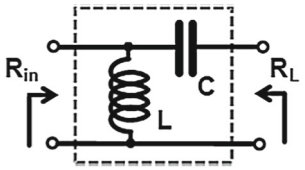
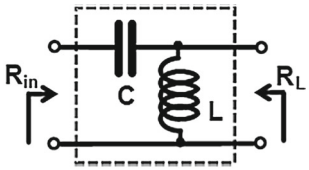
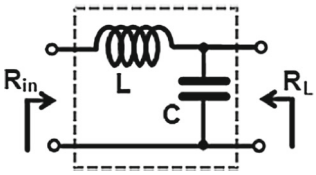
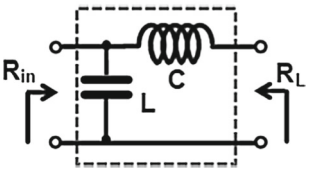
Though (8) is comparable to (7), the governing term in (8) is squared to represent the amount of power that is reflected.

The IMN circuit matches the impedance by resonating both source and load impedance through the storing and discharging of charges at a particular frequency. Similar use of the IMN circuit could be found in other application such as the Low-Noise Amplifier in RF receivers [77]. The most basic IMN network that has been implemented and studied for RFEH system is the L-matching [43, 73, 77, 83, 84]. Table 2 shows some variations of the L-matching and their corresponding mathematical relations used for RFEH systems. The term 'Q' is the Quality Factor which denotes the ratio of the stored energy to the dissipated power as a function of the frequency, R_{in} is the source (antenna) radiation resistance, and R_L is the load impedance which in the case of an RFEH system is the impedance of the rectifier and PMU. ω_o is the frequency of the input RF power while C and L are the values of the matching capacitor and inductor respectively.

Depending on the configuration of the L-matching selected, the imaginary part of the load impedance and the bond pads capacitance are considered in sizing the component of the IMN to achieve optimal matching condition during test condition of the IC chip. One of the main challenge in designing IMN circuit for RFEH system is that the impedance of the rectifier changes respective to the input RF power level.

Due to the fluctuation of impedance in the RF rectifier at different input power level, [77] suggests a methodology of using probability density distribution to determine the best value for the components to achieve highest performance of the IMN circuit across the operating input RF power range when designing for a RFEH system. Differential L-matching has also been implemented for RFEH system which is commonly used for differential rectifier topology such as the CCDD rectifier with two symmetrical

Table 2 Basic high-pass and low-pass L-matching network configuration with component sizing formula

High-Pass L-match		
	$Q = \sqrt{\frac{R_{in}}{R_L} - 1}$ $C = \frac{1}{\omega_o Q R_L}$ $L = \frac{1}{\omega_o^2 C}\left(1 + \frac{1}{Q^2}\right)$	 $Q = \sqrt{\frac{R_L}{R_{in}} - 1}$ $L = \frac{R_L}{\omega_o Q}$ $C = \frac{1}{\omega_o^2 L}\left(1 + \frac{1}{Q^2}\right)$
Low-Pass L-match		
	$Q = \sqrt{\frac{R_{in}}{R_L} - 1}$ $L = \frac{QR_L}{\omega_o}$ $C = \frac{1}{\omega_o^2 L}\left(\frac{Q^2}{1+Q^2}\right)$	 $Q = \sqrt{\frac{R_L}{R_{in}} - 1}$ $C = \frac{Q}{\omega_o R_L}$ $L = \frac{1}{\omega_o^2 C}\left(\frac{Q^2}{1+Q^2}\right)$

L-matching circuits at each input of the rectifier [38, 85, 86].

Alternatively, [73] reports a complex L-matching techniques such as a reconfigurable L-matching for RFEH system by a series of binary controlled capacitor to change the value of the capacitors to ensure lowest reflection across input RF power level due to the changing impedance of the rectifier and also to provide the capability of tuning the IMN circuit to operate at a variety of input RF frequency. The work was implemented with an RFEH system where the PMU (part of this work will be discussed later) controls the binary system presented in [87]. The work also investigates the difference of on-chip and off-chip IMN which concludes an off-chip IMN to perform better in the context of sensitivity and quality factor of the passive components [73]. While off-chip IMN exhibits better performance, on-chip IMN allows for fully system integration with much smaller physical size with regards to its form factor.

Another type of matching that has been reported for RFEH system is the transformer matching [81, 88, 89]. Figure 6 shows a simple circuit representation of a transformer matching used in RFEH systems. Transformer matching performs better for low-impedance antennas that naturally produces lower output voltage to be increased through the voltage gain capability of the IMN circuit [89]. In [81], the work utilizes a step-up transformer for power matching and as a voltage booster for the harvested RF power.

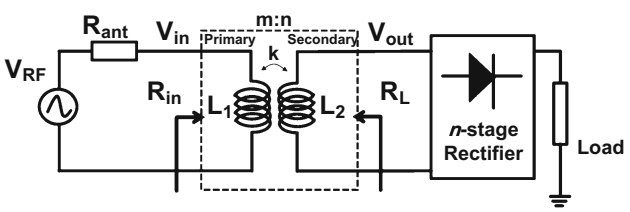


Fig. 6 Transformer matching

Other on-chip IMN design proposed for dual-band RF harvesting [90, 91] expands a focus of RFEH system design for more than one frequency opening up the scope of RFEH system that are capable of harvesting multiple input RF frequencies. The work in [90] developed a RFEH system with two series inductors connected to one input source where the power from two frequencies are harvested simultaneously to two different rectifier circuits while [91] developed a Band-Pass Filter (BPF) and a Band-Stop Filter (BSF) for two frequencies on an Integrated-Passive-Device (IPD) technology with the rectifier implemented on standard CMOS platform to achieve higher IMN circuit performance.

There are works that attempted to eliminate the IMN circuit in RFEH system by an antenna co-design strategy in the development of the system [41, 82]. The co-design strategy is to develop the antenna and the circuit simultaneously to matched impedance without the need for intermediate matching through an IMN circuit which could be explored further if one is to consider integrated antenna design in the scope of development. This can increase the overall efficiency as losses in the matching network is eliminated. Table 3 summarizes the reviewed IMN works for RFEH system.

Table 3 Comparison of IMN performance implemented for RFEH application

Refs.	Year	Technology	Topology	Frequency (MHz)	Sensitivity (dBm)	Effective area (μm^2)
[81]	2010	180 nm	L-match	3530	− 5	230 × 230
		180 nm	Transformer	3850	− 12	200 × 200
[88]	2010	180 nm	Transformer	2400	− 11[a]	192 × 192 (IMN only)
[89]	2015	130 nm	Transformer	1300	− 25	200 × 250
[73]	2014	180 nm	Tunable L-match	from 850 to 1200	− 21.7	450 × 820
		Off-chip	L-match	781–798	− 27.3	n.a.
[77]	2017	Off-chip	L-match	902–928	− 15	n.a.
[90]	2013	130 nm	Series inductor	900 and 1900	− 19.3	500 × 500
[91]	2017	On-chip IPD	BPF/BSF	930 and 2530	− 15.4	2900 × 4000

[a]Estimated from graph

Based on the review on IMN circuits, an apparent trade-off is observed between the L-matching and the transformer matching is in the area constraint of integration. The L-matching has a simple approach in design compared to the transformer matching. An on-chip L-matching circuit has inferior performance compared to an off-chip due to the Q factor of the inductor which limits boosting capability and affects the sensitivity. Transformer matching on the other hand has always been reported as an on-chip circuitry. Hence, the trade-off could be scaled down to the desire for highest performance for on-chip implementation with size constraint of the IMN circuit. The limited area for on-chip design makes transformer matching more attractive for on-chip IMN integration in RFEH system.

Another consideration in the aspect of voltage gain is the desire of the IMN to act as a gain boosting element. With transformer matching the gain could be configured based on

the winding ratio between the primary and secondary coils. The L-matching on the other hand is highly dependent on the Q factor of the inductor where its limitation for on-chip integration is apparent. The output voltage and loading current also affects the sensitivity where the parameters of the output load has to be considered during the design of the IMN to achieve optimal matching and performance.

5 Power management unit (PMU) of RFEH systems

The final block is the PMU which is usually integrated after the rectifier in the RFEH system chain. The PMU exists for a variety of power management purposes. One of the main reasons is to manage the fluctuation of the received power in effect to the environmental condition and the low-power level received at the input of the antenna. For whichever methods used for the PMU, its ultimate purpose in the system is to enhance the performance of the overall RFEH system. There are various circuits in a PMU depending on the method to manage the power of the system.

First of all, when low input RF power is expected, the rectifier could be sized to generate the highest voltage possible allowing high voltage generation at the output [92]. This leads to issues where higher number of stages increases the V_{th} drop which decreases the efficiency. Besides that, if the input RF power level fluctuates dramatically, with just a rectifying circuit will create an unbounded dc output voltage for the RFEH system. The rectified output dc voltage changes when the input RF level fluctuates in effect to the environmental condition or the change in distance from the transmitting antenna. One of the most basic PMU integration is to include a voltage regulator [75]. The voltage regulator is only applicable when the rectified output voltage fluctuates at a range close to the desired output dc value. In the case of high input fluctuation, a voltage regulator as a PMU will suffer in its efficiency when regulating the large dc voltage changes at the output. In [85], the work reported a RFEH system solution with a single stage rectifier paired with an inductor-based DC–DC boost converter and an adaptive control to provide an adaptive clocking for the converter respective to the input RF power level as a PMU. A single stage rectifier prevents excessive V_{th} drop of the transistor, unlike to higher number of rectifier stages. The proposed system detects the power level at the output of the rectifier using a comparator for latching a pulse generator that provides the clocking for the boost converter to supply charges to the load. The frequency of the clock changes according to the detected power level for optimal operation of the boost converter.

Another work in [38] realized a reconfigurable rectifier which mainly focuses on the start-up issue of RFEH systems to increase its sensitivity due to the fluctuating input power level. The proposed PMU allows the use of various digital blocks which includes a clock generator, load,

storage and rectifier controller with a latched comparator and binary blocks. A voltage reference generator is the only analog block used. The PMU configures the number of rectifier stages to the highest number according to the design to achieve highest voltage at a respective low input power level while increasing the sensitivity. Alternatively, the PMU configures to the least number of stages when the input power level reaches a level capable of rectifying to the desired output voltage.

Rather than reconfiguring the number of stages, some reported works in [45, 93] reconfigure the arrangement of the rectifier stages either in series or parallel depending on the input power level. Arranging the rectifier in series or parallel changes the impedance of the rectifier to enhance the impedance matching condition and thus increases the sensitivity of the RFEH system [45]. Another reason is due to the PCE curve where different rectifier configuration could shift the curve according to the input level [93]. Figure 7 illustrate the PCE against the input RF power for a single stage rectifier. Integrating another rectifier stage in series could shift the PCE to the right where the peak PCE lies at the higher power.

Similarly, configuring the rectifier stages in parallel shifts the peak PCE curve to the left at lower input RF power which proposes the development of a PMU that is able to reconfigure the arrangement of a multi-stage rectifier to enhance the PCE across input RF power level.

Besides that, transistors in a process might exhibit different performance based on the input power level where the work in [38] suggest a dual-path PMU solution to control the power fed between two types of rectifier using different transistors such as the standard-threshold, low-threshold and high-threshold transistors in a CMOS process. Based on the detected input power level, the PMU switches on and off a specific path in the RFEH system to allow power to be fed through the path where highest efficiency could be achieved at a specific input power level.

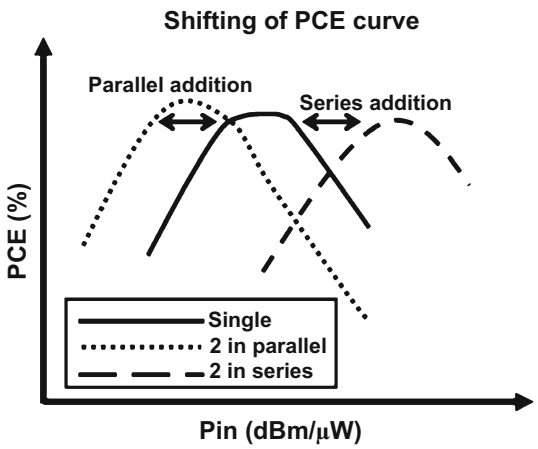


Fig. 7 Example of shift in PCE curve due to rectifier configuration

Regularly the RFEH system is limited by the received power which is insufficient at the load. Hence, alternative type of PMU is designed to manage a storage system in harvesting and storing energy subsequently discharging it to a load when sufficient charge is accumulated [87, 94, 95]. Level detectors are used to detect various power level in the RFEH system to charge a storage capacitor and discharge power to the load. Also, for the work in [87, 94], the charging and discharging can be disabled to allow the power to flow directly to the load when sufficiency high input power is made available.

The PMU of an RFEH system could be summarized into two topologies by virtue of the function. Figure 8 summarizes the two basic PMU methods used in an RFEH system. Figure 8(a) shows the PMU system which controls various elements such as rectifier configuration or the pulsing for the boost converter due to fluctuating input power level. PMU in Fig. 8(b) controls a storage element due to the available low input power. Regardless of the function in the PMU, a few circuits are common to a PMU such a voltage sensor, reference generator and a controller where its power is drawn from the harvested energy. Table 4 compares the state-of-the-art RFEH system implementations. Selecting a topology for designing the system depends solely on the application of the system. Applications such as RFID and transducers would require constant power being supplied while WSN requires a burst of power which demand energy storage.

The PMU topology could be selected based on the loading circuitry the harvested power intends to supply. As was mentioned in the rectifier section earlier, increasing the load reduces the PCE which only applies to application that requires constant power. If constant power is not required, a charging circuit could be developed to accumulate the energy to the required amount before it is discharged to the load dictating the load to be the least concern in designing the RFEH system. Also related to the first two considerations is the range of the input RF power level to be harvested. If low-power harvesting is desired, the PMU must be able to accumulate the energy when the input power is low and allow for power to be directed to the load when the input level is high. Complexity of the PMU will vary depending on the application and function. The PMU should also be designed to consume low-power when its power is drawn from the harvested energy to enhance the efficiency of the overall RFEH system.

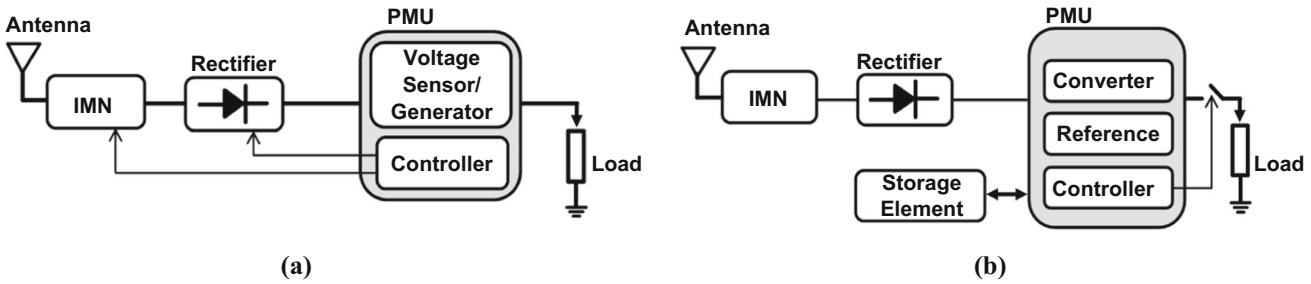


Fig. 8 PMU topologies in RFEH system with **a** reconfiguration control of other circuit blocks **b** control flow of harvested power

Table 4 Comparison of reported state-of-the-art RFEH systems

Refs.	Year	Technology	Frequency (MHz)	Rectifier	IMN	PMU function	Overall PCE (% for load @ dBm)	Sensitivity (dBm)
[95]	2011	130 nm	100–2500	Dickson	No	Load/storage controller	n.a.	− 18.7
[87]	2017	180 nm	900	Dickson	On-chip, reconfigurable L-match	Reconfigurable rectifier stages and IMN with load/ storage controller	25% for 1 MΩ @ 0 dBm	− 14.8[b]
[45]	2013	130 nm	868	Dickson	Off-chip	Reconfigure rectifier configuration	60% for no-load @ − 8.5 dBm (est.)	− 21
[105]	2016	Schottky Diode + 350 nm	136	Dickson	Off-chip, π-match	Load/storage controller	10% for 70 kΩ	− 19
[38]	2017	65 nm	900	CCDD	Off-chip, differential L-match	Reconfigure power flow of rectifier path	36.5% for 147 kΩ @ − 10 dBm	− 17.7[a]
[93]	2014	180 nm	2400	CCDD	No	Reconfigure rectifier configuration	47% for 2 kΩ @ 8.9 dBm	− 5
[85]	2015	180 nm	900	CCDD	Off-chip, differential L-match	Single-stage rectifier with Boost converter	44.1% for 144 kΩ @ − 12 dBm	− 17[c]
[86]	2017	40 nm	915	CCDD	Off-chip, L-match	Load/storage controller	36.83% for 88 kΩ @ − 11.47 dBm	− 22.6[a]
[94]	2014	130 nm	900	CCDD	No	Load/storage controller	n.a.	− 15[d]

[a]No load

[b]Load start receiving duty-cycled current

[c]For 1 MΩ load

[d]Circuit starts storing energy

6 Additional aspects of RFEH IC design applications

There are other research initiatives in RF energy harvesting as a whole that are related to design integrated RFEH systems. One emerging area is the millimetre (mm)-wave frequencies RF Transceivers in CMOS technology [48, 52, 67, 96]. Reported performance for RFEH systems in this area still stumbles where the highest reported peak PCE is only 20% with a sensitivity of 6dBm [67]. Secondly, there are research initiatives of harvesting various types of RF signal concurrently [97, 98]. Most of the RFEH system blocks investigated assume a pure sinusoidal input RF signal. The work in [98] shows that the performance of an RFEH system is not limited to the input RF power level and frequency but also the type and shape of the harvested waveform in a practical implementation. Finally, emerging research is exploring multi-band RF harvesting through circuit design both in a discrete and integrated form to increase the capable supply power density of an RFEH system [2, 82, 91, 99]. Current multi-band RF harvesting lies in the interest of rectenna design where the rectifier is fused into the antenna in one design using discrete components [100–104]. Future research on multi-band RF

harvesting has also potential for IC implementation to reduce the physical form factor of multi-band RFEH systems.

7 Conclusions

This paper presented a review of the RFEH system working on chip and various works related to the system blocks. It covered the gaps and narrowed down the focus of RFEH design in an IC implementation. Each block is identified with its scope, direction, performance, limitations and potential in circuit integration for real-life applications along with further research and improvements. A section on the design challenges and research trend of RFEH systems has also been presented to summarize the challenges in their designs and some recent reported research initiatives in RF energy harvesting that should be considered.

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