23.1 A 2.5V 57MHz 15-Tap SC Bandpass Interpolating Filter with 320MHz Output Sampling Rate in 0.35μm CMOS

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Integration of high-frequency analog filtering into the system analog front-end is increasingly demanded for high-speed communications. The highest previously-reported output rate CMOS switched-capacitor (SC) filter achieves 200MSample/s for a low-pass biquad section [1]. This 15-Tap, SC bandpass interpolating filter has 320MSample/s output (up to 400MSample/s) in 0.35μm CMOS technology. Based on multirate processing techniques, this filter is intended for use in an 8b direct-digital frequency synthesis (DDFS) system shown in Figure 23.1.1. It up-translates a 22-24MHz input band sampled at 80MHz to a 56-58MHz output band sampled at 320MHz, allowing a 3-fold speed reduction from original 240MHz to 80MHz for the DDFS+DAC core and a 2-fold relaxation from 4th-order to 2nd-order for the following continuous-time smoothing filter.

A multi-notch 15-tap FIR function is optimized to avoid use of a higher-sensitivity, high-Q IIR and rather large weight-spread, higher-order standard bandpass FIR function. Based on polyphase multirate interpolation structures in Reference [2], the main filter core efficiently operates at lower input sampling rate, as shown in Figure 23.1.2. Beside the 4-path polyphase sub-filters implementing FIR tap weights, an interleaved-serial delay line with rotating-switching achieves the 15 tap delays with 4 stages. Autozeroing in this low-speed filter core alleviates the pattern noise imposed by the offset propagation in the delay line and mismatches in parallel polyphase filter bands. The charge-transferring-free (CTF) property of the delay circuit eliminates capacitance ratio mismatches, reduces finite gain errors and increases speed. The filter tap weights are implemented as direct capacitance ratios of the SC branches to the summing capacitor by either in-phase direct charge coupling or out-phase charge transferring.

The high-speed output commutator has <2.4ns settling time to provide 320MSample/s outputs by counting non-overlapping phase gap. This is optimized to have full output sampling period operation at maximum speed while minimizing power consumption and improving linearity. The CTF property associated with double-sampled SC CMFB reduces path gain and bandwidth mismatches. The noise and gain errors are low using a sampling/holding capacitor of 0.48pF and 0.7pF, respectively, for the delay and commutator circuits, yielding efficient trade-off between feedback factor and slew rate. The maximum spread is only 8 and due to noise, matching and speed considerations, the unit capacitance is 0.1pF and 0.15pF, respectively for polyphase filters 0, 2 and 1, 3. An input track-and-hold (T/H) circuit and a wideband output driver including a level-shifter followed by a low-output impedance buffer are designed for testability.

Two different-speed, single-stage telescopic opamps are designed for the same input and output common-mode levels at 0.95V for 2.5V supply so as to use only nMOS switches to minimize routing complications due to the multirate scheme and noise coupling in high-frequency operations. Post-layout simulations show that the fastest opamp dissipates around 12mW at 2.5V supply to achieve 66.5dB gain, 1GHz unit-gain frequency for 2.5pF loading, and about 1.6ns to settle at 1V voltage step with 1.7V/ns slew rate.

The phase generation is designed to provide 8 and 13 phases rotating at 320 and 80MHz respectively from a 320MHz reference. Due to the high-frequency signal output, stringent criteria are needed for phase skew mismatches (σ<5ps) to the output commutator, thus minimizing modulated sidebands overlapped onto the filter-rejected bands. This is first by means of a careful logic design and layout for equal-propagation-gate-delay control to design systematic mismatches, and then by a specific edge trigger buffer circuit for last-stage rising-edge synchronization control to random process mismatches and individual-VDD-supply scheme for high- and low-speed phase generation parts with on-chip decoupling for dI/dt-noise control to supply noise mismatches.

The filter is integrated in a 0.35μm double-poly, triple-metal CMOS technology. Separated VDD supply pins but shared ground with on-chip decoupling for analog and digital parts minimizes inductivity in their current return path for signal transfer (nearly 50% noise reduction in simulation). Strict matching in sensitive circuit parts is maintained and a clean signal and substrate environment is achieved by ample substrate contacts, multi-dimensional shielding with minimized return-current-path impedance.

Measurements are taken for 10 samples at room temperature, with 2.5V analog and digital supplies, for 160 and 320MHz output sampling rate. Further measurements are carried out at 400MHz output rate at 2.5V analog and 3.3V digital supplies. The measured amplitude response in Figure 23.1.3 shows that the minimum stopband rejection is ~50/45/40dB for 160/320/400MHz output rates. To demonstrate the frequency up-translation process, Figure 23.1.4 presents the circuit waveforms of a $1V_{p\text{-}p}$ 22MHz input and the resulting 58MHz output sampled at 320MHz with its corresponding spectrum. The delta marker 1,2 and 3 are the folded images of their 3rd-harmonics sampled either at 80 or 320MHz, which are all <-66dBc, resulting in -62.4dB THD. The highest pattern noise at 80MHz is -70dBc, and the total pattern noise measured within Nyquist band with zero input is only ~$120\mu V_{rms}$. The observed modulation sidebands at 18, 62 and 98MHz caused by the phase skews are below -72dBc. Figure 23.1.5 reports the IM3 and THD performance vs. different input signal levels for 3 distinct output rates. For f_s=320MHz, 1% THD and 1% IM3 correspond to one $2.1V_{p\text{-}p}$ and two $0.85V_{p\text{-}p}$ inputs respectively, and the measured total output noise is $280\mu V_{rms}$ (including the T/H and output driver which only degrades performance), thus resulting in a dynamic range of 68.5dB for 1% THD and 61dB for 1% IM3. The detailed performance for 3 sampling rates are summarized in Figure 23.1.7, and the total power for 3 cases is 67, 136, 157mW, corresponding to 4mW (160MHz) or 8mW (320/400MHz) analog power per tap.

Acknowledgements:
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References:
[1] A.Baschirotto et al., "A 200-Ms/s 10-mW Switched-Capacitor Filter in 0.5-μm CMOS Technology," IEEE J. Solid-State Circuits, vol.35, no.8, pp.1215-1219, Aug. 2000.
[2] Seng-Pan U et al., "Improved Switched-Capacitor Interpolators with Reduced Sample-and-Hold Effects," IEEE Trans. on CAS-II, vol.47, no.8, pp.665-684, Aug. 2000.

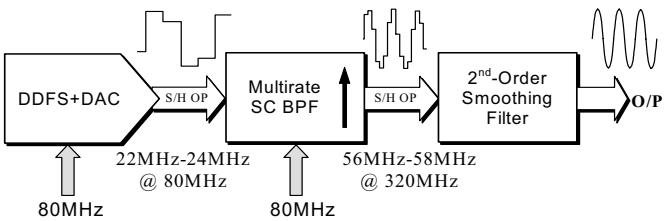

Figure 23.1.1: High-frequency SC interpolating BPF for DDFS system.

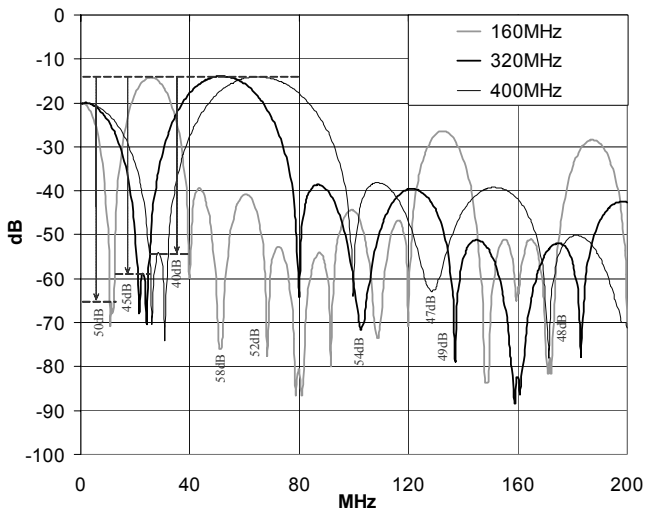

Figure 23.1.3: Measured amplitude responses for different output sampling rates.

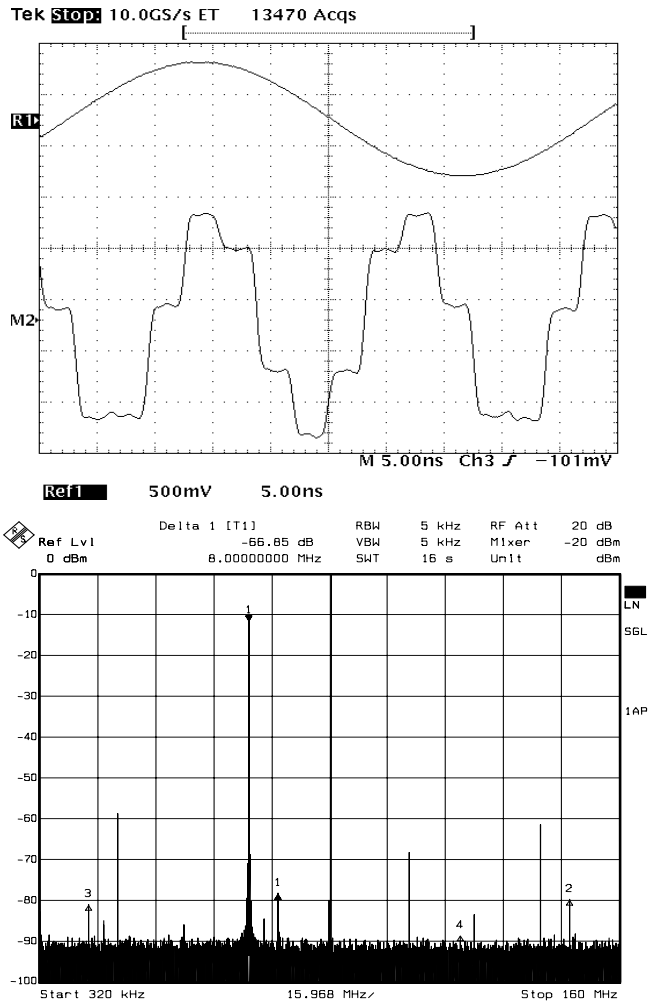

Figure 23.1.4: Measured waveform and spectrum of 58MHz signal output with a 1Vp-p 22MHz input (f_s=320MHz).

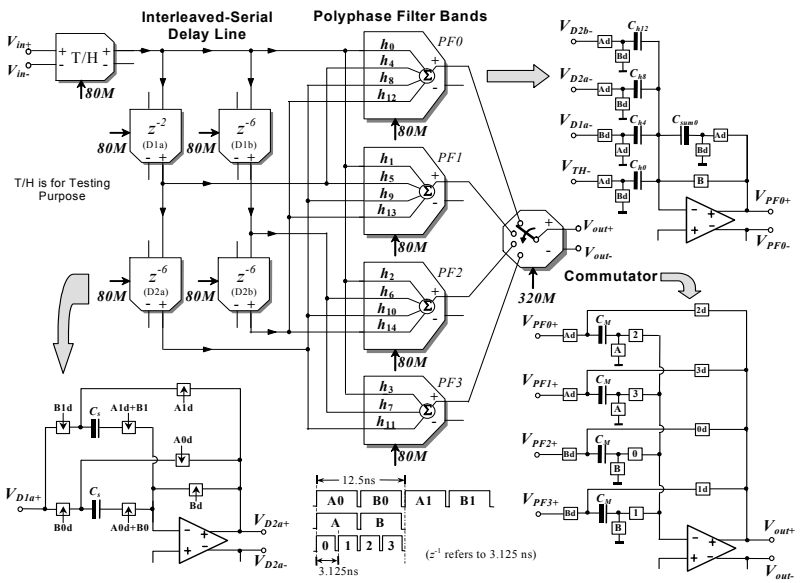

Figure 23.1.2: Circuit structure with simplified schematics.

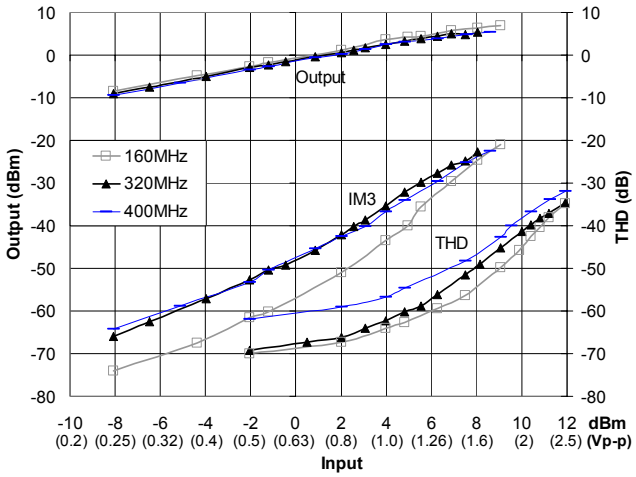

Figure 23.1.5: Measured THD and IM3 vs. input signal level for different output sampling rates.

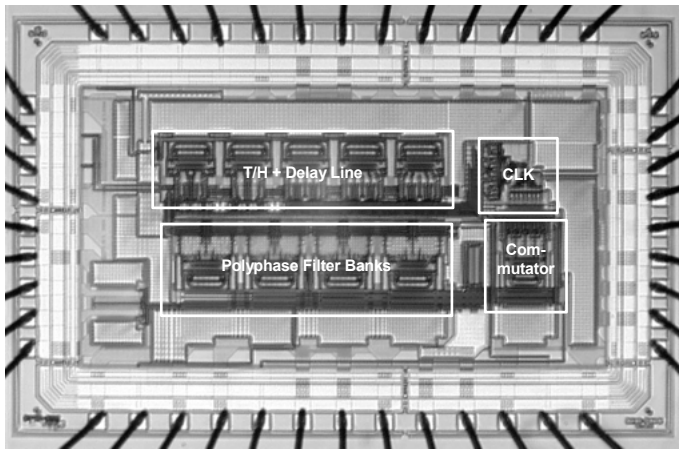

Figure 23.1.6: Die micrograph.

Technology		0.35µm CMOS	
Filter order		15-tap FIR	
Input Sampling Rate	100MHz	80MHz	40MHz
Output Sampling Rate	400MHz	320MHz	160MHz
Center Frequency (f_{center})	71.25MHz	57MHz	28.5MHz
Min. Stopband Rejection	-40dB	-45dB	-50dB
THD (FS: 1 V_{p-p}, $f_{out}=f_{center}$)[1,2]	-57dB	-62dB	-64dB
IM3 (-6dB of FS each tone)[2]	-53dB	-52dB	-62dB
Total Output Noise[2]	265µV_{rms}	280µV_{rms}	262µV_{rms}
Total Pattern Noise[2]	243µV_{rms}	120µV_{rms}	120µV_{rms}
Dynamic Range (1% THD)	68dB	68.5dB	69.4dB
Dynamic Range (1% IM3)	62dB	61dB	64dB
OIP3	22.5dBm	23dBm	26.4dBm
CMRR ($f_{in}=f_{center}$)	53dB	54.5dB	56dB
Active Core Area		$2mm^2$ (T/H + BPF + CLK)	
Supply (Analog, digital)	2.5V, 3.3V	2.5V, 2.5V	2.5V, 2.5V
Analog Power[3]	120mW	120mW	59mW
Analog Power -per-tap	8mW	8mW	4mW
Digital Power	37mW	15.8mW	7.8mW
Total Power	157mW	136mW	67mW

Note 1: THD measured with 20 tones by counting up to 5 th harmonic of both input and output signals as well as their folded images by the multirate sampling within Nyquist band.
Note 2: The distortion and noise measurements include the input T/H and output driver.
Note 3: Analog power excluding input T/H and output driver.

Figure 23.1.7: Measured filter performance.