A Fifth-Order 20-MHz Transistorized-LC-Ladder LPF With 58.2-dB SFDR, 68-μW/Pole/MHz Efficiency, and 0.13-mm^2 Die Size in 90-nm CMOS

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***Abstract*—A novel transistorized-LC-ladder low-pass filter (LPF) is realized by combining *source followers* with *Q-enhanced floating differential active inductors*. It features a small number of active devices to minimize the sources of nonlinearity and noise and a robust frequency response against process variations and device mismatches. A fifth-order 20-MHz LPF prototype is fabricated in 90-nm CMOS. It measures a 58.2-dB spurious-free dynamic range with 6.8 mW of power, which corresponds to a selectivity efficiency of 68-μW/pole/MHz favorably comparable with the state of the art. The die size is merely 0.13 mm^2.**

***Index Terms*—Active inductor, CMOS, continuous time, floating differential active inductor (FDAI), low-pass filter (LPF), source follower (SF).**

I. Introduction

WIRELESS receivers relying on direct conversion entails high-performance baseband low-pass filters (LPFs) for channel selection. Entered into the nanoscale CMOS regime, operational amplifier (Op-Amp)-less continuous-time LPF becomes a prospective direction to balance the power and area with selectivity and spurious-free dynamic range (SFDR). Cascade of source follower (SF)-based biquads [1] is an example of transistor-intensive LPF featuring the following: 1) very small number of active devices; 2) intrinsically linear I/O relationship (i.e., the $V_{\rm GS}$ of MOSFET); 3) no parasitic pole; and 4) free of common-mode feedback (CMFB) in differential realization.

Generally, there are two existing methods to build high-order SF-based LPFs. One is via cascading a number of SF-based biquads, with each implementing a complex pole pair of the transfer function [1]–[3]. However, due to the inconsistency of I/O common voltages and independency of each pole pair, this method is more sensitive to process variations and component mismatches. Another method is the single-loop high-order filter [4] via combining first-order positive- and negative-equivalent resistors. This topology is like a transistorized-RC-ladder filter and is hence less sensitive to process variations and component mismatches. The main pitfall of it is the dependence of its input impedance with the filter order at different frequencies, which degrades its generality to suit a wide variety of systems.

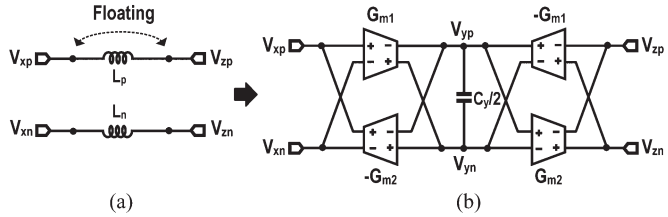

Fig. 1. (a) Floating differential inductor was typically emulated via (b) four G_m cells and one capacitor configured as a negative-feedback gyrator.

This brief proposes a transistorized-LC-ladder LPF merging the advantageous properties of SF and Q-enhanced floating differential active inductor (FDAI) techniques. It features not only a small number of active devices but also more robust filter response than the direct cascade of multiple SF biquads [1]–[3]. The input impedance is as high over a wide frequency range as it is solely the gate node of the MOSFET, resolving the limitation of [4]. The proof-of-concept prototype is a fifth-order 20-MHz LPF suitable for wideband applications such as the IEEE 802.11n wireless local-area network. The demonstrated merits are high SFDR, high power/pole/bandwidth $(f_{-3\ \rm dB})$ efficiency, and a compact die size.

This brief is organized as follows. Section II introduces a new transistorized Q-enhanced FDAI. The circuit implementation and simulation results of a fifth-order LPF design are presented in Section III, and the measurement results are given in Section IV. Finally, Section V draws the conclusions.

II. Transistorized Q-Enhanced FDAI

A high-order baseband LPF can be synthesized via cascade of biquads or denormalized from an LC-ladder prototype using active inductor emulation. The former is widespread for its ease of separated pole-pair design. However, the uncorrelated pole pairs also make the frequency response more sensitive to component mismatches, leading to unexpected gain droop and ripple. The LC ladder, in contrast, is a composite topology inherently more robust to process variations and component mismatches [5]. The key challenge lies on the active emulation of the floating inductors [Fig. 1(a)]. The typical realization of it is a negative-feedback gyrator [6]–[9] as shown in Fig. 1(b), which is, however, exposed to numerous sources of noise and nonlinearity due to the extensive use of transconductor (G_m)

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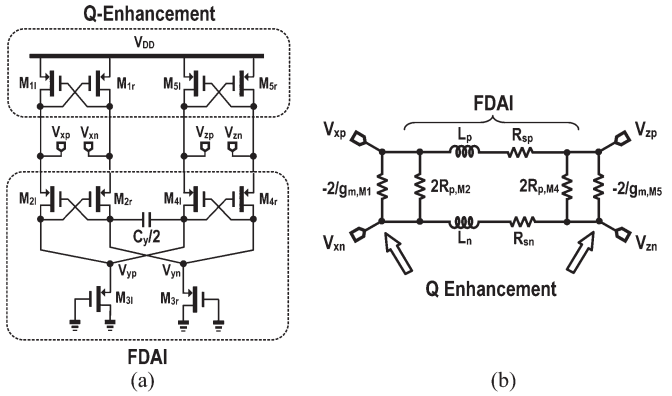


Fig. 2. (a) Proposed transistorized FDAI featuring current-reuse negative G_m cells for Q enhancement. (b) Its passive equivalent circuit.

cells and their high I/O impedances. For instance, if each G_m cell is implemented as a differential pair with an active load [7], at least 20 transistors and four independent current paths will be required. Also, the untunable quality factor (Q) of the emulated inductor is limited by the finite output resistance of all MOSFETs, which is particularly pronounced in nanoscale CMOS technologies.

The proposed transistorized Q-enhanced FDAI is depicted in Fig. 2(a). It is composed by two positive-feedback (PF) gyrators ($M_{2l,r}$ and $M_{4l,r}$) connected in parallel with respect to the medium nodes $(V_{\mathrm{yp},n})$, a positive-G_m stage $(M_{3l,r})$, and a capacitor $(C_y/2)$. When the PF gyrators transform the capacitive effect of $C_y/2$ into inductive, $M_{3l,r}$ cancels the negative G_m resulted from the PF gyrators at the $V_{\mathrm{yp},n}$ nodes. Two negative G_m cells ($M_{1l,r}$ and $M_{5l,r}$) cancel out the resistive parts ($R_{1,M2}$ and $R_{1,M4}$) of the PF gyrators at the one $(V_{\mathrm{xp},n})$ and another $(V_{\mathrm{zp},n})$ nodes. Comparing with the architecture in Fig. 1(b), the proposed FDAI reduces the transistor counts to ten and current paths to two while offering a crucial benefit of sizeable Q-enhancement under current reuse.

When the FDAI is considered differentially symmetric, the main design parameters can be derived based on the equivalent circuit [Fig. 2(b)] as follows:

$$L_p = L_n \approx \frac{C_y}{g_{m,M2}^2} \tag{1}$$

$$R_{p,M2} = R_{p,M4} \approx \frac{1}{g_{m,M2} + g_{\mathrm{ds},M2}} \tag{2}$$

$$R_{\mathrm{sp}} = R_{\mathrm{sn}} \approx \frac{g_{m,M3} - 2g_{m,M2} + g_{\mathrm{ds},M3} + 2g_{\mathrm{ds},M2}}{g_{m,M2}^2} \tag{3}$$

where $g_{m,\mathrm{Mx}}$ and $g_{\mathrm{ds,Mx}}$ are the transconductance and output conductance of the numbered transistors, respectively. Devices with a reasonable channel length can ensure $g_{\mathrm{ds,Mx}} \ll g_{m,\mathrm{Mx}}$. Thus, according to (2) and (3), the parasitic series resistance $R_{\mathrm{sp},n}$ is negligible when $g_{m,M3}$ is sized as $2g_{m,M2}$. The Q of the FDAI is mainly determined by the parasitic parallel resistance $R_{p,M2}$ $(R_{p,M4})$, which can be canceled by adding a current-reuse negative G_m cell $M_{1l,r}$ $(M_{5l,r})$. The enhanced Q of the FDAI is given by

$$Q_{L,\mathrm{en}} \approx \frac{g_{m,M2}^2}{(g_{m,M2} - g_{m,M1} + g_{\mathrm{ds},M2})\omega C_y} \tag{4}$$

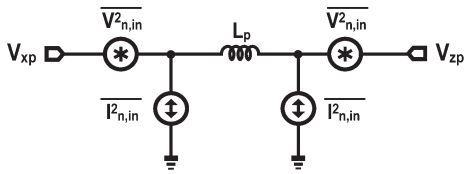


Fig. 3. Noise-equivalent circuit of the FDAI.

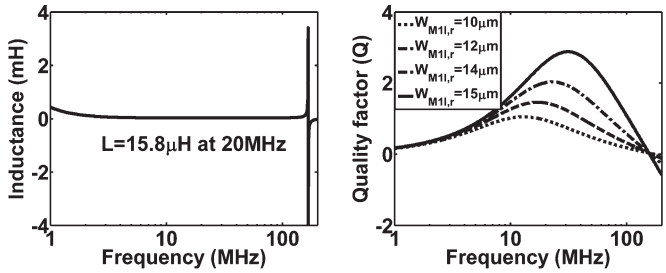


Fig. 4. Simulated frequency-domain behaviors of the FDAI: (a) inductance and (b) Q factor.

The half-circuit equivalent of the FDAI for noise analysis is depicted in Fig. 3, where, for simplicity, only the thermal noise currents of each transistor are considered. Owing to the low input impedance ($R_{p,M2}$ and $R_{p,M4}$) at the V_{xp} and V_{zp} of the FDAI in Fig. 2(a), the input-referred noise current is not negligible even at low frequencies [10]. By referring the thermal noise currents to the external terminals (V_{xp} and V_{zp}) of the FDAI, the equivalent parameters (input-referred noise voltage and noise current) are derived as

$$\overline{V_{n,1n}^2} = \frac{4kT\gamma}{g_{m,M2}^2}\left(g_{m,M2} + \frac{g_{m,M3}}{2}\right) \tag{5}$$

$$\overline{I_{n,1n}^2} = 4kT\gamma\frac{g_{m,M3}}{2} \tag{6}$$

It can be observed that the noises referred to the external terminals can be reduced by increasing the transconductance of the PF gyrators.

The FDAI also has the simplicity on biasing. First, since all devices are PMOS, the bulk and source terminals can be tied to avoid the body effect. Second, while all devices are in either diode- or cross-diode connection, an elevated supply voltage (V_{DD}) can effectively enlarge the signal swing of inner nodes while improving the linearity due to more overdrive voltages. Simulations show that the input-referred 3rd-order intercept point (IIP3) of the FDAI is +9.1 dBm at 1.8 V (90% of V_{DD}), +10.7 dBm at 2 V, and +11.8 dBm at 2.2 V (110% of V_{DD}). When the FDAI is interfaced with other devices to form a high-order LPF, the IIP3 can be better as both the input and output ports will be loaded by other low impedance nodes. Due to such loading effects, like other ladder LPFs, the noise and linearity of the LPF that adopt more than one FDAI can only be examined as a whole. The overall complexity, however, renders the assessments of linearity and noise more handable by computer simulations.

Under the following sizing parameters: $W_{1l,r}/L_{1l,r} = W_{2l,r}/L_{2l,r} = 12/0.3$ μm, $W_{3l,r}/L_{3l,r} = 24/0.3$ μm, and $C_y/2 = 24.5$ pF, the emulated inductance (L) is useful over a wide spectrum as shown in Fig. 4(a). For the $V_{\mathrm{xp},n}$ nodes,

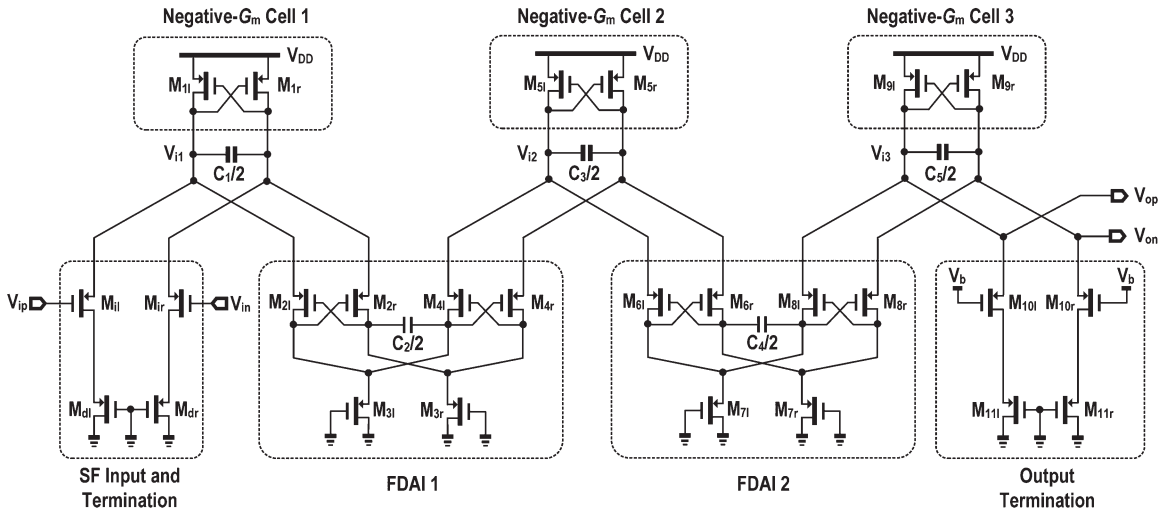


Fig. 5. Realized fifth-order transistorized-LC-ladder LPF using SF for double termination and Q-enhanced FDAIs for the floating inductors.

under a fixed width of $M_{2l,r}$ (i.e., $W_{2l,r} = 12\ \mu$m), sizing the width of $M_{1l,r}$ ($W_{1l,r}$) can easily adjust the $Q_{L,\mathrm{en}}$ as shown in Fig. 4(b). The technique holds also for the $V_{\mathrm{zp},n}$ nodes with respect to the size ratio of $M_{4l,r}$ and $M_{5l,r}$.

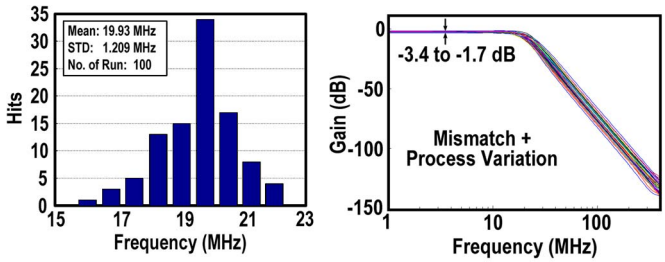
III. Implementation and Simulation Results of a Fifth-Order LPF Prototype

The design example is a transistorized fifth-order LPF as shown Fig. 5. It is transformed from the LC-ladder topology. The input termination is a first-order SF ($M_{\mathrm{dl},r} - M_{\mathrm{il},r}$) for its high linearity and high input impedance. The output termination exploits an SF replica ($M_{10l,r} - M_{11l,r}$) balancing the bias and parasitics. Three current-reuse negative G_m cells ($M_{1l,r}$, $M_{5l,r}$, and $M_{9l,r}$) are adopted at the I/O ports of the two FDAIs ($M_{2l,r} - M_{4l,r}$ and $M_{6l,r} - M_{8l,r}$) for current-reuse Q enhancement. These three negative G_m cells can be made switchable for Q tuning of the LPF.

The inner nodes have no explicitly assigned gain to reduce the footsteps of nonlinearity. The frequency response is mainly determined by the width ratio of MOSFETs and the capacitors $C_1 - C_5$. Needless of any CMFB, the stability is ensured as every inner node features at least some parasitic conductance (g_{ds}). Unlike the traditional Op-Amp-based active-RC LPF, here, all capacitors can be differentially connected to save the chip area. The filter selectivity is easily expandable by repeating the interstage FDAIs. Lack of explicit bias current sources, the LPF relies on the differential balancing to reject the even-order distortion and common-mode noises.

As expected, the inner nodes of the LPF are stable in SFDR. From simulations, the voltage gains at V_{i1}, V_{i2}, and V_{i3} are -0.6, -1.2, and -2.1 dB, and the corresponding SFDR are 54.9, 58.4, and 58.2 dB, respectively.

The LPF under 100-time Monte Carlo simulations with mismatch plus process variations exhibits a mean of $f_{-3\ \mathrm{dB}}$ at 19.93 MHz and a fair intrinsic standard deviation of 1.209 MHz [Fig. 6(a)]. If a higher bandwidth accuracy is required, the LPF can incorporate with a general bandwidth tuning loop to set the cutoff frequency, via replacing $C_1 - C_5$ with capacitor banks. The tradeoff is on the area efficiency. In this brief, the bandwidth and Q of this LPF were not designed for tunability. The simulated passband gain variation is within -1.7 to -3.4 dB [Fig. 6(b)].



(a) (b)

Fig. 6. One-hundred-time Monte Carlo simulation results: (a) $f_{-3\ \mathrm{dB}}$ variation and (b) the passband gain variation.

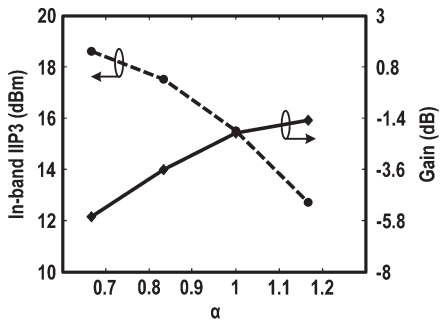


Fig. 7. Tradeoff between gain and in-band IIP3 with respect to α, which represents the conversion capability from the input signal to the FDAI 1.

The width ratio between $M_{\mathrm{il},r}$ ($W_{\mathrm{il},r}$) and $M_{2l,r}$ ($W_{2l,r}$) in the FDAI 1 can be defined α. This parameter represents the conversion capability from the input signal to the FDAI 1 as shown in Fig. 7. An aggressive α boosts the gain but penalizing the IIP3. Thus, $\alpha = 1$ is selected in this work to balance both. Simulation results show that the IIP3 of the fifth-order LPF is $+16$ dBm and passband gain is -2.1 dB.

TABLE I
SIMULATED PERFORMANCES OVER PROCESS CORNERS, VOLTAGES, AND TEMPERATURES

V_{DD}=2V, Temp=27°C	SS	TT	FF
DC Gain (dB)	–1.7	–2.1	–2.8
–3dB BW (MHz)	18	20	21.2
IRN (nV/√Hz)	14.8	14	13.8
IIP3 (dBm)	14.2	16.2	12.7
SFDR (dB)	56.8	58.2	55.8
Power (mW)	5.41	6.75	8.25

Temp=27°C, TT	V_{DD}=1.8 V	V_{DD}=2 V	V_{DD}=2.2 V
DC Gain (dB)	–1.3	–2.1	–2.9
–3dB BW (MHz)	18.7	20	21.1
IRN (nV/√Hz)	13.9	14	15.1
IIP3 (dBm)	12.1	16.2	15
SFDR (dB)	55.7	58.2	56.8
Power (mW)	4.33	6.75	9.95

V_{DD}=2V, TT	0 °C	27 °C	80 °C
DC Gain (dB)	–1.8	–2.1	–2.7
–3dB BW (MHz)	21.1	20	18.3
IRN (nV/√Hz)	11.9	14	17.7
IIP3 (dBm)	15.9	16.2	12.4
SFDR (dB)	58.8	58.2	54.5
Power (mW)	6.75	6.75	6.76

Table I summarizes the key performance metrics of the LPF over process corners, $V_{\rm DD}$, and temperature variations. Most data vary acceptably small indicating the robustness of the LPF. Among them, a lower $V_{\rm DD}$ of 1.8 V is more crucial to SFDR (dropped by 2.5 dB) as it influences both the transistor overdrives and power consumption. A potential solution for it is to adopt an on-chip stable supply or resorting via an off-chip low dropout regulator (e.g., TPS742xx).

IV. MEASUREMENT RESULTS

The LPF was fabricated in a 90-nm CMOS process with 2-fF/μm^2 capacitance density. The chip micrograph is shown Fig. 8. The LPF using the Butterworth approximation occupies a die size of 0.13 mm^2. The measured dc gain is -2.1 dB as shown in Fig. 9(a), and the input-referred noise density is 14.1 nV/$\sqrt{}$Hz as shown in Fig. 9(b). Both results are in good agreement with the typical simulation results, confirming the robust shape of the proposed active LC-ladder topology. Since the $V_{\rm DD}$ is shared among three cascode devices (see Fig. 5), a 2-V $V_{\rm DD}$ effectively enlarges the device overdrive (i.e., better linearity) with no reliability risk (confirmed by rigorous transient simulations with node-voltage trajectory checks [11]). A two-tone test at 7 and 8 MHz measures the in-band 3rd-order intermodulation distortion (IM3) as shown in Fig. 10(a), which corresponds to an IIP3$_{\rm in-band}$ of $+16$ dBm. The test is repeated with two tones at other frequencies (f_1 and f_1+1 MHz) measuring the full IIP3$_{\rm in-band}$ profile as shown in Fig. 10(b). The IIP3$_{\rm out-of-band}$ is obtained with two out-of-band tones at (20, 34), (30, 54), and (80, 154) MHz; all generate an IM3 at 6 MHz.

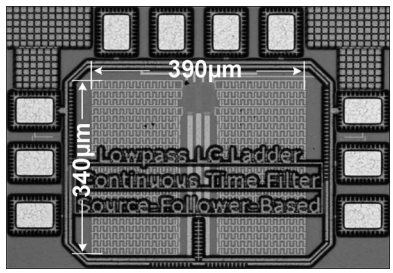


Fig. 8. Chip micrograph.

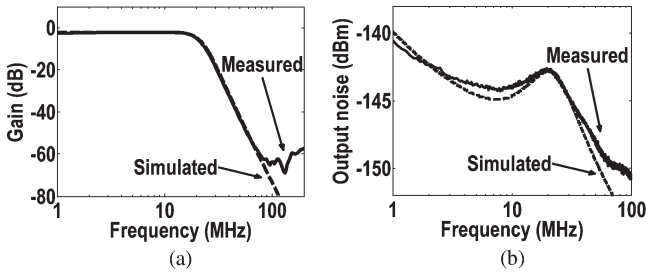


Fig. 9. Measured and simulated (a) frequency response and (b) noise response.

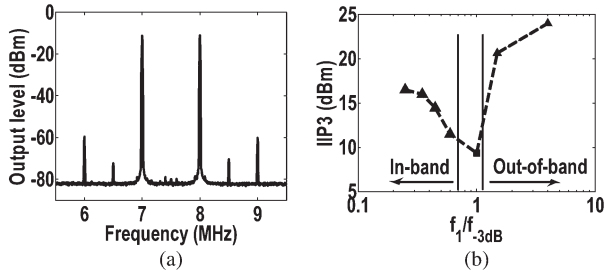


Fig. 10. (a) In-band two-tone test at 7 and 8 MHz (tones at 6.5 and 8.5 MHz are from equipment Agilent E4438C). (b) In-band and out-band IIP3 profile.

Table II shows the chip summary and benchmarks the work to the state of the art having over a 10-MHz $f_{-3\ \rm dB}$ [1], [12]–[17]. This transistorized-LC-ladder LPF using SF and FDAI techniques is highly competitive for its high SFDR (58.2 dB), high selectivity efficiency (68 μW/pole/MHz), and small die size (0.13 mm^2).

V. CONCLUSION

This brief has described the design and implementation of a transistorized-LC-ladder LPF built by SF and Q-enhanced FDAI techniques. It features a small number of active devices and, thereby, less source of nonlinearity and noise than the conventional Op-Amp-based solutions. The robust frequency response against process variations and component mismatches is due to the correlated feature of LC-ladder topology. The proof-of-concept fifth-order 20-MHz LPF prototype measures 58.2-dB SFDR with 6.8 mW of power. The selectivity efficiency is 68 μW/pole/MHz, and the die size is 0.13 mm^2 in a 90-nm CMOS process.

TABLE II
PERFORMANCE SUMMARY AND BENCHMARK WITH THE STATE OF THE ART

	[1] JSSC'06	[12] JSSC'09	[13] JSSC'09	[14] JSSC'11	[15] TCASII'11	[16] CICC'10	[17] JSSC'11	This Work
Technology CMOS	0.18μm	0.13μm	0.18μm	90nm	0.18μm	0.13μm	0.18μm	90nm
Topology	SF	G_m-RC	G_m-C	G_m-C	Active-RC	Active-RC	Active-RC	SF + FDAI
Filter Type	Bessel	Butterworth	Butterworth	Butterworth	Elliptic	Elliptic	Chebyshev	Butterworth
DC Supply (V)	1.8	0.55	1.2	1	1.8	1.2	1.8	2
Chip area (mm^2)	0.26	0.43	0.23	0.239	0.17	0.1	0.22	0.133
Power (mW)	4.1	3.5	11.1	4.35	1.8	5.8	4.5	6.8
Filter Order (Pole)	4	4	3	6	3	4	5	5
f_{-3dB} (MHz)	10	11.3	20	8.1 - 13.5	17	17.5	20	20
Power/Pole/f_{-3dB} (μW/Pole/MHz) @ f_{-3dB}	102.5 @ 10 MHz	77.4 @ 11.3 MHz	185 @ 20 MHz	53.7 @ 13.5 MHz	35.3 @ 17 MHz	82.9 @ 17.5 MHz	45 @ 20 MHz	68 @ 20 MHz
DC Gain (dB)	-3.5	0	0	-2.8	-0.4	0	0	-2.1
$IIP3_{In\text{-}band}$ (dBm)	17.5	10	19	21.7 - 22.1	28.2	N/A	43.3	16 [1]
$IIP3_{Out\text{-}of\text{-}band}$ (dBm)	N/A	13	13	17.5 - 18.9	N/A	N/A	N/A	24 [2]
IRN (nV/√Hz)	7.5	33	12	75	170	N/A	219.1	14.1
$SFDR_{in\_band}$ [3] (dB)	64.7	50.7	60.9	54.4	51.5	N/A	60.3	58.2
FOM [4]	0.035	0.659	0.15	0.244	0.25	N/A	0.042	0.103

[1] Two tones at 7 and 8 MHz. [2] Two tones at 30 and 54 MHz.
[3] $FDR_{in\_band} = (IIP3_{in\_band}/PN)^{2/3}$ where PN is the input referred noise power. [4] FOM= Power/(Order × SFDR × f_{-3dB}).

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