

# Fully Integrated Inductor-Less Flipping-Capacitor Rectifier for Piezoelectric Energy Harvesting

Zhiyuan Chen, Man-Kay Law, *Senior Member, IEEE*, Pui-In Mak, *Senior Member, IEEE*,  
Wing-Hung Ki, *Member, IEEE*, and Rui P. Martins, *Fellow, IEEE*

**Abstract**—This paper presents a fully integrated piezoelectric energy harvesting interface without external components. Instead of relying on bulky external inductors with high quality factor as in the conventional parallel-synchronized-switch harvesting-on-inductor (P-SSHI) approach, we propose a flipping-capacitor rectifier (FCR) topology to achieve voltage inversion of the piezoelectric energy harvester through a reconfigurable capacitor array. This fundamentally preserves a fully integrated solution without inductors while achieving a high-energy extraction capability. Measurement results from FCR<sub>1</sub> using discrete components shows an output power enhancement of up to 3.4×, which is close to the theoretical prediction. We also fabricated a seven-phase FCR<sub>3</sub> with four MIM capacitors and 21 switches using a 0.18-μm 1.8/3.3/6 V CMOS process, occupying an active area of ~1.7 mm<sup>2</sup>. Additionally, we implemented an active rectifier based on a common-gate comparator with phase alignment to ensure high-speed operation while minimizing the diode voltage drop. A phase generate-and-combine circuit eliminates redundant switching activities. Systematic optimization of the three main energy loss mechanisms during the finite flip time: 1) phase offset; 2) incomplete charge transfer; and 3) reduced conduction time, is also introduced. Measurement results show that the output power enhancement can reach up to 4.83× at an excitation frequency of 110 kHz.

**Index Terms**—CMOS, deep-tissue implant, flipping-capacitor rectifier (FCR), fully integrated, high efficiency, inductor-less, parallel-synchronized-switch harvesting-on-inductor (P-SSHI), piezoelectric energy harvesting, reconfigurable capacitor array, ultrasound.

## I. INTRODUCTION

ENERGY harvesting is becoming an attractive alternative to conventional battery-powered systems, especially for miniaturized implants where energy availability is scarce. Due

to the application specific requirement, biomedical implants generally exhibit stringent system size and energy bottlenecks and highly efficient energy generation approaches are becoming a necessity. Many existing implantable systems, including retinal prosthesis [1], intraocular pressure monitoring [2], cochlear implants [3], subcutaneous glucose monitoring [4], and micro-oxygenator [5], can benefit from scavenging energy from ambient sources to achieve minimal invasiveness and extend the system lifetime. RF inductive coupling is generally desirable due to its portability and high energy transfer efficiency. Yet, the hard tradeoff between the antenna size and the substantial tissue attenuation makes it inconvenient in many deep-tissue implant applications [6]. For large distance (>1 cm) and small implants (<1 cm diameter), the ultrasonic method outperforms inductive coupling due to the improved coupling efficiency as a result of the significantly shorter wavelength [6]. Moreover, energy scavenging using piezoelectric energy harvesters (PEHs) from an external ultrasound source also ensures much relaxed directionality requirement [5].

In case of vibration energy harvesting, PEH is a popular choice due to its high power density, high scalability, and high output voltage generation [7]. When the PEH is subjected to mechanical vibrations, stress is induced within the material, thus giving rise to an electromotive force that generates harvestable electrical charge. The PEH can be modeled as a spring-mass-damper system [8]. Fig. 1 shows the application scenario of an ultrasound energy harvesting implantable system using a PEH. The equivalent electromechanical model of a PEH can be reduced to a dependent current source  $I_p$  in parallel with the inherent piezoelectric capacitor  $C_p$ . Here,  $I_p$  depends on the PEH mechanical properties, with  $L_M$ ,  $C_M$ , and  $R_M$  representing the effective mechanical mass, the inverse of the spring stiffness, and the mechanical loss, respectively. Fig. 2 shows the commonly used approaches to extract energy from the PEH. They are: 1) the full bridge rectifier (FBR); 2) the switch only rectifier (SOR); and 3) the parallel-synchronized-switch harvesting-on-inductor (P-SSHI). Fig. 2 also presents the circuit implementations and the illustrative current and voltage waveforms. In [5], the FBR is implemented with discrete components to convert the PEH ac current into a dc output voltage. However, the charge loss of the PEH parasitic capacitor  $C_p$  due to voltage inversion ( $Q_{\text{loss}}$ ) limits the energy extraction capability. The SOR resolves this problem by simply shorting the PEH during the zero crossing of  $I_p$ . As a result, the voltage change in  $C_p$  is only  $V_{\text{rect}}$  instead of  $2V_{\text{rect}}$ , effectively doubling the extracted power.

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Z. Chen and P.-I. Mak are with the State Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macau 999078, China (e-mail: mklaw@umac.mo).

M.-K. Law is with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau 999078, China (e-mail: mklaw@umac.mo).

W.-H. Ki is with the Department of Electronics and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong 999077.

R. P. Martins is with the State Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macau 999078, China, and also on leave from the Instituto Superior Técnico/Universidade de Lisboa, 1049-001 Lisbon, Portugal.

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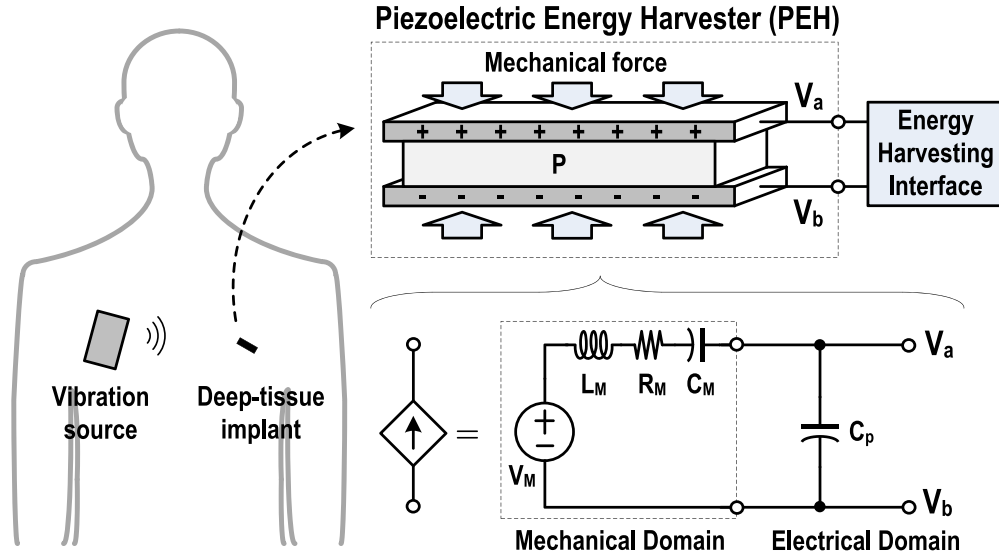


Fig. 1. System overview of an ultrasound energy harvesting implantable system using a PEH, together with the equivalent electromechanical model of the PEH.

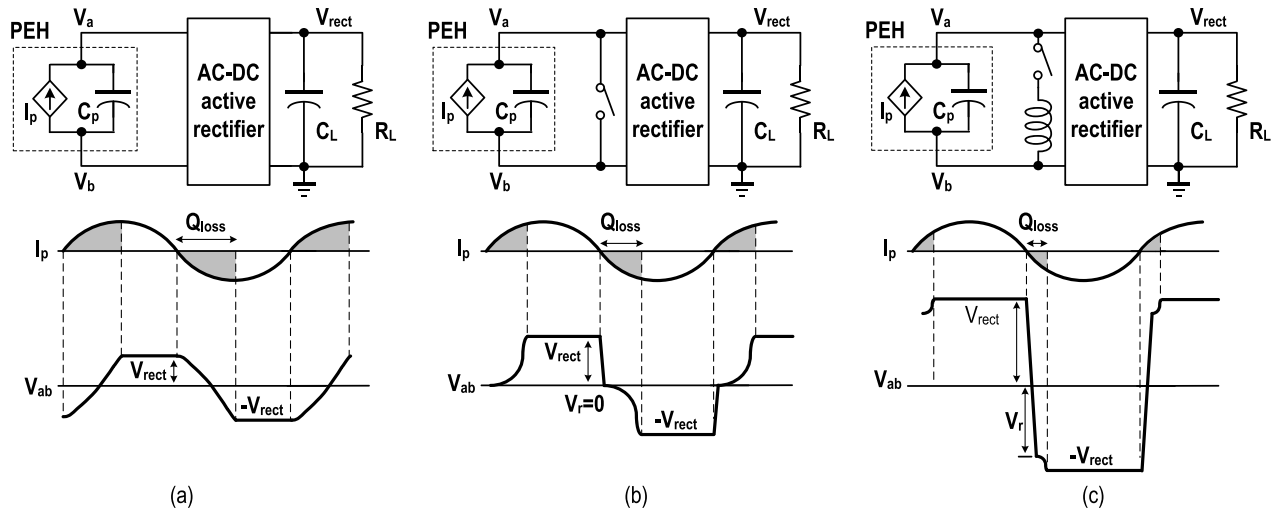


Fig. 2. Commonly used piezoelectric energy harvesting interfaces with the corresponding current and voltage waveforms. (a) FBR. (b) SOR. (c) P-SSHI.

To extract more energy from the PEH, the P-SSHI [7], [9], [10] swiftly flips the voltage across  $C_p$  using  $LC$  resonance, effectively increasing the conduction period and enhancing the extractable energy. Yet, this approach requires a large inductor (up to the millihenry range in [7]) with high quality factor ( $Q$ ) to achieve a high rebuilt voltage ( $V_r$ ) for reducing  $Q_{loss}$ . This defeats its viability in deep-tissue implants due to the lack of on-chip high- $Q$  inductors. Apart from that, it also imposes the restriction that the excitation frequency ( $f_{EX}$ ) is much lower than the  $LC$  resonance frequency, i.e., the flip time ( $t_{flip}$ ) required to reverse the PEH voltage during the zero crossing of  $I_p$  is short. In case of ultrasound energy harvesting, the excitation frequency can be in the order of tens of kilohertz to megahertz, which can essentially jeopardize the selection of large high- $Q$  inductors to increase the extracted power.

This paper, an expanded version of [11], presents a fully integrated flipping-capacitor rectifier (FCR) for piezoelectric energy harvesting. It requires no external high- $Q$  inductor and is suitable for deep-tissue implant applications. By harvesting the PEH energy off-resonance at a lower frequency, an increased penetration depth can be achieved, leading to an improved power transmission efficiency without sacrificing the data transmission bandwidth at the system level. Two FCRs, the FCR<sub>1</sub> using discrete components and the FCR<sub>3</sub> that is fully integrated using on-chip MIM capacitors, are implemented to validate the effectiveness of our proposed FCR topology for ultrasound energy harvesting. The rest of this paper is organized as follows. Section II discusses the design and analysis of the FCR topology. Section III outlines the system architecture of the proposed PEH system with the detailed discussion of each building block. Section IV summarizes the

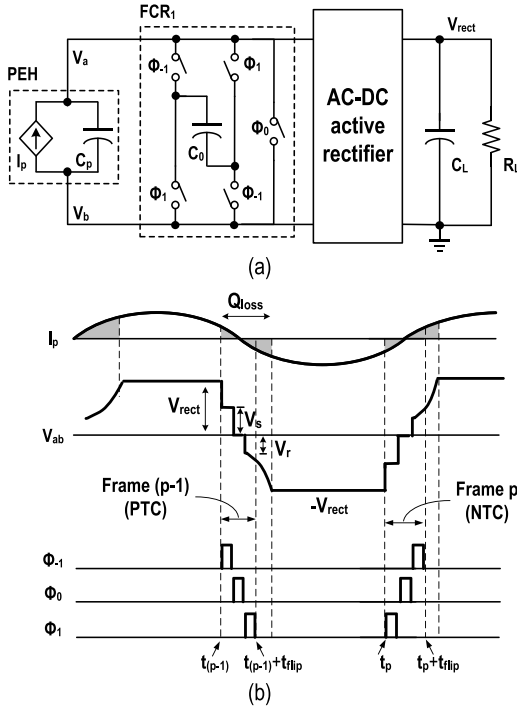


Fig. 3. (a) Proposed FCR1 implementation. (b) Current, voltage, and control phase waveforms, with the PTC ( $t_{(p-1)} \sim t_{(p-1)} + t_{flip}$ ) and NTC ( $t_p \sim t_p + t_{flip}$ ) as shown.

measurement results. Finally, Section V concludes the research efforts.

## II. DESIGN AND ANALYSIS OF THE PROPOSED FCR TOPOLOGY

As observed in Fig. 2, the P-SSHI achieves increased PEH extracted power by swiftly recycling the energy in  $C_p$  to reverse the PEH polarity. A large  $V_r$  is essential to reduce  $Q_{loss}$  and increase the conduction time. Based on this observation, our proposed FCR topology achieves PEH voltage inversion during the zero crossing of  $I_p$  through a reconfigurable capacitor array. Consequently, a high-Q inductor as the energy storage element can be eliminated, realizing a low-cost, highly compact, and fully integrated solution. This section outlines the basic FCR operations, and conducts detailed analysis on its performance for piezoelectric energy harvesting. To simplify the mathematical derivations while extracting design insights, we make the following three assumptions: 1) the diode voltage drop in the rectification stage is negligible; 2) all the switches and capacitors have negligible parasitic loss; and 3)  $t_{flip}$  is short but ensures complete charge transfer. In a practical implementation, these parameters can lead to loss in system efficiency, and the corresponding circuit design considerations will be discussed in Section III.

### A. FCR With One Capacitor

Fig. 3(a) shows the basic form FCR1 that utilizes only one flipping capacitor  $C_0$  and five switches. The corresponding voltage, current, and phase control waveforms for both the positive transition cycle (PTC) and the negative transition cycle (NTC) are illustrated in Fig. 3(b). Due to symmetrical operations, we only need to study the FCR1 during the NTC,

i.e., frame  $p$  from  $t_p$  to  $t_p + t_{flip}$  in Fig. 3(b). Based on the direction of charge flow, the FCR operations can be sub-divided into three phases: 1) the sharing phase ( $\Phi_{-1}$ ), when the charge in  $C_p$  is redistributed to  $C_0$ ; 2) the shorting phase ( $\Phi_0$ ), when  $C_p$  is completely discharged; and 3) the recharging phase ( $\Phi_1$ ), when  $C_p$  is recharged in the opposite direction through  $C_0$ . In order to quantify the performance improvement of FCR1, we calculate the theoretical maximum output power as follows. In the steady state, the rectifier output voltage is equal to  $V_{rect}$ . The PEH voltages ( $V_{ab}$ ) at the end of the current sharing and recharging phases (i.e., frame  $p$ ) are defined as  $V_s$  and  $V_r$ , respectively. Based on charge conservation, the charge balancing equations for  $\Phi_{-1}$  and  $\Phi_1$  can be expressed as

$$V_s(C_p + C_0) = C_p V_{rect} + C_0 V_r' \quad (1)$$

$$V_r(C_p + C_0) = C_0 V_s \quad (2)$$

where  $V_r'$  is the rebuilt voltage at the end of the previous recharging phase [i.e., frame (p-1)]. As  $V_r = V_r'$  during the steady state, we obtain

$$k_{FCR1} = \frac{V_r}{V_{rect}} = \frac{1}{2 + \frac{C_p}{C_0}} \quad (3)$$

where  $k_{FCR1}$  denotes the ratio between the PEH rebuilt voltage and the rectifier voltage within one FCR operation cycle, which is a direct indication of the power extraction efficiency. To estimate the maximum output power achievable by FCR1, with a total charge  $Q_{out}$  transferred to the output, the output power delivered by the PEH operating at an excitation frequency  $f_{EX}$  is computed as

$$P_{out} = Q_{out} V_{rect} \times 2f_{EX}. \quad (4)$$

During half of a switching cycle, the charge transferred to the output is the difference between the charge generated by the PEH and the loss in charge, that is

$$Q_{out} = 2C_p V_p - Q_{loss} \quad (5)$$

where  $V_p$  is the PEH open-circuit voltage. Note that  $Q_{loss}$  is due to the recharging of  $C_p$  from  $V_r$  to  $V_{rect}$ , it is

$$Q_{loss} = C_p (V_{rect} - V_r). \quad (6)$$

Combining (3) to (6) leads to

$$P_{out} = 2C_p V_{rect} f_{EX} (2V_p - (1 - k_{FCR1}) V_{rect}). \quad (7)$$

By differentiating (7) with respect to  $V_{rect}$  and equating the result to zero, it can be proved that the FCR1 output power is maximum when  $V_{rect} = V_p / (1 - k_{FCR1})$  and

$$P_{FCR1, max} = \frac{2C_p V_p^2 f_{EX}}{1 - k_{FCR1}}. \quad (8)$$

The above equation indicates that the FCR1 maximum output power is only dependent on  $k_{FCR1}$  (as  $C_p$ ,  $V_p$ , and  $f_{EX}$  are fixed for a particular PEH under a predetermined excitation frequency). As verified in [10], the maximum output power for FBR and SOR are  $C_p V_p^2 f_{EX}$  and  $2C_p V_p^2 f_{EX}$ , respectively. The

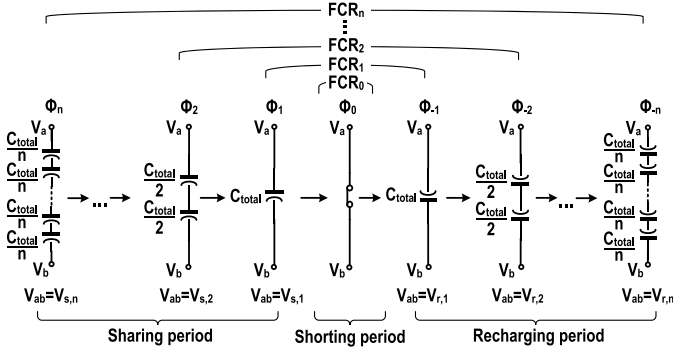


Fig. 4. Capacitor configurations for different FCR implementations in one PTC.

performance of the proposed FCR<sub>1</sub> can be quantitatively compared with FBR using the maximum output power improving rate (MOPIR) [10] that can be calculated as

$$\text{MOPIR}_{\text{FCR}_1} = \frac{P_{\text{FCR}_1, \max}}{P_{\text{FBR}, \max}} = \frac{2}{1 - k_{\text{FCR}_1}}. \quad (9)$$

From (9),  $C_0 = 0$  in the case of SOR, which leads to  $k_{\text{FCR}_1} = 0$  and an MOPIR of 2. This result is consistent with that obtained in [10]. For our proposed FCR<sub>1</sub>, from (3),  $k_{\text{FCR}_1}$  converges to  $1/2$  as  $C_0 \rightarrow \infty$ , and (9) exhibits an asymptotic limit of 4. This corresponds to  $2\times$  performance improvement when compared to that of SOR. The limited MOPIR with large  $C_0$  in FCR<sub>1</sub> can be fundamentally improved by FCR<sub>n</sub>, as described in the following section.

### B. Generalized FCR<sub>n</sub> Topology

As discussed in Section II-A, the MOPIR of FCR<sub>1</sub> is closely related to  $k_{\text{FCR}_1}$ . In fact, a higher MOPIR can be achieved by boosting the PEH voltage through reconfiguring an increased number of flipping capacitors. Specifically, Fig. 4 shows that FCR<sub>1</sub> can be extended to FCR<sub>n</sub> by simply using  $n$  reconfigurable capacitors with  $n$  sharing/recharging phases. Due to symmetrical operations, total number of reconfiguration phases for FCR<sub>n</sub> is  $2n + 1$ , where  $n$  is the number of switching phases in each of the sharing/recharging period. It is clear from Fig. 4 that SOR is equivalent to FCR<sub>0</sub>. Now, the total capacitance ( $C_{\text{total}}$ ) should remain constant throughout the reconfiguration cycles, and  $m$  capacitors with size  $C_{\text{total}}/m$  are connected in series in the  $m$ th sharing/recharging phase ( $m < n$ ). This ensures step-wise reconfiguration with balanced capacitance distribution to reduce charge redistribution loss. The switching phases for FCR<sub>n</sub> are denoted as  $\Phi_{-n}, \Phi_{-(n-1)}, \dots, \Phi_{-1}, \Phi_0, \Phi_1, \dots, \Phi_{(n-1)}, \Phi_n$ . We further define the PEH voltage ( $V_{\text{ab}}$ ) at the end of the current  $m$ -th sharing ( $\Phi_{-m}$ ) and recharging phase ( $\Phi_m$ ) as  $V_{s,m}$  and  $V_{r,m}$ , respectively. Similar to Section III-A, we can evaluate the power extraction efficiency of FCR<sub>n</sub> based on charge conservation. During the current sharing period, the charge balancing equations for  $\Phi_{-n}$  and

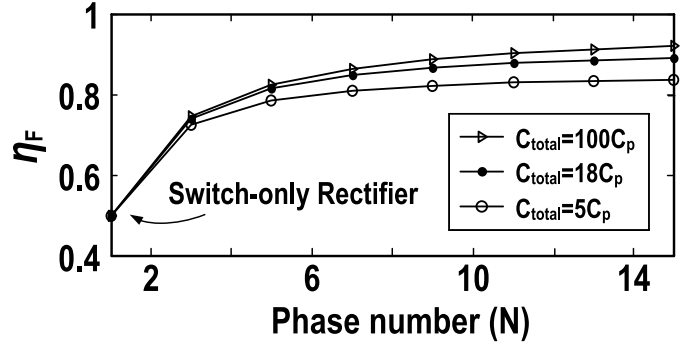


Fig. 5. Theoretical voltage flipping efficiency ( $\eta_F$ ) versus different phase number ( $N$ ), with  $C_{\text{total}}/C_p = 5, 18$ , and  $100$ .

the general case  $\Phi_{-m}$  are

$$V_{s,n} \left( C_p + \frac{1}{n^2} C_{\text{total}} \right) = C_p V_{\text{rect}} + \frac{C_{\text{total}}}{n^2} V'_{r,n} \quad (10)$$

$$V_{s,m} \left( C_p + \frac{1}{m^2} C_{\text{total}} \right) = C_p V_{s,m+1} + \frac{C_{\text{total}}}{m(m+1)} V_{s,m+1} \quad (11)$$

where  $m = 1, 2, \dots, n-1$ , and  $V'_{r,n}$  is the rebuilt voltage at the end of the previous recharging period. Note that the term  $C_{\text{total}}/m^2$  of (11) is the equivalent capacitance of the flipping capacitor in the  $m$ -th sharing phase, while the coefficient  $m(m+1)$  is due to the reconfiguration of the flipping capacitor (from  $(m+1)$  to  $m$  capacitors connected in series). Similarly, during the current recharging period, the charge conservation equations for  $\Phi_n$  and the general case  $\Phi_m$  are

$$V_{r,n} \left( C_p + \frac{1}{n^2} C_{\text{total}} \right) = C_{\text{total}} V_{r,1} \quad (12)$$

$$V_{r,m+1} \left( C_p + \frac{1}{m^2} C_{\text{total}} \right) = C_p V_{r,m} + \frac{C_{\text{total}}}{m(m+1)} V_{r,m}. \quad (13)$$

During the steady state,  $V'_{r,n} = V_{r,n}$  and we obtain

$$k_{\text{FCR}_n} = \frac{V_r}{V_{\text{rect}}} = \left[ \frac{(1+x)^2}{x} \prod_{m=1}^{\frac{N-3}{2}} \frac{\left(1 + \frac{x}{(m+1)^2}\right)^2}{\left(1 + \frac{x}{(m+1)m}\right)^2} - \frac{4x}{(N-1)^2} \right]^{-1} \quad (14)$$

where  $x = C_{\text{total}}/C_p$  is the ratio of the total flipping capacitor size to the PEH parasitic capacitor, and  $N = 2n + 1$  is the number of phases ( $n = 0$  is the special case for SOR). From (14), it is noted that a larger  $k_{\text{FCR}_n}$  (and hence a higher power extraction improvement) can be achieved by increasing  $C_{\text{total}}$  and  $N$ . By substituting (14) into (8), the MOPIR of an arbitrary FCR implementation can be determined. The voltage flipping efficiency ( $\eta_F$ ) defined in [7] is closely related to  $k_{\text{FCR}_n}$ . With a negligible rectifier diode drop, it is defined as

$$\eta_F = \frac{V_r + V_{\text{rect}}}{2V_{\text{rect}}}. \quad (15)$$

Fig. 5 shows  $\eta_F$  with respect to the phase number ( $N$ ) when  $C_{\text{total}}/C_p = 5, 18$ , and  $100$ . As expected, the achieved  $\eta_F$  improves as  $N$  and  $C_{\text{total}}/C_p$  increases. Fig. 6 summarizes the theoretical MOPIR with respect to different  $C_{\text{total}}/C_p$



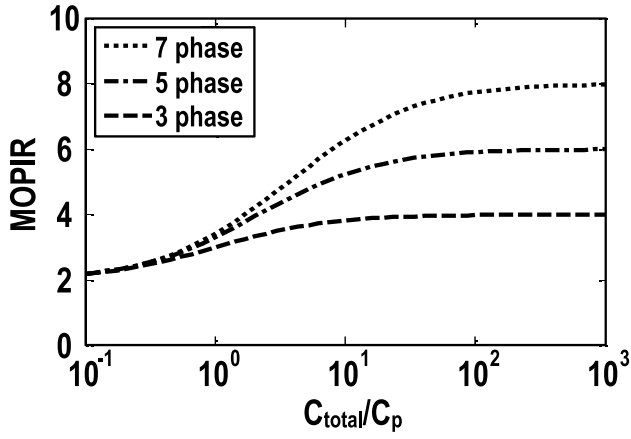


Fig. 6. Theoretical MOPIR versus different  $C_{\text{total}}/C_p$ , with phase number ( $N$ ) = 3, 5, and 7.

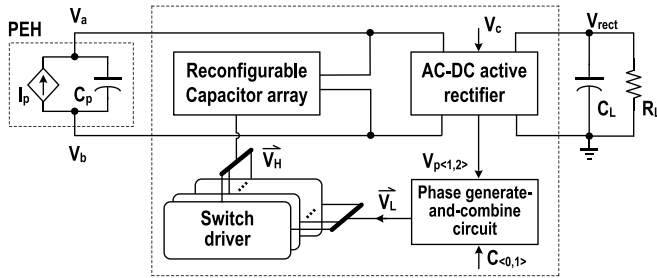


Fig. 7. Block diagram of the proposed fully integrated inductor-less PEH system using FCR<sub>3</sub>.

ratios when  $N = 3, 5$ , and  $7$ . By using (9) and (14), the maximum achievable MOPIR by FCR<sub>1-3</sub> are 4, 6, and 8, respectively. Moreover, the output power can be improved by increasing  $C_{\text{total}}$  and  $N$  for a particular PEH, but the improvement flattens off as  $C_{\text{total}}$  becomes much larger than  $C_p$ . A large  $C_{\text{total}}$  means an increase in chip area that is undesirable for the target application. Moreover, as  $N$  increases, the associated increase in the circuit complexity can lead to a higher switching loss that limits the achievable MOPIR. Besides, the achievable system efficiency improvement of FCR <sub>$n$</sub>  can also be degraded due to parasitics, which can result in a reduced  $k_{\text{FCR}_n}$  in (14).

### III. PROPOSED SEVEN-PHASE FLIPPING-CAPACITOR RECTIFIER

To validate the proposed concept, we designed a fully integrated seven-phase FCR. Existing biomedical applications typically require power levels from a few microwatt to a few milliwatt [12]. In this paper, we target at an output power of  $\sim 50 \mu\text{W}$  with a PEH size of  $1 \times 1 \times 5 \text{ mm}^3$  using PSI-5A4E (Piezo Systems, Inc.). The parasitic capacitance  $C_p$  is estimated to be  $\sim 80 \text{ pF}$ . In the chosen  $0.18\text{-}\mu\text{m}$   $1.8/3.3/6 \text{ V}$  CMOS process, the on-chip MIM capacitor density is  $1 \text{ fF}/\mu\text{m}^2$ . This translates to an area requirement of roughly  $1.44 \text{ mm}^2$  for  $C_{\text{total}} = 18 C_p$ , which is feasible for fully on-chip implementation.

Fig. 7 shows the system level block diagram that consists of a reconfigurable capacitor array, an active rectifier, a phase

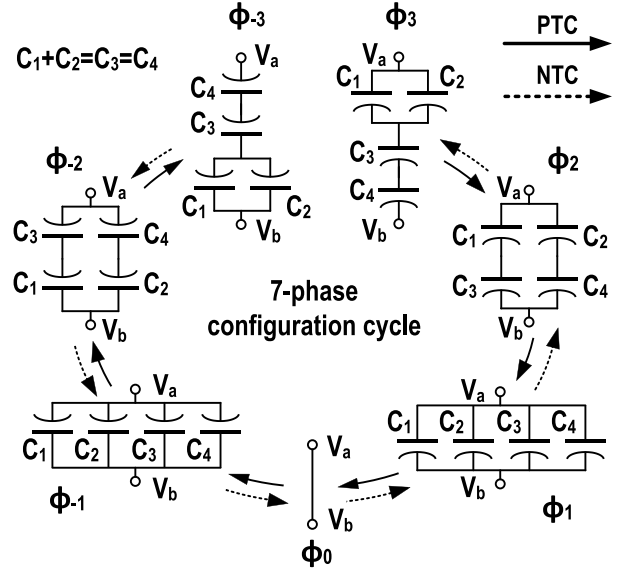


Fig. 8. Seven-phase FCR<sub>3</sub> reconfiguration cycle for both PTC and NTC.

generate-and-combine circuit, and switch drivers. The capacitor array is composed of four flipping MIM capacitors that realize the seven configurations when reversing the voltage across  $C_p$  during the zero crossing of  $I_p$ . The active rectifier rectifies the ac voltage of the harvester while ensuring phase alignment. The phase generate-and-combine circuit produces the required control signals that are level shifted by the switch drivers to ensure proper switching on and off operations, while redundant switching activities are eliminated by phase combining to improve the system efficiency. In this paper,  $C_{\text{total}}/C_p$  and  $N$  are set to 18 and 7, respectively. This design choice can balance the energy extraction efficiency, the area overhead and the design complexity, while achieving a theoretical  $\eta_F$  of 0.85 (Fig. 5) and MOPIR of  $6.85 \times$  (Fig. 6). Detailed discussions about each individual building block are outlined next.

#### A. Reconfigurable Capacitor Array

Fig. 8 illustrates the capacitor reconfiguration cycles of the proposed seven-phase FCR<sub>3</sub>. We denote the number of series-connected flipping capacitors in each phase as (3, 2, 1, 0, -1, -2, -3) during the PTC and (-3, -2, -1, 0, 1, 2, 3) during the NTC, respectively, with the sign indicating the polarity of the flipping capacitors with respect to  $C_p$ . To ensure balanced branch capacitance during the step-wise reconfiguration cycles, we utilize a total of four capacitors with  $2C_1 = 2C_2 = C_3 = C_4$ . On-chip MIM capacitors have parasitic top- and bottom-plate capacitances that are a few percent of the main capacitor. They incur extra energy loss that leads to reduced system efficiency. As the PEH generally exhibits negligible parasitic with reference to the substrate, this parasitic loss is mainly caused by stacking of capacitors, but is insignificant for the flipping operations (i.e.,  $\Phi_{\pm 1}$ ). Since the parasitic loss is mainly dominated by the bottom-plate capacitance, we estimated this loss by using a 5% parasitic bottom plate capacitance in simulation, and resulted in an efficiency loss of roughly 4%. After accounting for equivalent

TABLE I  
SUMMARY OF THE CONTROL PHASE FOR DIFFERENT  
CONFIGURATION SWITCHES

Switch #	Control phase						
	-3	-2	-1	0	1	2	3
$S_0$	Off	Off	Off	On	Off	Off	Off
$S_{11}$	On	On	On	Off	Off	Off	Off
$S_{12}$	Off	Off	Off	Off	On	On	On
$S_{13}$	Off	Off	Off	Off	On	Off	Off
$S_{14}$	Off	Off	On	Off	Off	Off	Off
$S_{21}$	On	Off	On	Off	Off	Off	Off
$S_{22}$	Off	Off	Off	Off	On	Off	On
$S_{23}$	Off	Off	Off	Off	On	On	Off
$S_{24}$	Off	On	On	Off	Off	Off	Off
$S_{31}$	Off	On	On	Off	Off	Off	Off
$S_{32}$	Off	Off	Off	Off	On	On	Off
$S_{33}$	Off	Off	Off	Off	On	Off	Off
$S_{34}$	Off	Off	On	Off	Off	Off	Off
$S_{41}$	Off	Off	On	Off	Off	Off	Off
$S_{42}$	Off	Off	Off	Off	On	Off	Off
$S_{43}$	Off	Off	Off	Off	On	On	On
$S_{44}$	On	On	On	Off	Off	Off	Off
$S_{i1}$	On	Off	Off	Off	Off	Off	On
$S_{i2}$	On	Off	Off	Off	Off	Off	On
$S_{i3}$	On	On	Off	Off	Off	On	On
$S_{i4}$	Off	On	Off	Off	Off	On	Off

switch connections, the complete seven-phase capacitor configuration is realized by using a total of 21 switches, with  $S_{i1-4}$  for interconnecting  $C_{1-4}$  and  $S_0$  for shorting  $C_p$ , as shown in Fig. 9. Table I tabulates the complete control sequence for each individual switch. Note that many of the switches share the same controls, and should be turned on in multiple phases. Such redundant switching activities are reduced through phase combining for improved switching loss, to be discussed in Section III-C. Due to the high excitation frequency  $f_{EX}$ , the switches are implemented using transmission gates to reduce the conduction loss during different voltage level transitions in different phases. We also utilize active body biasing to further enhance the switch conductance and to fulfill the stringent settling time requirement ( $<150$  ns with  $f_{EX} = 110$  kHz) without increasing the reversion loss. The switch drivers are a group of level converters that translates  $\bar{V}_L$  to  $\bar{V}_H$ . Two complementary bootstrapping capacitors of 50 fF each are implemented to properly turn on and off the relevant pMOS transistors from  $V_{rect}-2V_d$  to  $V_{rect}-2V_d + V_L$ , where  $V_d$  is the diode drop in Fig. 9. Capacitor flipping operation occurs during the zero crossing of  $I_p$ , and hence the operating frequency is  $2f_{EX}$ .

#### B. Active Rectifier With Phase Alignment Control

Fig. 10 shows the schematic of the active rectifier [13] for ac-dc conversion that eliminates the diode voltage drop as in a passive rectifier [10]. The equivalent diode drop is lower than 20 mV, which is less than 1% of the nominal  $V_{rect}$ . A phase alignment control circuit composed of  $M_C$ ,  $M_f$ ,

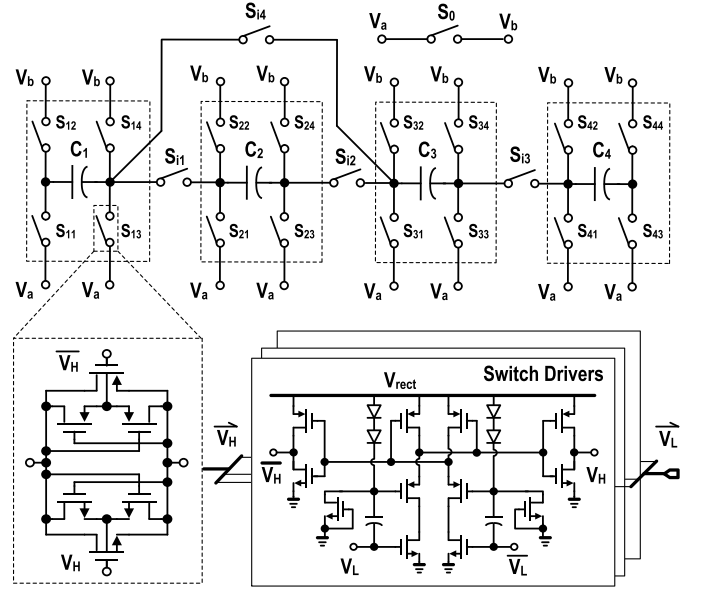


Fig. 9. Switch arrangements of the seven-phase FCR<sub>3</sub>, together with the implementation of the transmission gate with active body biasing and the switch drivers.

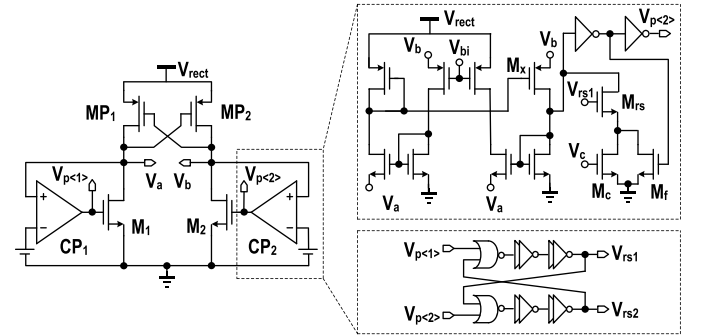


Fig. 10. Active rectifier implementation with common-gate comparator, with embedded phase alignment control using  $M_C$ ,  $M_f$ , and the SR latch.

and an SR-latch is embedded to reduce the loss due to the misalignment between the zero crossing of  $I_p$  and the PEH shorting phase  $\Phi_0$ . High speed operation is guaranteed by using a common-gate comparator.  $M_C$  is controlled by  $V_C$  externally for adjusting the current that flows through  $M_x$  (and hence the comparator offset,  $V_{offset}$ ) to achieve comparator delay tuning of roughly 8.5 ns/mV for phase alignment.  $M_f$  belongs to a positive feedback loop that guarantees fast comparator transitions. The SR latch that is controlled by  $V_{p(1,2)}$  enforces operation only during  $t_{flip}$ . Furthermore, intrinsic comparator offset is added to ensure that the FCR operation starts earlier than the transitions of  $I_p$  for aligning  $\Phi_0$  when  $I_p = 0$ , as illustrated in Fig. 11. Closed-loop  $V_C$  control can be accomplished by utilizing a maximum power point tracking circuit based on the perturb and observe method similar to [14], where the optimal  $V_C$  can be obtained by comparing two sampled output voltages at two different time instances.

Due to the high  $f_{EX}$ , reducing energy loss during  $t_{flip}$  can improve the overall energy extraction significantly. There are three main energy loss mechanisms during  $t_{flip}$ , namely: 1) loss due to the phase offset ( $t_{offset}$ ) that is defined as

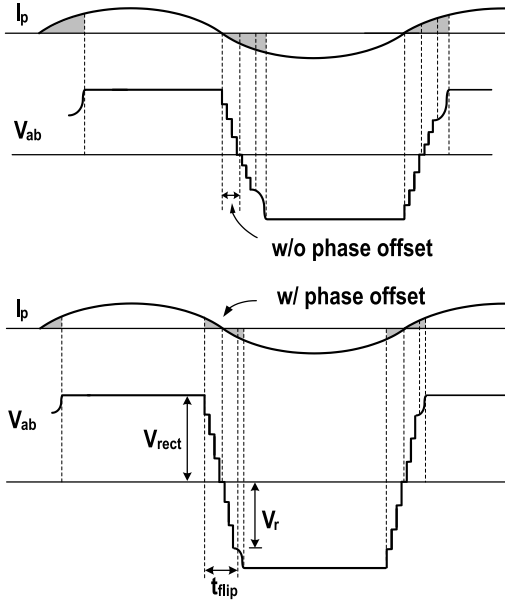


Fig. 11. FCR3 operation diagram without (top) and with (bottom) phase alignment.

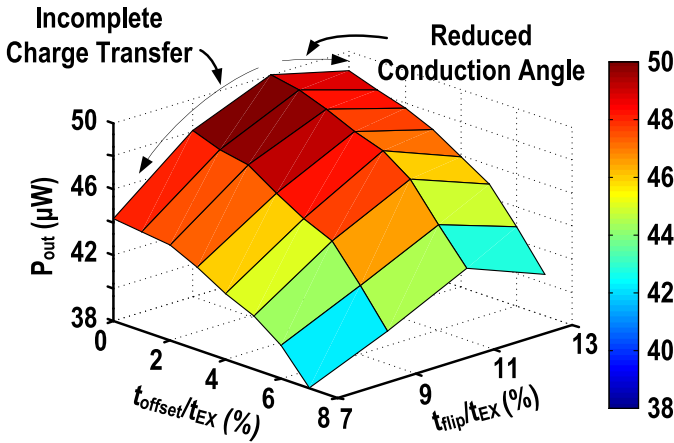


Fig. 12. Simulated variation in output power under the influence of the three main loss mechanisms during  $t_{\text{flip}}$ : (1) phase offset; (2) incomplete charge transfer; and (3) reduced conduction angle.

the time misalignment between the  $I_p$  zero crossing and the PEH shorting phase; 2) loss due to incomplete charge transfer because of insufficient settling time; and 3) loss due to reduced conduction time as a result of excessive time allocated for  $RC$  settling. Fig. 12 summarizes the simulation results of the above three main energy loss mechanisms at  $f_{\text{EX}} = 110$  kHz. In this paper, we choose  $t_{\text{flip}}$  to be roughly 10% of the excitation period ( $t_{\text{EX}}$ ), corresponding to  $\sim 1 \mu\text{s}$ .

### C. Phase Generate-and-Combine Circuit

Fig. 13(a) shows the phase generate-and-combine circuit that issues the control vector to the switch drivers, with the corresponding timing diagram provided in Fig. 13(b). The required phases are a group of non-overlapping successive pulses, with the beginning of  $t_{\text{flip}}$  indicated by  $V_{p(1,2)}$  transitions. Referring to Fig. 13(a),  $C_{(0,1)}$  controls the 2-bit pulse generator ( $PG$ ) as well as the 2-bit delay generator ( $\tau_d$ ) to

manipulate the pulsewidth and delay of the control vector to ensure complete charge transfer with non-overlapping pulse generation while minimizing  $t_{\text{flip}}$ . Furthermore, the positive and negative transitions of  $I_p$ , indicated by  $V_{p(1)}$  and  $V_{p(2)}$ , should be processed separately.  $V_{p(1)}$  ( $V_{p(2)}$ ) is delayed using six  $\tau_d$  blocks to generate  $D_{1,-3}$  to  $D_{1,3}$  ( $D_{2,-3}$  to  $D_{2,3}$ ), which are connected to seven  $PG$  blocks to determine a series of pulses  $P_{1,-3}$  to  $P_{1,3}$  ( $P_{2,-3}$  to  $P_{2,3}$ ). These 14 control signals are systematically processed to obtain the control vector  $\Phi_{(-3:3)}$ , and are phase combined to obtain  $V_{L(0:11)}$ . As discussed in Section III-A, redundant switching activities exist during the seven-phase reconfiguration cycles. As an example,  $S_{11}$  in Fig. 9 should be turned on during  $\Phi_{-3}$ ,  $\Phi_{-2}$ , and  $\Phi_{-1}$ , as shown in Table I. In this paper, multi-phase pulses are generated by combining multiple controls using the phase combining circuit to reduce redundant switching activities through simple digital logics, as presented in Fig. 13(a). The pulses for  $\Phi_{-3}$ ,  $\Phi_{-2}$ , and  $\Phi_{-1}$  are combined to  $V_{L-3,-2,-1}$  in Fig. 13(b). The proposed phase combining circuit can effectively reduce the total number of pulses from 41 to 24, corresponding to a gate driving activity reduction of 41.5%.

### D. System-Level Simulations

Fig. 14(a) provides the simulated PEH voltage during system startup and in the steady state. The system initially operates with FCR turned off and is equivalent to an FBR implementation. After FCR turns on at  $300 \mu\text{s}$ , the PEH output swing increases from 2.8 to 7 V due to the charge accumulation process. Fig. 14(b) illustrates the zoomed-in-view of the same simulation from  $580$  to  $600 \mu\text{s}$ , highlighting the PEH voltage difference with and without phase alignment. It can be observed that the loss due to phase misalignment ( $\sim 1 \mu\text{s}$  in simulation) as a result of the comparator and logic delay can be significant, and a PEH voltage improvement from 6 to 7 V is achieved for the proposed FCR3 with phase alignment enabled. Based on simulations, the maximum output power of FBR and the proposed FCR3 are  $7.53$  and  $37.2 \mu\text{W}$ , respectively. This corresponds to a MOPIR of  $4.94\times$ , which is lower than the theoretical value of  $6.85\times$ . This difference is mainly due to the finite  $t_{\text{flip}}$ , as well as the losses due to the control overhead (i.e., phase generate-and-combine circuit and active rectifier), gate switching (i.e., switch drivers), and parasitic capacitances.

## IV. MEASUREMENT RESULTS

In this paper, we use the PEH PSI-5A4E (Piezo Systems, Inc.) that is made of the widely used piezoelectric material lead zirconate titanate. Biomedical implants usually have size constrained to  $<10 \text{ mm}^3$  with limited power budget. Consequently, we choose a PEH size of  $1 \times 1 \times 5 \text{ mm}^3$ . We use the  $d_{33}$ -mode due to its higher piezoelectric strain ( $d_{33}$ ), voltage ( $g_{33}$ ), and coupling ( $k_{33}$ ) coefficients. The PEH is characterized by the precision impedance analyzer (Agilent 4294A) through independently accessing the PEH electrodes. The extracted  $L_M$ ,  $C_M$ ,  $R_M$ , and  $C_p$  (Fig. 1) at an excitation frequency of 110 kHz are 60 mH, 5.24 pF, 1.29 MΩ, and 78.4 pF, respectively.

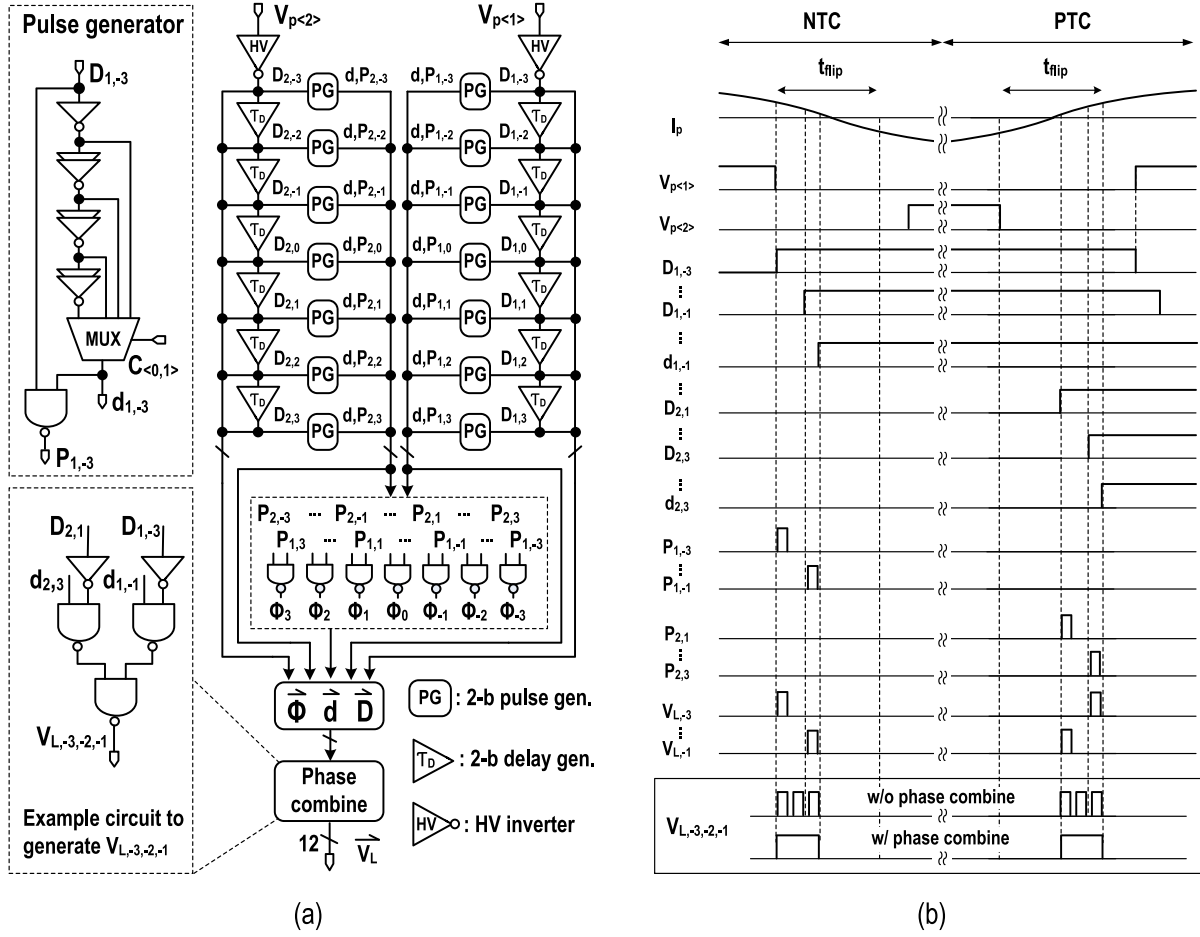


Fig. 13. (a) Implementation. (b) Timing diagram of the phase generate-and-combine circuit.

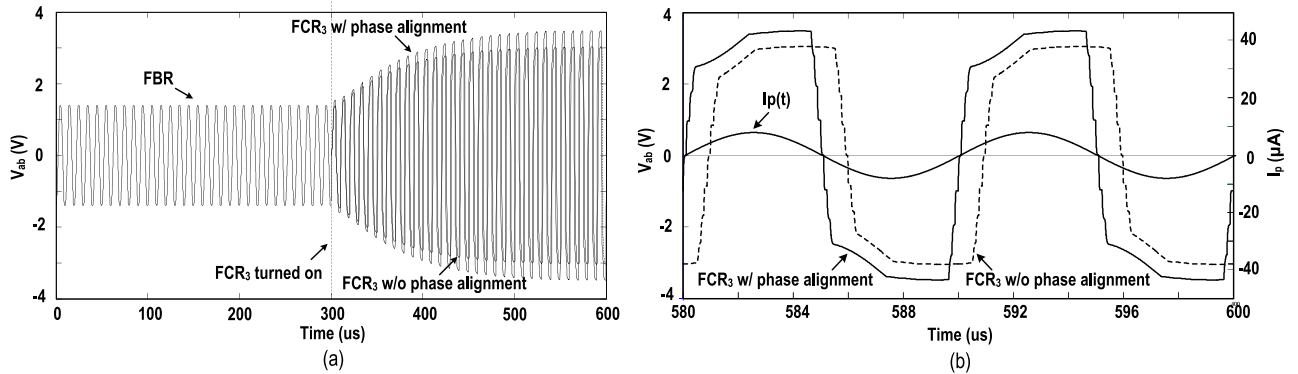


Fig. 14. Simulated PEH voltage with/without phase alignment. (a) During startup and steady state. (b) Zoomed-in-view during the steady.

Fig. 15 outlines the system measurement setup. The sinusoidal wave generated by the signal generator (Agilent 33220A) is amplified by the power amplifier (ENI240L). The PSI-5A4E serves as both the transmitter ( $76.4 \times 76.4 \times 5 \text{ mm}^3$ ) and the receiver ( $1 \times 1 \times 5 \text{ mm}^3$ ). Impedance matching between the power amplifier and the transmitter is achieved by the matching network. We selected oil as the transmission medium due to its high electrical impedance. We first demonstrate the feasibility of the proposed FCR technique by presenting the measurement results of FCR<sub>1</sub> implemented using discrete

components, followed by a fully integrated FCR<sub>3</sub> chip prototype fabricated using a  $0.18\text{-}\mu\text{m}$  1.8/3.3/6 V CMOS process, as discussed in Section III. In both measurements, the excitation signal from the power amplifier is set to 110 kHz with amplitude of 20 V unless otherwise stated.

#### A. Measurement Results for FCR<sub>1</sub> (Discrete Component)

In this measurement, the FCR<sub>1</sub> from Fig. 3(a) is implemented using three discrete capacitors, five transistor switches (NXP BSS83 N MOSFET), and an active rectifier. The signal



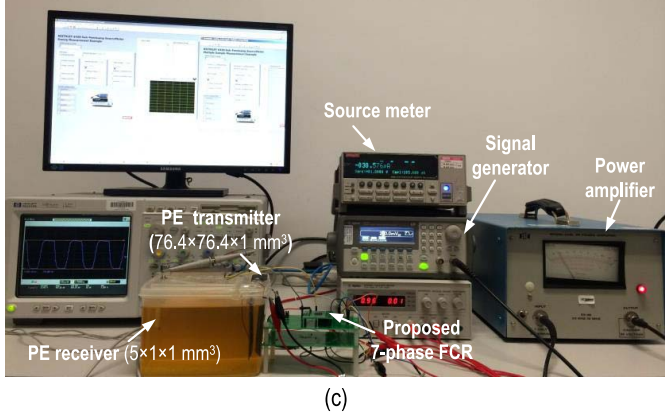
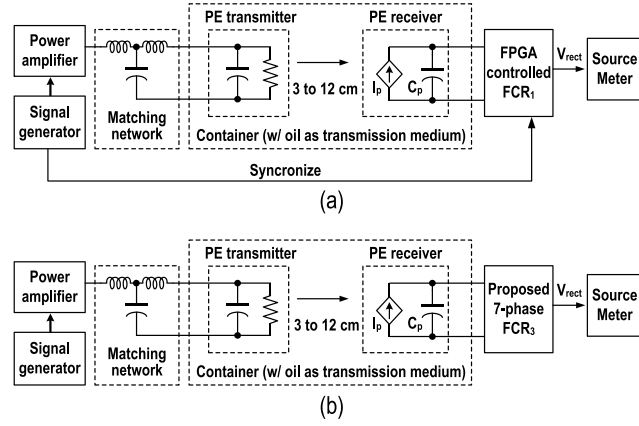


Fig. 15. Block diagram for the measurement of (a) FCR<sub>1</sub> with discrete component; and (b) FCR<sub>3</sub> with the chip prototype. (c) Photograph showing the measurement setup of FCR<sub>3</sub>.

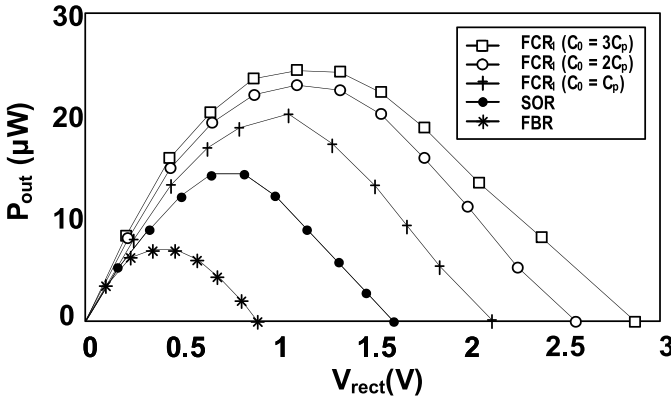


Fig. 16. Measured FCR<sub>1</sub> output power versus different  $V_{rect}$ .

generator controls both the FPGA (Altera DE2-115) and the power amplifier for synchronization to ensure proper phase alignment at the zero crossing of  $I_p$ . We use three discrete capacitors for varying the total flipping capacitance ( $C_{total}$ ) during the experiment. We control the transistors, which serve as the configuration switches, to ensure negligible switch conductance. Here, we utilize the same active rectifier as implemented using the 0.18- $\mu$ m 1.8/3.3/6 V CMOS process from FCR<sub>3</sub>, which exhibits a measured diode drop of <40 mV. Fig. 16 shows the measured FCR<sub>1</sub> output power with respect to  $V_{rect}$  with different  $C_{total}$ . It is demonstrated that an

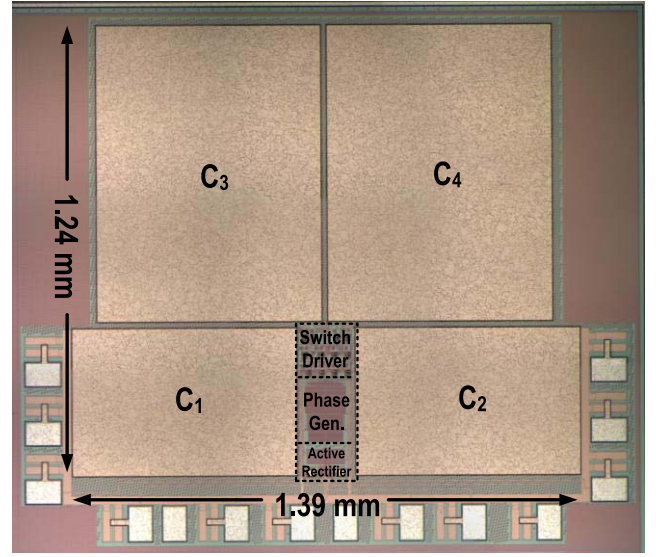


Fig. 17. Chip micrograph of the implemented FCR<sub>3</sub>.

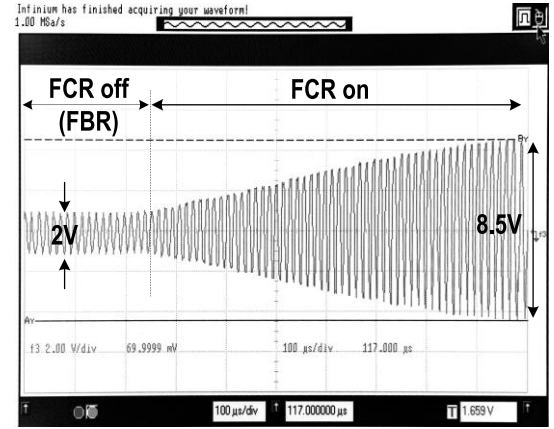


Fig. 18. Measured PEH voltage during system startup of FCR<sub>3</sub>.

increased output power is achieved when compared to FBR and SOR using the same measurement settings, and the achieved MOPIR with  $C_{total} = 80, 160$ , and  $240$  pF are  $2.9\times$ ,  $3.3\times$ , and  $3.4\times$ , respectively, without including the losses due to the control circuit and the active rectifier. The obtained results are close to the theoretical values of  $3\times$ ,  $3.33\times$ , and  $3.5\times$ .

### B. Measurement Results for FCR<sub>3</sub> (Chip Prototype)

We designed and fabricated a chip prototype based on FCR<sub>3</sub> as discussed in Section III using a standard 0.18- $\mu$ m 1.8/3.3/6 V CMOS process. The chip micrograph is shown in Fig. 17, occupying an active area of  $1.24 \times 1.39$  mm<sup>2</sup>. The flipping capacitors  $C_{1,2}$  and  $C_{3,4}$  are 240 and 480 pF, respectively, dominating the chip area (84.7%). Fig. 18 shows the PEH voltage of the proposed FCR<sub>3</sub> during system startup. It is observed that the PEH voltage increases from 2 to 8.5 V, demonstrating the effectiveness of the proposed FCR<sub>3</sub> for piezoelectric energy harvesting.

Fig. 19 compares the PEH voltage waveforms with and without phase alignment (through controlling  $V_c$ ). With phase

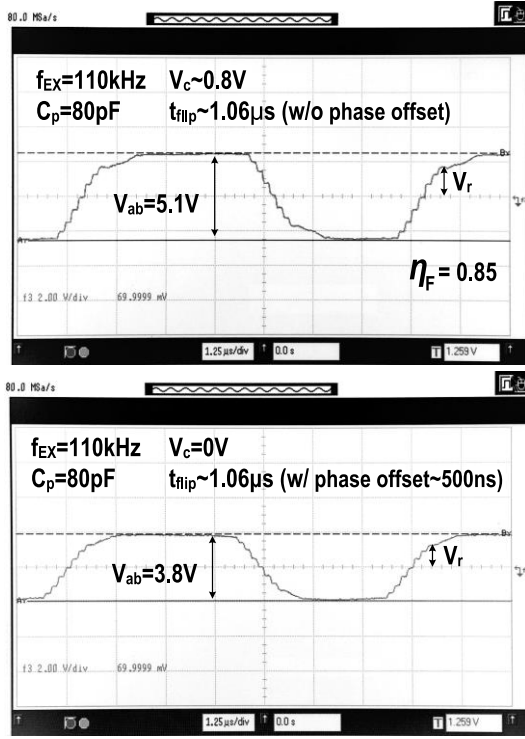


Fig. 19. Measured PEH voltage with (top) and without (bottom) phase alignment.

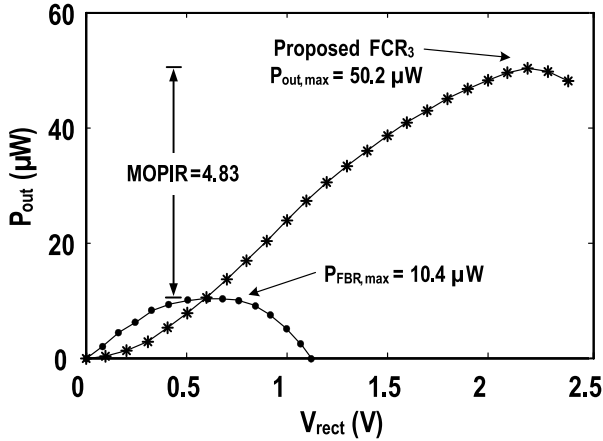


Fig. 20. Measured output power of the proposed FCR<sub>3</sub> and FBR versus  $V_{rect}$ , showing an achieved MOPIR of 4.83.

alignment, the voltage swing increases from 3.84 to 5.1 V (with a pulsewidth of 234 ns), leading to a measured  $\eta_F$  of 0.85. By controlling  $C_{(0,1)}$ , we also measured the FCR<sub>3</sub> performance with different pulse widths. The corresponding PEH voltages are 4.47, 5.03, and 4.94 V when the pulse widths are 357, 256, and 196 ns, respectively.

Fig. 20 shows the measured FCR<sub>3</sub> output power versus different  $V_{rect}$ , together with the output power achieved by FBR. The FBR achieves a maximum power output of 10.4  $\mu$ W at  $V_{rect} = 0.8$  V. With the proposed FCR<sub>3</sub>, the maximum output power increases to 50.2  $\mu$ W, leading to an MOPIR of 4.83 $\times$ . When compared with the simulated MOPIR of 4.93 $\times$  in Section III-C, the difference is mainly due to the extra loss in the

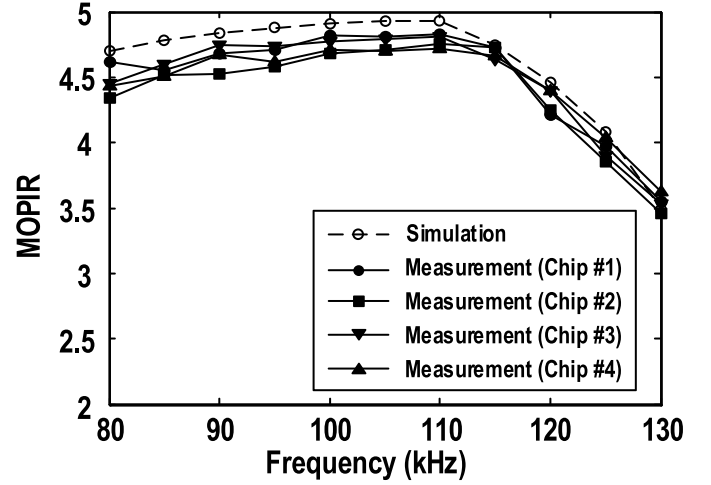


Fig. 21. Simulated and measured MOPIR versus excitation frequency from four samples.

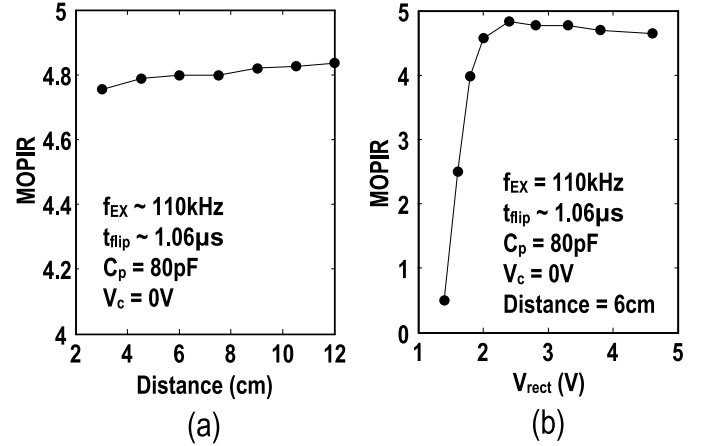


Fig. 22. (a) Measured MOPIR versus distance. (b) Measured MOPIR versus  $V_{rect}$ .

control circuitry. For  $V_{rect}$  lower than 0.6 V, the output power of FCR<sub>3</sub> is lower than that of FBR due to the performance degradation of the active rectifier at a low supply voltage.

The MOPIR versus different frequencies from four samples is shown in Fig. 21. It can be observed that the proposed FCR<sub>3</sub> achieves an MOPIR of  $>3.5\times$  from 80 to 130 kHz. The drop in the MOPIR at high frequency is mainly caused by the reduced conduction time as described in Section III-B. At low frequency, the slight drop in MOPIR is due to the increased gate switching loss as a result of increased driving voltage. Fig. 22(a) shows the measured MOPIR versus the distance between the transmitter and the receiver. Even though a reduced  $V_{rect}$  is observed during the measurement as the distance increases, the MOPIR remains roughly at 4.8 $\times$ . Fig. 22(b) shows the measured MOPIR versus different  $V_{rect}$ , and the MOPIR can be maintained with a value  $>4.5\times$  with  $V_{rect} > 2$  V.

At  $f_{EX} = 110$  kHz, the active rectifier and switch driver dissipates a power of  $\sim 8.5$  and  $\sim 6.4$   $\mu$ W while delivering an output power of 50.2  $\mu$ W, respectively. Fig. 23 summarizes the measured power breakdown. The proposed FCR<sub>3</sub> achieves a system efficiency of 71%, with 12%, 9%, and 1% consumed

TABLE II  
PERFORMANCE COMPARISON OF STATE-OF-THE-ART PEH SYSTEMS

	This work	JSSC'16 [7]	ISSCC'14 [18]	JSSC'14 [15]	JSSC'10 [10]	TCAS-I'17 [16]	JSSC'16 [17]
Technology	0.18 $\mu\text{m}$	0.35 $\mu\text{m}$	0.35 $\mu\text{m}$	0.35 $\mu\text{m}$	0.35 $\mu\text{m}$	0.25 $\mu\text{m}$ Bi	0.35 $\mu\text{m}$ HV
Energy Extraction Technique	Flipping-Capacitor Rectifier	P-SSHI	Energy Pile-Up	Energy Investment	P-SSHI	P-SSHI	P-SSHI
Piezoelectric Harvester	Piezo Systems Inc. (P5A4E @ 5mm <sup>3</sup> )	MIDE V21B & V22B	Emulated (Transformer + RC)	MIDE V22B	MIDE V22B	MIDE V22B	MIDE V20W
Key Component	On-chip MIM Capacitor ( $C_{\text{total}} = 1.44 \text{ nF}$ ) <sup>a</sup>	External Inductor (L = 3.3 mH)	External Inductor (L = 10 mH) <sup>b</sup>	External Inductor (L = 330 $\mu\text{H}$ )	External Inductor (L = 47 $\mu\text{H}$ )	External Inductor (L = 220 $\mu\text{H}$ )	External Inductor (L = 20 $\mu\text{H}$ )
Max. Output Power Increasing Rate (MOPIR)	4.83x 4.78x <sup>c</sup>	6.81x	4.22x	3.6x	2.8x	2.07x	5x <sup>e</sup>
Max. Voltage Flipping Eff. ( $\eta_F$ )	0.85	0.94	0.77 <sup>b</sup>	NA	0.75 <sup>b</sup>	0.75	0.67 <sup>b</sup>
Chip Size	1.7 mm <sup>2</sup>	0.72 mm <sup>2</sup>	5.5 mm <sup>2</sup>	2.34 mm <sup>2</sup>	4.25 mm <sup>2</sup>	0.74 mm <sup>2</sup>	0.6 mm <sup>2</sup>
Output Power	50.2 $\mu\text{W}$	160.7 $\mu\text{W}$ <sup>d</sup>	87 $\mu\text{W}$	52 $\mu\text{W}$	32.5 $\mu\text{W}$	136 $\mu\text{W}$	75 $\mu\text{W}$
Operating Freq.	110 kHz	225 Hz	100 Hz	143 Hz	225 Hz	144Hz	82Hz

<sup>a</sup> Total capacitance for  $C_{1,4}$

<sup>b</sup> Estimated from the corresponding literature

<sup>c</sup> Averaged over 4 measured samples

<sup>d</sup> Off-resonance with 3.35g acceleration

<sup>e</sup> FBR output power limited by excessive diode voltage drop

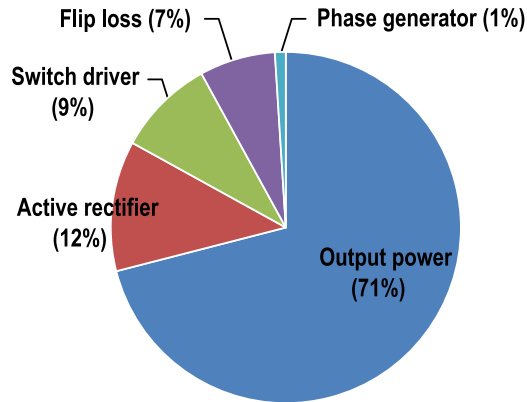


Fig. 23. Measured power breakdown of FCR3.

by the active rectifier, switch driver, and phase generate-and-combine circuit, respectively. The flip loss, which includes all the intrinsic losses due to capacitor reconfigurations during the finite  $t_{\text{flip}}$ , contributes to roughly 7%.

Table II compiles the chip performance summary and benchmark. The proposed PEH system achieves an MOPIR enhancement of  $>1.2\times$  when compared with [10], [15], [16] that requires only a relatively small external inductor (tens to hundreds of microhenry). Even though Du *et al.* [17] achieves a high MOPIR of  $5\times$  with a 20- $\mu\text{H}$  external inductor, this is mainly achieved by the excessive diode voltage drop at a low output voltage, which ultimately limits the FBR output power. Unlike [7], [18] that achieve high MOPIR by using

an excessively large external high-Q inductor in the order of millihenry, this paper reports the first PEH that exhibits a high MOPIR ( $4.83\times$ ) and high  $\eta_F$  (0.85) in a compact area with zero external components.

## V. CONCLUSION

This paper presented a fully integrated FCR for piezoelectric energy harvesting without requiring large external inductors. We derived mathematical expressions for the extractable energy using different FCR implementations, obtaining a good match between the simulation and measured results. The low-cost, ultra-compact, single chip solution with a measured MOPIR of  $4.83\times$  reveals the proposed FCR as a promising solution for piezoelectric energy harvesting applications, especially for deep-tissue implant implementations.

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**Man-Kay Law** (M'11–SM'16) received the B.Sc. degree in computer engineering and the Ph.D. degree in electronic and computer engineering from The Hong Kong University of Science and Technology (HKUST), in 2006 and 2011, respectively.

Since 2011, he has been with HKUST as a Visiting Assistant Professor. He is currently an Associate Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China. He has authored or co-authored over 70 technical journals and conference papers. He

holds 5 U.S. patents. His research interests include the development of ultra-low power sensing circuits and integrated energy harvesting techniques for wireless and biomedical applications.

Dr. Law is/has been a member of the Technical Program Committee of Asia Symposium on Quality Electronic Design from 2012 to 2013, the Review Committee Member of the IEEE International Symposium on Circuits and Systems from 2012 to 2017, the Biomedical Circuits and Systems Conference from 2012 to 2017, the International Symposium on Integrated Circuits in 2014, and the University Design Contest Co-Chair of Asia and South Pacific Design Automation Conference in 2016. He serves as a Technical Committee Member in both the IEEE CAS committee on Sensory Systems as well as Biomedical Circuits and Systems. He is also an ITPC Member of the IEEE International Solid-State Circuits Conference. He was a co-recipient of the Asia Symposium on Quality Electronic Design Best Paper Award in 2013, the A-SSCC Distinguished Design Award in 2015, the Asia and South Pacific Design Automation Conference Best Design Award in 2016, and the Macao Science and Technology Invention Award (second class) by Macau Government–FDCT in 2014.



**Pui-In Mak** (S'00–M'08–SM'11) received the Ph.D. degree from the University of Macau (UM), Macao, China, in 2006.

He is currently a Full Professor with the UM Faculty of Science and Technology–ECE, and the Associate Director (Research) with the UM State Key Laboratory of Analog and Mixed-Signal VLSI. His research interests include analog and radio-frequency (RF) circuits and systems for wireless and multidisciplinary innovations.

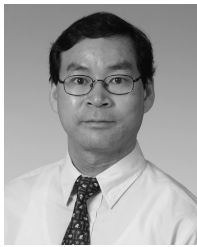
Dr. Mak involvements with IEEE are the Editorial Board Member of the IEEE Press from 2014 to 2016, a member of Board-of-Governors of the IEEE Circuits and Systems Society from 2009 to 2011, a Senior Editor of the IEEE Journal on Emerging and Selected Topics in Circuits and Systems from 2014 to 2015, a Guest Editor of the IEEE RFIC VIRTUAL JOURNAL in 2014 and the IEEE JOURNAL OF SOLID-STATE CIRCUITS in 2018, an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I from 2010 to 2011, from 2014 to 2015, and II from 2010 to 2013. He was a co-recipient of the DAC/ISSCC Student Paper Award'05, the CASS Outstanding Young Author Award'10, the National Scientific and Technological Progress Award'11, the Best Associate Editor of IEEE Transactions on Circuits and Systems II 2012–2013, the A-SSCC Distinguished Design Award'15, and the ISSCC Silkroad Award'16. He is/was the TPC Vice Co-Chair of ASP-DAC in 2016, a TPC Member of A-SSCC from 2013 to 2016, and ESSCIRC and ISSCC since 16. He has been an Associate Editor of the IEEE SOLID-STATE CIRCUITS LETTERS since 2017. He is/was the Distinguished Lecturer of IEEE Circuits and Systems Society from 2014 to 2015 and the IEEE Solid-State Circuits Society from 2017 to 2018. In 2005, he was decorated with the Honorary Title of Value for scientific merits by the Macau Government.



**Zhiyuan Chen** received the B.Sc. and M.Sc. degrees from the University of Macau (UM), Macao, China, in 2011 and 2013, respectively, where he is currently pursuing the Ph.D. degree with the UM State Key Laboratory of Analog and Mixed-Signal VLSI and the Faculty of Science and Technology, ECE.

His current research interests include solar and piezoelectric energy harvesting systems.





**Wing-Hung Ki** (S'86–M'91) received the B.Sc. degree in electrical engineering from the University of California, San Diego, CA, USA, in 1984, the M.Sc. degree in electrical engineering from the California Institute of Technology, Pasadena, CA, USA, in 1985, and the Ph.D. degree in electrical engineering from the University of California, Los Angeles, CA, USA, in 1995.

In 1992, he joined the Department of Power and Battery Management, Micro Linear Corporation, San Jose, CA, USA, as a Senior Design Engineer, where he was involved in the design of power converter controllers. In 1995, he joined the Hong Kong University of Science and Technology, Hong Kong, where he is currently a Professor with the Department of Electronic and Computer Engineering. His current research interests include power management circuits and systems, switched-inductor and switched-capacitor power converters, low dropout regulators, wireless power transfer for biomedical implants, and analog IC design methodologies.

Prof. Ki served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 2004 to 2005 and from 2012 to 2013, and the IEEE TRANSACTIONS ON POWER ELECTRONICS since 2016, and was on the International Technical Program Committee of the IEEE International Solid-State Circuits Conference from 2010 to 2014.



**Rui P. Martins** (M'88–SM'99–F'08) was born in 1957. He received the bachelor's (five-years), the master's, and the Ph.D. degrees, and the Habilitation for Full-Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon, Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

He has been with the Department of Electrical and Computer Engineering, IST, TU of Lisbon, since 1980. Since 1992, he has been on leave from IST, TU of Lisbon. He is currently with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he has been a Chair-Professor since 2013. In FST, he was the Dean of the Faculty from 1994 to 1997. He has been the Vice-Rector of the University of Macau since 1997. Since 2008, after the reform of the UM Charter, he was nominated after open international recruitment, and reappointed in 2013, as the Vice-Rector (Research) until 2018. Within the scope of his teaching and research activities, he has taught 21 bachelor's and master's courses. In UM, he has supervised (or co-supervised) 40 theses, Ph.D. (19), and master's (21). He has co-authored six books and nine book chapters, 377 papers, in scientific journals (111) and in conference proceedings (266), as other 60 academic works, in a total of 470 publications. He holds 18 patents, including USA (16) & Taiwan (2). He was a co-founder of Synopsys, Macao, China, in 2001/2002, and created in 2003, the Analog and Mixed-Signal VLSI Research Laboratory, UM, in 2011 to the State Key Laboratory of China (the first in engineering in Macao), being its Founding Director.

Dr. Martins was the Founding Chairman of both IEEE Macau Section from 2003 to 2005, and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications from 2005 to 2008 [2009 World Chapter of the Year of IEEE CAS Society (CASS)]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on CAS, and the Vice-President for Region 10 (Asia, Australia, and the Pacific) of the IEEE CASS from 2009 to 2011. Since then, he was the Vice-President (World) Regional Activities and Membership of the IEEE CASS from 2012 to 2013. He was an Associate Editor of the IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS from 2010 to 2013, nominated Best Associate Editor of T-CAS II for 2012 and 2013. He was a member of the IEEE CASS Fellow Evaluation Committee in 2013 and 2014, and the CAS Society representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)—the Director of the IEEE. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference—ASPAC' 2016. He was a Nominations Committee Member in 2016. He is now the Chair of the IEEE Fellow Evaluation Committee (class of 2018), both of IEEE CASS. He was the recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In 2010, he was elected, unanimously, as the Corresponding Member of the Portuguese Academy of Sciences, Lisbon, being the only Portuguese Academician living in Asia.