Gain Error Calibrations for Two-Step ADCs: Optimizations Either in Accuracy or Chip Area

Guan Cheng Wang, Yan Zhu, *Member, IEEE*, Chi-Hang Chan, *Member, IEEE*, Seng-Pan U, *Fellow, IEEE*, and Rui P. Martins, *Fellow, IEEE*

***Abstract*— This paper presents two calibration schemes to correct the stage gain error in analog-to-digital converters. The two approaches target different scenarios, either better calibration accuracy or less digital overhead. First, we optimize the gain calculation scheme in the conventional code statistics-based approach, which improves the calibration accuracy. Moreover, we introduce a missing-code-detected calibration that replaces the calculation of the gain coefficient by counting and multiplying the number of missing codes in the digital domain, which significantly simplifies the digital implementation. To eliminate the calibration dependence on the input signal, we implement a testing signal generation on-chip. We also compare these calibration schemes with the requirements of the input signal, the calibration accuracy, as well as the hardware overhead based on a mathematical model with behavior simulations. Both concepts were verified in an 11-bit 80-MS/s successive approximation register with a bridge digital-to-analog converter fabricated in a 65-nm CMOS.**

***Index Terms*— Bridge digital-to-analog converter (DAC), gain error calibration, successive approximation register (SAR) analog-to-digital converters (ADCs), testing signal generation (TSG).**

I. Introduction

SUCCESSIVE approximation register analog-to-digital converters (SAR ADCs) [1]–[3] rely on the capacitive digital-to-analog converter (DAC) array to perform binary-searched feedback. By employing the binary-weighted DAC with increased resolution (>12 bit), it imposes that the capacitor matching rather than noise will dominate the performance, as the noise-optimized design dictates that the unit capacitance is too small to fulfill the required matching. The bridge DAC [1], [4] is one of the prevalent structures that can circumvent this problem. By inserting an attenuation capacitor C_a between the most significant bit (MSB)- and the least significant bit (LSB)-array, the total capacitive units of the DAC can be significantly reduced. The bridge DAC has less total unit capacitors when compared with the binary-weighted DAC under the same sampling capacitance for the kT/C noise, e.g., we design a total capacitance of 1.2 pF is designed according to 12-b kT/C noise under a 1.2 V_{p-p} full scale. By using the advanced switching approaches [5], [6], we only need an 11-bit DAC to quantize 12 bit. A binary-weighted structure has a total number of 2048 units, while the bridge DAC obtains a minimum of 97 units by implementing a 6 and 5 bit in the MSB- and the LSB-array, respectively. Therefore, the unit capacitance for bridge DAC can be designed 32× larger than its counterpart, leading to better unit element matching. However, the required matching in the binary DAC and the bridge DAC is 0.55% and 0.1%, respectively, canceling out the $\sqrt{32}\times$ unit element matching benefit of the bridge DAC due to its more stringent matching requirement. Thus, the purpose of using the bridge DAC is that it can simplify the implementation and reduce the interconnection, thus leading to lower parasitics for high-speed implementation. However, the key design limitation of the bridge DAC is that the mismatch of C_a and the inner node parasitics introduce a gain error between the reference voltages in the MSB- and the LSB-array. The error pattern exhibited by the ADC's output characteristic is identical to the stage gain error in a two-stage ADC. Previous research has investigated such problems and tried to overcome them either in the analog [7]–[9] or in the digital domain [10]–[16]. The analog-based calibrations compensate for the error by utilizing an additional capacitive DAC, where the error measurement is sensitive to the comparator offset and noise. Suppressing them to a lower level usually causes increased analog circuit complexity. Motivated by the benefits of technology scaling, the digitally assisted solutions exhibit much better power efficiency in high-speed implementations. The correlation-based [11], [12], [15] and the code statistics-based [13], [14], [16] schemes estimate and compensate

Manuscript received April 2, 2018; revised June 29, 2018; accepted August 6, 2018. Date of publication September 18, 2018; date of current version October 23, 2018. This work was supported in part by NSFC under Grant 61604180, in part by Macao Science and Technology Development Fund under Grant 117/2016/A3, and in part by the Research Grants of University of Macau under Grant MYRG2018-00113-AMSV. *(Corresponding author: Yan Zhu.)*

G. C. Wang, Y. Zhu, and C.-H. Chan are with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau 999078, China (e-mail: yanzhu@umac.mo).

S.-P. U is with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau 999078, China, also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macau 999078, China, and also with Synopsys Macau Ltd., Macau 999078, China.

R. P. Martins is with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau 999078, China, and also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macau 999078, China, on leave from the Instituto Superior Técnico, Universidade de Lisboa, 1649004 Lisboa, Portugal.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TVLSI.2018.2865595

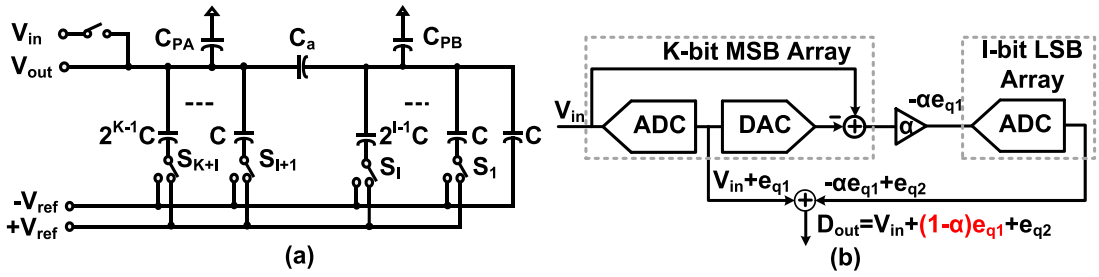


Fig. 1. (a) N-bit bridge structure DAC containing K-bit MSB- and I-bit LSB-array ($K + I = N$). (b) Nonlinearity introduced by the bridge DAC can be modeled as a stage gain error in a two-stage ADC.

the nonlinearity in the digital domain, requiring less modification of the analog circuitry, while the error estimation based on a large amount of data increase the converging time.

This paper reports two calibration schemes for gain error correction, which are applicable in either SAR ADCs using a bridge DAC or other two-stage architectures. The two schemes aim for different design targets. The algorithm of the code statistics-based [10], [13] scheme is optimized to suppress the differential-nonlinearity (DNL) error to within ±0.5 LSBs. While the missing-code-detected (MCD) scheme [14] transforms the gain error calculation derived from the code statistics measurement to a simple missing-code count, which requires the data recording only from two adjacent samples, and thus significantly reducing the digital overhead. The design tradeoffs of the two schemes are discussed in detail with behavior simulations and measurement verifications in an 11-bit, 80-MS/s SAR ADC. The two schemes demonstrate their corresponding advantages in different aspects. Moreover, to remove the dependence on the input signal, we present a testing signal generator (TSG) and analyze its design considerations. The measurement results show that the signal-to-noise ratio (SNR) can be improved by ∼6 dB from 57.3 to 63 dB.

This paper is organized as follows. Section II introduces the error characteristics of a SAR ADC using the bridge DAC. It reports the accuracy limitation in the conventional code density-based scheme [10], [13] and its optimized version in Section III. Section IV presents the proposed MCD calibration [14] and its comparison with the code density-based schemes. Section V includes the circuit implementation of the TSG and its accuracy considerations under process variation and device mismatch. Finally, Section VI exhibits the measurement results and Section VII presents the conclusion.

II. Gain Error in SAR ADC Using Bridge DAC

When a bridge DAC [Fig. 1(a)] structure is used in a SAR ADC, the conversion can be modeled as a two-stage operation with a unity stage gain, where the MSB- and the LSB-array resolve the fine K- and I-bit, respectively. In this analysis, we ignore the overall gain error caused by the parasitics C_{PA} and C_{PB}. The output voltage V_{out} from the DAC can be simplified as [14]

$$V_{out} \approx \frac{1}{\delta}\left(\underbrace{\frac{2^I C + C_{\mathrm{PB}} + C_a}{C_a}\sum_{j=1}^{K} 2^{j-1} C S_{i+j}}_{\text{MSB Array}} + \underbrace{\sum_{j=1}^{I} 2^{j-1} C S_j}_{\text{LSB Array}}\right) \cdot V_{\mathrm{ref}} \tag{1}$$

$$\delta = (2^I + 2^K - 1)C + 2^{I+K} C^2 / C_a \tag{2}$$

where C and C_a are the unit and the attenuation capacitors, respectively, and S_j equal to 1 or 0 represents the digital input. From (1), it can be found that the parasitic C_{PB} and the mismatch of C_a cause a gain error between two stages, i.e., the MSB- and the LSB-array. Therefore, in Fig. 1(b), the final digital output contains a residue error $(1-\alpha)e_{q1}$) originated by the gain error between two stages, where α is the actual gain. If C_{PB} is represented as a γ percentage of the total capacitance in the LSB-array ($C_{\mathrm{PB}} = \gamma 2^I C$), we can obtain the relationship between the coefficient of the MSB-array in (1) and α as

$$\frac{(1+\gamma)2^I C + C_a}{C_a} = \alpha \frac{2^I C + C_{a,\mathrm{id}}}{C_{a,\mathrm{id}}} \tag{3}$$

where $C_{a,\mathrm{id}}$ is the ideal value of the attenuation capacitor. Thus, α can be derived as

$$\alpha = 1 + \frac{(1+\gamma)2^I C \cdot C_{a,\mathrm{id}} - 2^I C \cdot C_a}{2^I C \cdot C_a + C_a \cdot C_{a,\mathrm{id}}}. \tag{4}$$

Fig. 2(a) shows the residues after a K-bit quantizer in the first stage supposing that we apply a uniformly distributed input to an N-bit ADC using the bridge DAC. If the numerator of (4) is larger than 0, implying $C_a < (1+\gamma)\, C_{a,\mathrm{id}}$ and accordingly $\alpha > 1$, the residue from the first stage (αe_{q1}) saturates the second-stage full scale ($V_{\mathrm{FS},2}$). The outputs near the decision boundaries of the first stage are repeated creating peaks in Fig. 2(b1). Since K-bits are determined in the first stage, it results in 2^K intervals and the width of each segment is 2^I codes. The pattern is systematic; thereby, the following

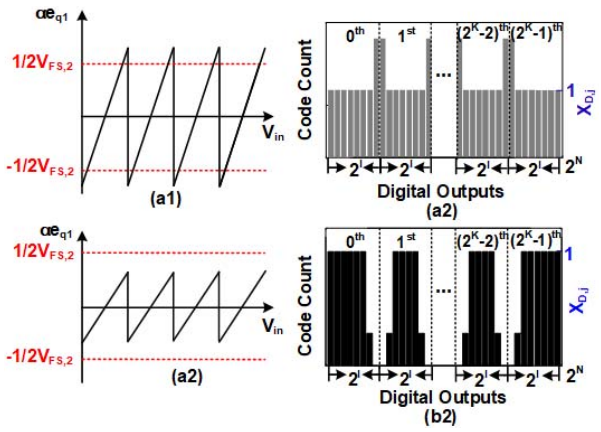


Fig. 2. (a1) Residue after K-bit quantizer in MSB-array with $\alpha > 1$ and (a2) with $\alpha < 1$. (b1) Output code histogram and corresponding code density with $\alpha > 1$ and (b2) with $\alpha < 1$.

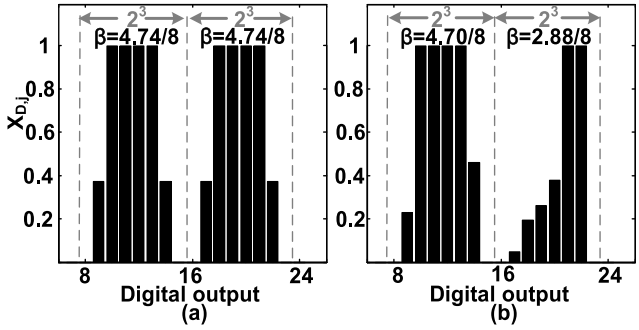


Fig. 3. (a) Code density plot of a 5-bit ADC with ramp input signal. (b) With nonuniformly distributed input.

discussion is based on one segment. We define the density of the jth code ($X_{D,j}$) to be the ratio of its code count (X_j) and the average count $\bar{X}j$ that can be expressed as

$$X_{D,j} = \frac{X_j}{\overline{X_j}} \tag{5}$$

$$\overline{X_j} = \frac{1}{2^I}\sum_{j=1}^{2^I} X_j. \tag{6}$$

Obviously, all uniformly distributed outputs have their density equal to 1. As mentioned before, there are 2^I codes in one statistic segment; thus; theoretically the sum of the code density $\sum_{j=1}^{2^I} X_{D,j}$ is 2^I. In the case of $\alpha > 1$, large peaks occur at the boundaries of the segment, whose pattern is even symmetrical.

If C_a is adjusted to a value larger than $(1+\gamma)C_{a,\mathrm{id}}$, leading to $\alpha < 1$, the residue from the first stage [Fig. 2(a2)] is much smaller than the $V_{\mathrm{FS},2}$ resulting in the gaps at the boundaries of each segment shown in Fig. 2(b2). The peaks cannot be removed in the digital domain, as the accumulated codes cannot be separated [10]. Only the error outputs containing lower code density can be fixed; thereby, C_a is initially designed to be larger than its ideal value to ensure $\alpha < 1$.

III. Histogram-Based Ratio Mismatch Calibration

A. Calibration According to Code Density

Histogram-based ratio mismatch (HBRM) calibration [10], [13] can obtain high accuracy and a large calibration range. According to [5], the gain error can be corrected as

$$D_{\mathrm{cal,out}} = \mathrm{round}\left(\beta * \sum_{j=1}^{K} 2^I \cdot 2^{j-1} B_{j+I} + \sum_{j=1}^{I} 2^{j-1} B_j\right) \tag{7}$$

where B_j is the ADC output and β is the gain coefficient. The first term $\sum_{j=1}^{K} 2^I \times 2^{j-1} B_{j+I}$ is the output from the MSB-array. For intuitive understanding, it defines the code width of each segment (ideal width is 2^I codes) and the total number of segments (2^K segments in this case) as shown in Fig. 2(b2). If there is a gain error, the actual code width is smaller, generating the gaps among each segment. The gain coefficient β applied to the first term $\sum_{j=1}^{K} 2^I \times 2^{j-1} B_{j+I}$ adjusts the code width to fix the gaps. The gain coefficient β can be calculated as

$$\beta = \frac{\sum_{j=1}^{2^I} X_{D,j}}{2^I} \tag{8}$$

where the numerator is the measured code width of one segment calculated by the cumulative sum of the code density. In practice, the gain estimation based on code density requires a large computational effort, so the calculation of $X_{D,j}$ can be simplified to

$$\begin{cases} \text{if}, & X_{D,j} \geq 0.5 \rightarrow X_{D,j} = 1 \\ \text{otherwise}, & X_{D,j} = X_{D,j} \end{cases} \tag{9}$$

where we add a decision threshold of 0.5. If $X_{D,j}$ is not smaller than 0.5 implying the output has no error, we set its code density to 1. Otherwise, it is determined as an error code, whose density of $0 \leq X_{D,j} < 0.5$ will be accumulated to the numerator of (8).

The HBRM calibration has the input constraint. The accuracy of the code density-based calibration depends highly on the type of the input signal, and it may fail if the input signal is nonuniformly distributed. The behavior simulations are performed in a 5-bit SAR ADC with a (2+2) bridge DAC and the ADC is otherwise ideal. C_a is enlarged 2.35× and γ is set to 0; thereby, the gain factor α calculated according to (4) should be equal to 0.57. The output characteristic is expected to have 2^2 periodic segments and each one should contain 2^3 codes. In Fig. 3(a), the gain factor estimated according to (8) and (9) is 0.59, where the deviation from the theoretical value is due to the limited accuracy of the HBRM scheme. However, in Fig. 3(b), β calculated from different segments is quite different suggesting that the calibration accuracy depends highly on the type of input signal.

B. Proposed Optimized Code-Density Estimation

The error can be fixed by applying the estimated gain coefficient as discussed earlier, and by combining (7) and (8),

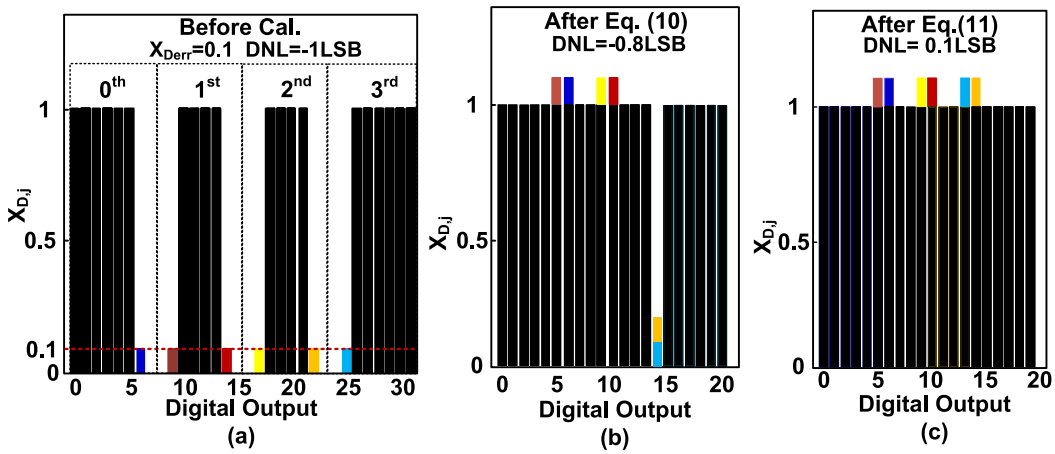


Fig. 4. (a) Code density of 5-bit ADC output before HBRM calibration. (b) After conventional HBRM calibration. (c) After OHBRM calibration.

we can obtain

$$D_{\text{cal,out}} = \text{round}\left(\sum_{j=1}^{2^I} X_{D,j} \cdot \sum_{j=1}^{K} 2^{j-1} B_{j+I} + \sum_{j=1}^{I} 2^{j-1} B_j\right) \tag{10}$$

where the original segment width 2^I in (7) is modified to $\sum_{j=1}^{2^I} X_{D,j}$ representing the measured code width. Rounding the overall output is not accurate enough, as illustrated in the case in Fig. 4, the missing codes can be removed after HBRM calibration while the DNL is still large. This occurs because the round operation leads to a nonuniform adjustment of segment width, e.g., we adjust the width of the first and second segment to four while the third is five. In addition, the errors are code dependent which need to be quantified in many cases. This can be avoided by performing the round operation to $\sum_{j=1}^{2^I} X_{D,j}$ rather than the overall output, which can be expressed as

$$D_{\text{cal,out\_opt}} = \text{round}\left(\sum_{j=1}^{2^I} X_{D,j}\right) \cdot \sum_{j=1}^{K} 2^{j-1} B_{j+I} + \sum_{j=1}^{I} 2^{j-1} B_j. \tag{11}$$

As $X_{D,\text{err}}$ is a decimal number, the accuracy rounding off the measured code width depends only on $X_{D,\text{err}}$, which affects the segment width after calibration. If we process the raw outputs according to (11), it can guarantee the DNL $<\pm 0.5$ LSB. Since now the adjustment of segment width becomes uniform, the DNL after calibration can be quantified by four cases illustrated in Table I. As mentioned before, each segment contains two identical error codes, which will be summed together through the calculation in (11). Therefore, the actual rounding is performed in $2X_{D,\text{err}}$. The width adjustment varies under different values of $X_{D,\text{err}}$, resulting in different DNL patterns in Table I, which are all suppressed within ± 0.5 LSBs. Fig. 4(c) shows the calibrated output of the previous 5-bit ADC by using the optimized HBRM (OHBRM) approach, which corresponds to the $X_{D,\text{err}}$ range of (0, 0.25)

TABLE I

OUTPUT CODE HISTOGRAM AFTER ROUND OPERATION UNDER A DIFFERENT $X_{D,\text{err}}$

$X_{D,\text{err}}$	Rnd($2X_{D,\text{err}}$)	Code density Histogram After Cal.
(0,0.25)	0	
[0.25,0.5)	1	
[0.5,0.75)	2	
[0.75,1)	2	

in Table I. It can be concluded that the OHBRM scheme can obtain better accuracy; the tradeoff it imposes is that the code statistics and processing require large memory and computational effort. If it is implemented on chip, its digital overhead would be significant. To simplify the algorithm and the implementation on chip, we propose an MCD scheme in Section IV.

IV. MISSING-CODE-DETECTED GAIN ERROR CALIBRATION

A. Missing-Code Detected Algorithm

The proposed MCD calibration [14] estimates β by counting the number of missing codes instead of code statistics, which can significantly simplify the implementation of the calibration circuitry. In the MCD scheme, the defined

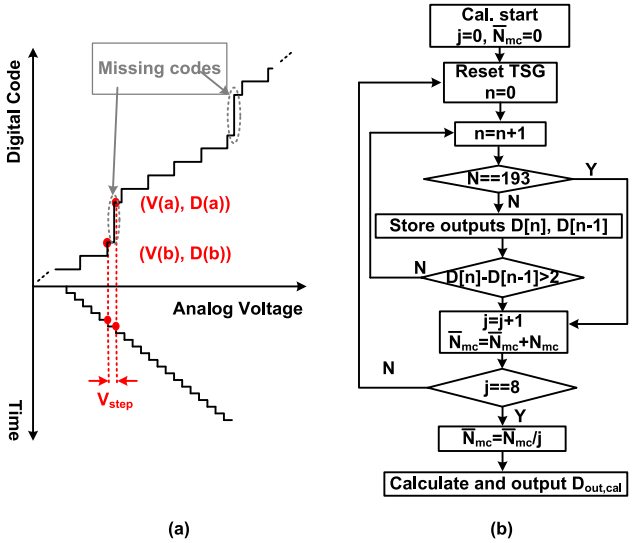


Fig. 5. (a) Transfer characteristic of the ADC containing the transition errors caused by the bridge DAC. (b) Flowchart of MCD calibration.

$X_{D,j}$ becomes

$$\begin{cases} \text{if} & X_{D,j} > 0 \rightarrow X_{D,j} = 1 \\ \text{otherwise,} & X_{D,j} = 0 \end{cases} \tag{12}$$

where the code density larger than 0 will be counted as 1. This is the key difference between the MCD calibration and the code density-based calibration, where the $X_{D,j}$ less than 0.5 will be enlarged to 1 in the MCD scheme. By sacrificing some of the calibration accuracies, (8) can be simplified to

$$\beta = \frac{2^I - N_{\text{mc}}}{2^I} \tag{13}$$

where N_{mc} is the number of inherent missing codes in one segment (2^I codes). The missing code can be easily detected in the digital domain. Fig. 5(a) shows that the ADC's output transfer characteristic has the large step which occurs at the boundaries of each segment and can be easily sensed in the digital domain by applying a slow ramp or staircase input signal. In this design, we generate a staircase testing-signal on chip for error detection whose resolution needs to be higher than the ADC itself. Since the testing signal is only required to cover a small range of 2^I codes (~18.75 mV in this design), its implementation draws less design difficulty. Fig. 5(b) illustrates the flowchart of the calibration. To guarantee the calibration range covering 2^I codes, the input is swept by 192 steps. The register saves the output of two adjacent samples $D_{\text{out}}[n-1]$ and $D_{\text{out}}[n]$, whose difference implies the number of missing codes when their difference is larger than 2. Fig. 5(a) displays the missing codes that occur periodically, implying detection in only one segment. Considering the missing codes may occur due to the noise, the detection threshold is set to 2. To further improve the calibration accuracy, we use the average value of $\bar{N}_{\text{mc}}$ by repeating the above-mentioned operation $n\times$ (in this design, $n = 8$). We combine (7) and (13) to obtain the final

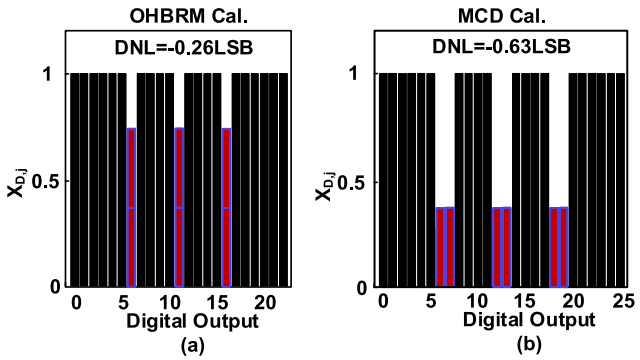


Fig. 6. (a) Code histogram after OHBRM calibration with a uniform input signal. (b) After MCD calibration.

expression as

$$D_{\text{cal,out}} = \sum_{j=1}^{2^{I+K}} 2^{j-1} B_j + \text{round}(\bar{N}_{\text{mc}}) \sum_{j=1}^{K} 2^{j-1} B_j. \tag{14}$$

It is worth noting that (14) does not contain the β term implying the omission of β calculation. The MCD scheme simplifies the algorithm requiring only a multiply function between the $\bar{N}_{\text{mc}}$ and the output codes from the MSB-array.

B. Algorithm Comparisons

From the input constraint point of view, the MCD scheme is more relaxed than the code density-based approaches. The MCD calibration only requires the input to be continuous in certain error detection range (2^I codes) rather than being uniformly distributed. To verify this, we use the MCD scheme to process the 5-bit ADC outputs of Fig. 3(b) where the estimated value of β is 0.75 and the corresponding signal-to-noise-distortion ratio (SNDR) after calibration can be improved by ~4 dB from 20.6 to 24.9 dB. However, the OHBRM fails to estimate the gain coefficient under the same input signal, resulting in an SNDR of 20.1 dB. Thus, the MCD scheme relaxes the input constraint of the input signal. The code histogram with the outputs in Fig. 3(a) after OHBRM and MCD calibrations as shown in Fig. 6(a) and (b), respectively. Both schemes remove the missing codes, while as expected due to limited accuracy the outputs from MCD calibration contain |DNL| > 0.5 LSBs. This is because the error code density $X_{D,\text{err}} < 0.5$ is set to 1 in (12), but it still guarantees a |DNL| error less than 1 LSB. To verify the effectiveness of the calibrations, we performed behavioral simulations modeling the conversion nonlinearities in a 12-bit SAR ADC built with a $(7b + 4b)$ bridge DAC. The values of the unit capacitors are Gaussian random variables with a standard deviation of σ ($\Delta C/C = 0.1\%$). As discussed in Section III-B, the final calibration accuracy depends on how the inherent error $X_{D,\text{err}}$ is processed. We compare the accuracy of three schemes through sweeping the value of $X_{D,\text{err}}$. C_a is set as 20/16 C (25% larger than the ideal value) generating a gap width of four missing codes. By varying γ from 0% to 7%, it can correspondingly adjust the $X_{D,\text{err}}$ from 0.1 to 0.9. Fig. 7(a) shows the average SNDR versus $X_{D,\text{err}}$ from 100 Monte Carlo (MC) simulations. The OHBRM

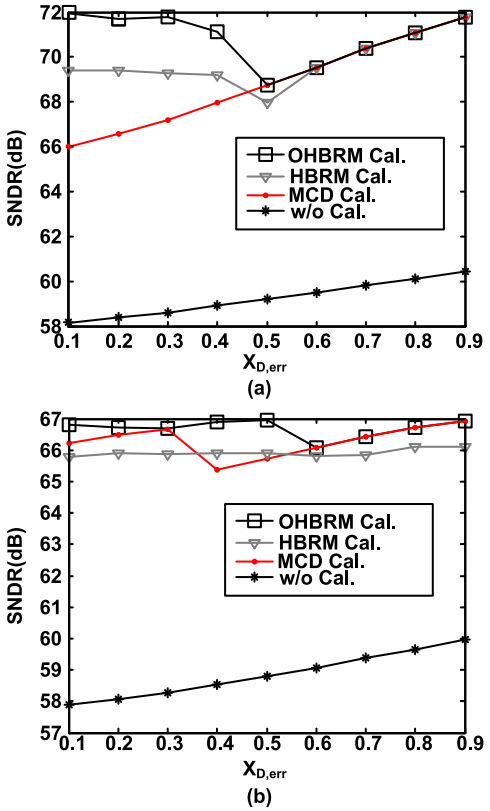


Fig. 7. (a) SNDR versus $X_{D,\text{err}}$ before and after calibrations under three calibration schemes without noise and (b) with noise.

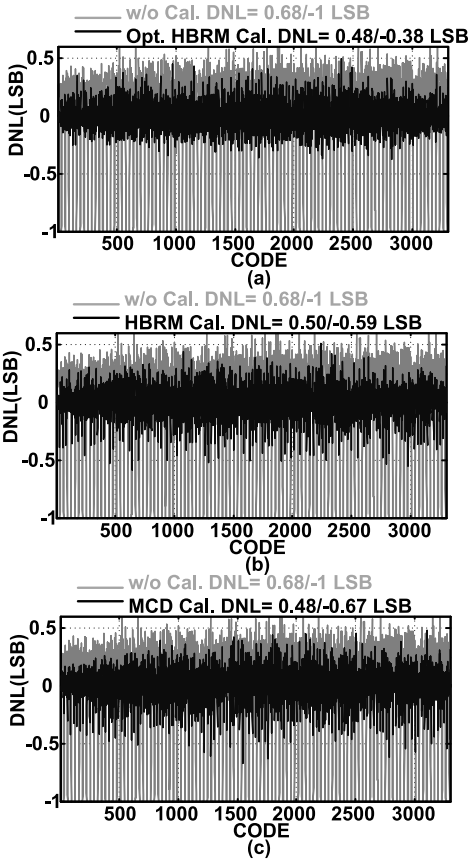


Fig. 8. (a) DNL before and after opt. HBRM calibration. (b) After HBRM calibration. (c) After MCD calibration.

calibration is expected to achieve the best accuracy when the $X_{D,\text{err}}$ is smaller than 0.5, because, according to (9), the error code threshold is set at 0.5, and when $X_{D,\text{err}} \geq 0.5$ the calculation of the gain factor in (8) and (13) will result in the same value. In practice, if the SNDR is dominated by other circuit nonidealities, e.g., noise from kT/C, comparator, clock jitter, and reference error due to switching transient, the three schemes will have the similar results. To model the cases, we include the comparator noise in the simulations of Fig. 7(b). The σ standard deviation of the comparator noise voltage is set as $\Delta/2$ (Δ is the LSB of the ADC). Since the noise dominates the SNDR after calibration, three approaches show less than 1 dB difference from the SNDR, but the finite calibration accuracy can be demonstrated in the DNL plot. Fig. 8 depicts the corresponding DNL at $X_{D,\text{err}} = 0.2$. Before calibration, the DNL contains a large number of missing codes. Comparing the result after three calibrations, the OHBRM achieves the highest improvement and its DNL is well within ± 0.5 LSBs. The conventional HBRM and MCD schemes exhibit the similar levels of accuracy. Table II summarizes the three calibration approaches. Depending on different targeted specifications, the proposed MCD and the OHBRM scheme provide a design option either for low area cost or better accuracy.

TABLE II
COMPARISON OF THREE CALIBRATIONS

Algorithm	Input constrain	|DNL| after Cal.	Cal. Time @80MS/s	Gate Count
HBRM	Uniform	<1LSB	8 us	~ 5k
OHBRM	Uniform	<0.5LSB	8 us	~ 5k
MCD	Continuous	<1LSB	3.2 us	~ 0.5k

V. CIRCUIT IMPLEMENTATION

A. Overall ADC Architecture

We implemented the proposed MCD calibration in an 11-bit SAR ADC operating at 80-MS/s [14] with the overall architecture shown in Fig. 9, which comprises a bridge DAC array, a comparator, a SAR controller, a TSG, and a calibration block. The SAR logic controls the DAC to perform the binary-searched feedback to the input signal, where we used the V_{cm}-based switching [5] for better conversion linearity. Once the MCD calibration is activated, the input signal is reconfigured to a staircase-type signal generated by the TSG to search for the number of missing codes, suspending the normal sampling operation of the DAC. After averaging the results, we obtain $\bar{N}_{\text{mc}}$ and store it in the calibration block; the ADC resumes its normal sampling. The raw digital output is processed by the calibration block to fix the error before the final output. One extra bit is resolved during the calibration to further suppress the quantization error and enhance the calibration accuracy. The MCD is based on 12-bit outputs, while the final ADC output is 11 bit.

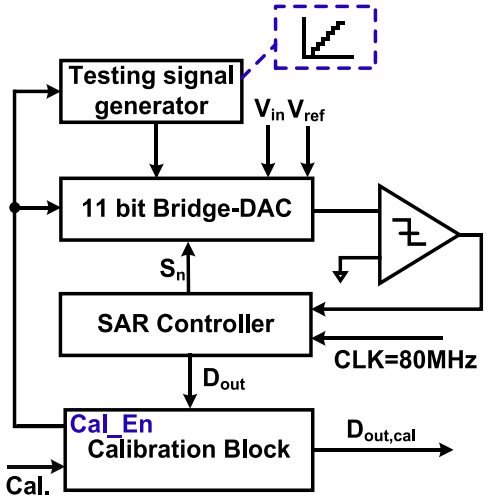


Fig. 9. Overall ADC architecture.

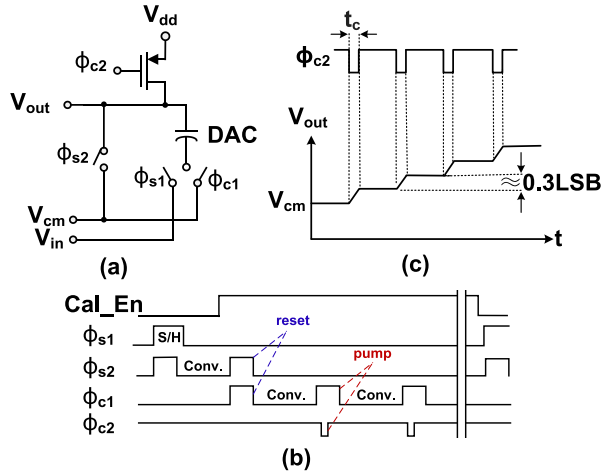


Fig. 10. (a) Architecture of the DAC and the TSG. (b) Timing diagram of the control clocks. (c) Top-plate voltage of the DAC array versus time.

We implemented an 11-bit bridge DAC where the attenuation capacitor C_a divides the capacitor array into (7-bit) MSB- and (4-bit) LSB-array. The unit capacitor is 5.68 fF resulting in the equivalent sampling capacitance of 727 fF. C_a is enlarged by 1.45× (8.78 fF) from its ideal value for the purpose of covering 45% of C_{PB} variation.

B. Proposed Testing Digital Generator

In this design, the MSB- and LSB-array quantizes 7 and 5 bit, respectively, accordingly the range of the TSG covers at least 2^5 codes which is 18.75 mV with a full scale of 2.4 V_{p-p}. Fig. 10(a) shows the TSG circuit [14], which uses a simple pMOS transistor at the top plate of the DAC working as a charge pump. According to the timing diagram shown in Fig. 10(b), before calibration, the input signal is sampled at the bottom plate of the DAC. Once the calibration is triggered (Cal_En = 1), the bottom-plate switches connecting to V_{in} are disabled. At the first sampling phase, both DAC top and bottom plates are reset to V_{cm}, after that the sampled signal is quantized normally. In the next sampling, the DAC top plate stops being reset to V_{cm} while the charge-pump circuit is activated, which generates a small voltage step above the previously sampled value. The transition level of ϕ_{c2} is from

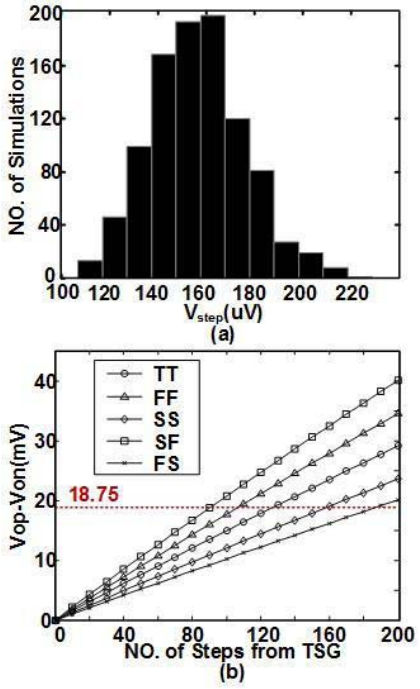


Fig. 11. (a) Histogram plot of V_{step} from 1000× MC-Process simulations. (b) Number of steps from the TSG versus its corresponding output voltage obtained at the DAC top-plate.

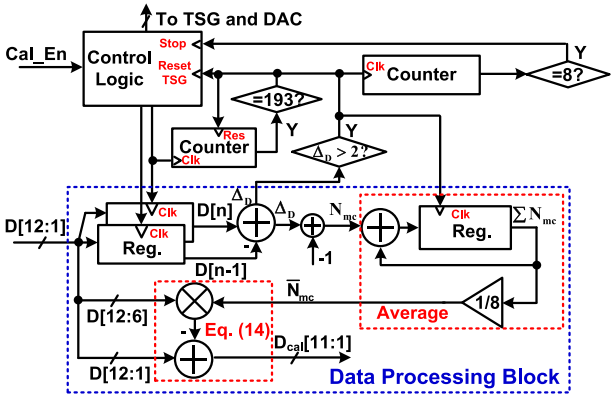


Fig. 12. Block diagram of the MCD calibration.

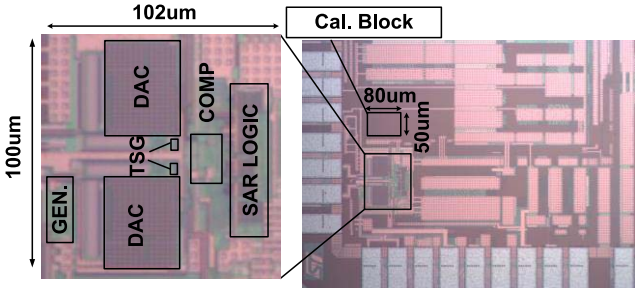


Fig. 13. Die microphotograph of the ADC and calibration block.

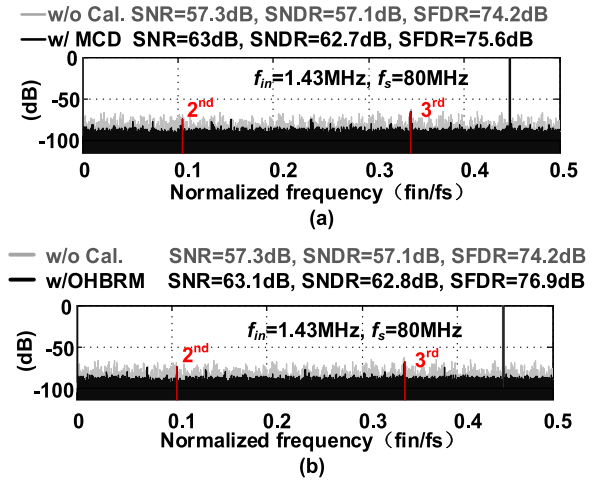


Fig. 14. Measured FFT at dc input (decimated by 25). (a) Before and after MCD Calibration. (b) Before and after OHBRM calibration.

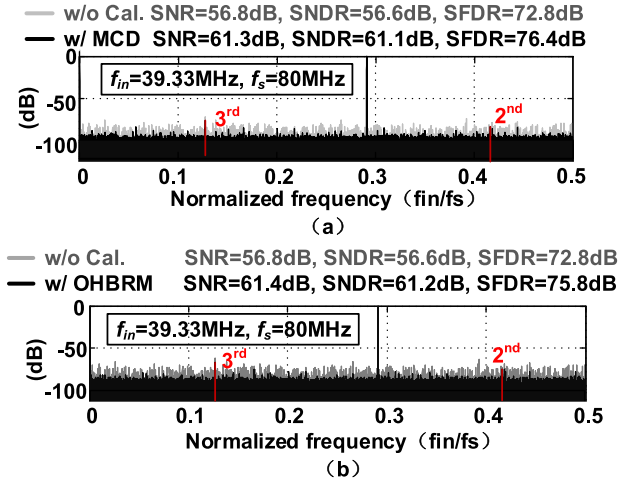


Fig. 15. Measured FFT at Nyquist input (decimated by 25). (a) Before and after MCD Calibration. (b) Before and after OHBRM calibration.

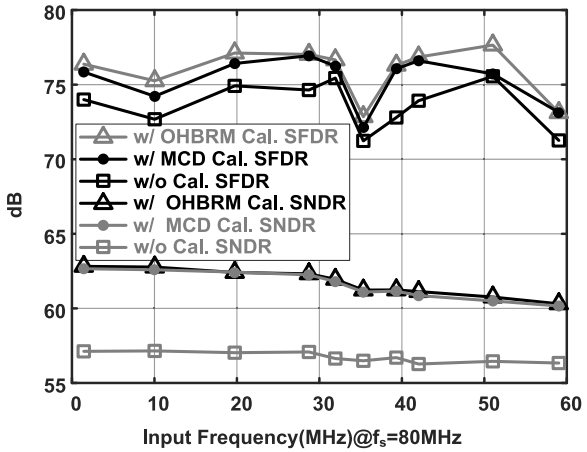


Fig. 16. Dynamic performance of the SAR ADC with and without two calibration schemes for different input frequencies.

V_{dd} to V_{cm} and by enabling the current source device for a short duration t_c(150 ps), the voltage step can be controlled to be sufficiently smaller than 1/2 LSB. According to 100 runs

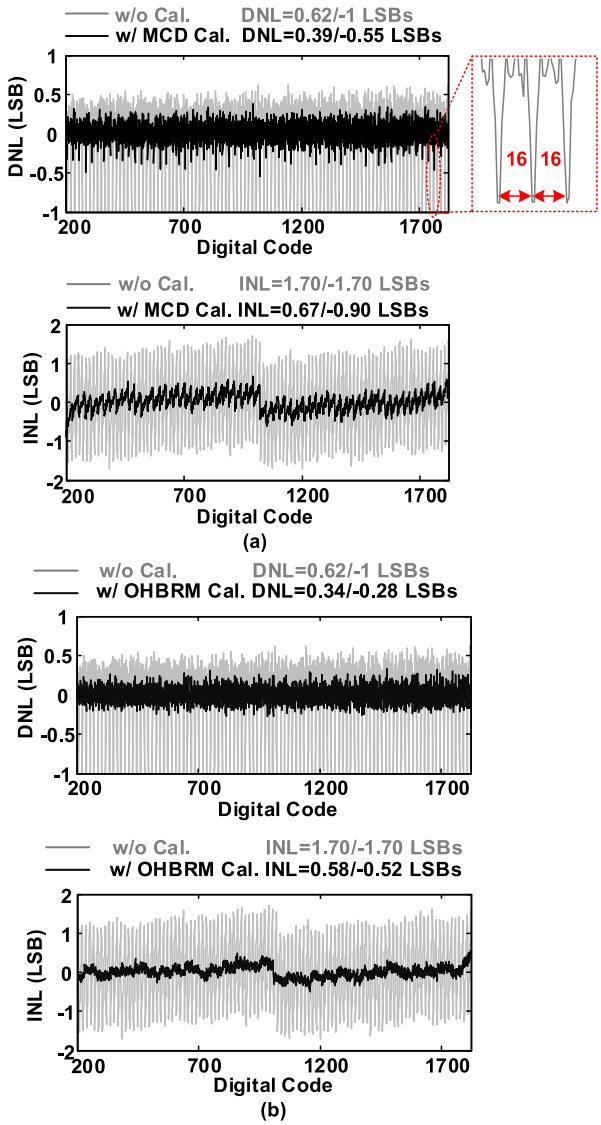


Fig. 17. Measured static performance. (a) Before and after MCD calibration. (b) Before and after OHBRM calibration.

of the MC process and mismatch simulation at 27 °C, the 3σ step size variation is around 32% with a mean of 158 μV. It guarantees that the minimum step size approximates 0.2 LSB under the 12-bit resolution, as illustrated in Fig. 11(a). Once the conversion is completed the bottom-plate switches are reset restoring the DAC output to its sampled value before the next incoming sampling. Consequently, the charge-pump circuit generates a staircase testing signal. As the DAC output increase shown in Fig. 10(c), V_{DS} of the current source decreases, leading to the reduction of the voltage step. However, this is not problematic as the testing signal does not need a good linearity and its voltage step lower than 1/2 LSB is enough to sense the missing codes. Under process variations, the TSG range is guaranteed to be larger than 18.75 mV corresponding to 2^I code width. As shown in Fig. 11(b), the TSG runs for 192 cycles that cover at least 18.75 mV under a minimum step size. The gain error estimation is based on 12-bit outputs, while the final ADC output is 11 bit.

TABLE III
SUMMARY OF PERFORMANCE AND BENCHMARK

	ISSCC '14 [17]	JSSC '15 [19]	ASSCC '16 [18]	TCASI'17 [7]	MCD Cal.	OHBRM Cal.
Architecture	Pipelined-SAR	Pipelined-SAR	SAR	Pipelined-SAR	SAR	SAR
Technology(nm)	28	40	40	65	65	65
Resolution(bit)	14	12	12	12	11	11
Sampling Rate(MS/s)	80	160	150	180	80	80
Supply Voltage(V)	1.0	1.1	0.9	1.2	1.2	1.2
Power(mW)	1.5	4.96	1.5	6	1.4	1.28
SNDR(dB) @ Nyquist	55	65	56.2	60.92	61.1	61.2
DNL(LSB)	N/A	N/A	1.77/-0.91	0.88/-0.6	0.39/-0.55	0.34/-0.28
Area(mm^2)	0.137	0.042	0.04	0.068	0.015	0.011
Cal. Gate Count(k)	N/A	0.2	N/A	N/A	0.5	5*
FoM @ Nyq.(fJ/conv.step)	11.5	20.6	18.9	36.7	20	18.3
Calibration	Off-chip	Off-chip	Off-chip	On-chip	On-chip	Off-chip

* Estimated gate count

C. Calibration Digital Block

Fig. 12 shows the block diagram of the MCD calibration. The Cal_En signal activates the TSG and disables the normal sampling in the ADC. The data processing block consists of several registers and arithmetic units. The registers store two adjacent outputs (D[n] and D[$n-1$]) and pass them to the subtractor to check whether the difference Δ_D is larger than 2. Considering that the noise may affect the conversion accuracy the detection threshold is set to 2. If it senses $\Delta_D > 2$, the TSG is reset and the number of missing codes $N_{\rm mc} = \Delta_D - 1$ will be stored. To average the noise, this operation repeats eight times. Once the counter arrives at 8, the calibration stops and the ADC resumes its normal sampling. Only the algorithm units designed to realize the function of (14) keep working, which consume 0.12 mW from the 1.2-V supply operating at 80 MHz. The total gate count to implement the MCD calibration is ~0.5 K occupying an area of 0.004 mm^2.

VI. MEASUREMENT RESULTS

Since the MCD calibration consumes less digital overhead, it was implemented on chip in an 11-bit, 80-MS/s SAR ADC in 65-nm CMOS with metal–oxide–metal capacitors. The OHBRM approach was verified off-chip. Fig. 13 shows the die microphotograph; the active area is 0.015 mm^2 including the calibration. Fig. 14 shows the measured fast Fourier transformation (FFT) without and with the two proposed calibrations at a dc input under a sampling rate of 80 MS/s. The spurs are widely spread over the spectrum, limiting the SNDR to 57.1 dB due to the gain error between the MSB- and LSB-array. After calibrations, the spurs are suppressed, and the two schemes result in a similar SNDR of ~62.7 dB. As discussed in Section IV-B, if the conversion is limited by other circuit nonidealities, the dynamic performance of the two calibrations will be similar. In this design, the switching noise and DAC mismatch limit the SNR to ~63 dB. The SNDR drops by 1.6 dB at a Nyquist input frequency as shown in Fig. 15. The spurious-free dynamic range is slightly improved by ≈1 dB, which is limited by the third harmonic caused by the DAC mismatches dominate over others. Fig. 16 shows the measured dynamic performance before and after calibrations where the SNDR remains above 60 dB up to a 59-MHz input frequency. The measured SNDR with OHBRM and MCD are similar, which matches the behavior simulation results of Section IV-B. Fig. 17 shows the measured static performance before and after two calibrations. The value of C_a is enlarged by 1.45× from its ideal value, which can theoretically compensate a γ of 45%. As the final ADC output is 11 bit, the code width of one segment is 2^4 codes. According to postlayout simulations, it is expected that there are three missing codes persegment, while due to process and mismatch the measured DNL contains a maximum of two missing codes. They are all removed after two calibrations. The accuracy difference between the two schemes can be demonstrated in the static measurement. The DNL and integral nonlinearity after the MCD calibration can be improved to 0.39/−0.55 and 0.67/−0.9 LSBs, respectively, while there are some residue errors still remaining near −0.5 LSBs persegment. In Fig. 17(b), those residue spurs are all sup-

pressed below −0.28 LSBs verifying the accuracy advantage of the OHBRM scheme. The total power consumption is 1.4 mW at 80 MS/s from a 1.2 V supply, where the analog and digital blocks (including calibration) consume 660 and 740 μW, respectively, leading to a figure-of-Merit (FoM) of 20 fJ/conv.-step at Nyquist input. Table III summarizes and compares the overall measured performance with the state-of-the-art SAR-type ADCs with similar specifications. The estimated gate count of OHBRM is ∼5k, which is much larger than the gate count obtained with the MCD algorithm. However, OHBRM is performed off-chip its area and digital power from calibration are not included in Table III. This paper with the MCD scheme exhibits an overall comparable FoM targeting high-conversion accuracy with the on-chip DAC error calibration.

VII. Conclusion

This paper discussed the conversion nonlinearity in a SAR ADC caused by the gain error in a bridge DAC. Its error characteristic is identical to the stage gain error in a two-stage ADC. Two schemes designated by OHBRM and MCD have been proposed, and their design considerations and limitations are analyzed. The OHBRM scheme achieves higher accuracy guaranteeing the DNL is within ±0.5 LSB while the tradeoff implies more digital overhead for code statistics. The MCD calibration slightly sacrifices the accuracy leading to significant hardware reduction due to the simplification of the algorithm. Implemented on chip, a TSG with low complexity, and good robustness remove the input constraint in both schemes.

References

[1] M. Yoshioka, K. Ishikawa, T. Takayama, and S. Tsukamoto, "A 10-b 50-MS/s 820-μW SAR ADC with on-chip digital calibration," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2010, pp. 384–385.

[2] W. Liu, P. Huang, and Y. Chiu, "A 12-bit, 45-MS/s, 3-mW redundant successive-approximation-register analog-to-digital converter with digital calibration," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2661–2672, Nov. 2011.

[3] S. Liu, Y. Shen, and Z. Zhu, "A 12-bit 10 MS/s SAR ADC with high linearity and energy-efficient switching," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 10, pp. 1616–1627, Oct. 2016.

[4] A. H. Chang, H. S. Lee, and D. Boning, "A 12 b 50 MS/s 2.1 mW SAR ADC with redundancy and digital background calibration," in *Proc. IEEE ESSCIRC*, Sep. 2013, pp. 109–112.

[5] Y. Zhu *et al.*, "A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.

[6] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.

[7] J. Zhong, Y. Zhu, C.-H. Chan, S.-W. Sin, U. Seng-Pan, and R. P. Martins, "A 12 b 180 MS/s 0.068 mm^2 with full-calibration-integrated pipelined-SAR ADC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 7, pp. 1684–1695, Jul. 2017.

[8] Y. Chen *et al.*, "Split capacitor DAC mismatch calibration in successive approximation ADC," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2009, pp. 279–282.

[9] H.-S. Lee, D. A. Hodges, and P. R. Gray, "A self-calibrating 15 bit CMOS A/D converter," *IEEE J. Solid-State Circuits*, vol. JSSC-19, no. 6, pp. 813–819, Dec. 1984.

[10] Y. Zhu, C.-H. Chan, S.-S. Wong, U. Seng-Pan, and R. P. Martins, "Histogram-based ratio mismatch calibration for bridge-DAC in 12-bit 120 MS/s SAR ADC," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 3, pp. 1203–1207, Mar. 2016.

[11] W. Liu, P. Huang, and Y. Chiu, "A 12-bit 50-MS/s 3.3-mW SAR ADC with background digital calibration," in *IEEE CICC Dig. Tech. Papers*, Sep. 2012, pp. 1–4.

[12] W. Liu, P. Huang, and Y. Chiu, "A 12 b 22.5/45 MS/s 3.0 mW 0.059 mm^2 CMOS SAR ADC achieving over 90 dB SFDR," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2010, pp. 380–381.

[13] Y. Zhu, C. H. Chan, U. Seng-Pan, and R. P. Martins, "A 10.4-ENOB 120 MS/s SAR ADC with DAC linearity calibration in 90 nm CMOS," in *Proc. IEEE A-SSCC*, Nov. 2013, pp. 69–72.

[14] G. C. Wang, Y. Zhu, C.-H. Chan, U. Seng-Pan, and R. P. Martins, "A missing-code-detection gain error calibration achieving 63 dB SNR for an 11-bit ADC," in *Proc. IEEE ESSCIRC*, Sep. 2017, pp. 239–242.

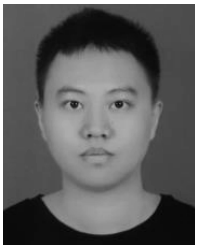
[15] N. Sun, "Exploiting process variation and noise in comparators to calibrate interstage gain nonlinearity in pipelined ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 4, pp. 685–695, Apr. 2012.

[16] L. Brooks and H. S. Lee, "Background calibration of pipelined ADCs via decision boundary gap estimation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 10, pp. 2969–2979, Nov. 2008.

[17] F. van der Goes *et al.*, "A 1.5 mW 68 dB SNDR 80 Ms/s 2× interleaved pipelined SAR ADC in 28 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 200–201.

[18] K.-H. Chang and C.-C. Hsieh, "A 12 bit 150 MS/s 1.5 mW SAR ADC with adaptive radix DAC in 40 nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2016, pp. 157–160.

[19] Y. Zhou, B. Xu, and Y. Chiu, "A 12 bit 160 MS/s two-step SAR ADC with background bit-weight calibration using a time-domain proximity detector," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 920–931, Apr. 2015.



Guan Cheng Wang was born in Guangdong, China, in 1992. He received the B.S. degree in automation from Sun Yat-sen University, Guangzhou, in 2014, and the M.S. degree in electrical and computer engineering from the University of Macau, Macau, China, in 2017.

From 2014 to 2017, he was with the Research Group, State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. His current research interests include calibration algorithm for ADCs, analog and mixed-signal circuit designs, and signal processing.

Yan Zhu (S'10–M'12) received the B.Sc. degree in electrical engineering and automation from Shanghai University, Shanghai, China, in 2006, and the M.Sc. and Ph.D. degrees in electrical and electronics engineering from the University of Macau, Macau, China, in 2009 and 2011, respectively.

She is currently an Assistant Professor at the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. Her current research interests include low-power and wideband high-speed Nyquist A/D converters as well as digitally assisted data converter designs. She has authored or coauthored over 50 technical journals and conference papers in her field of interests. She holds three U.S. patents.

Dr. Zhu was a recipient of the Best Paper Award in ESSCIRC 2014, the Student Design Contest Award in A-SSCC 2011, and the Chipidea Microelectronics Prize and the Macao Scientific and Technological Research and Development Awards in 2012, 2014, and 2016 for outstanding academic and research achievements in microelectronics.

Chi-Hang Chan (S'12–M'15) was born in Macau, China, in 1985. He received the B.S. degree in electrical engineering from the University of Washington, Seattle, WA, USA, in 2008, the M.S. and Ph.D. degrees from the University of Macau, Macau, in 2012 and 2015, respectively.

He was an Intern with Synopsys Macau Ltd., Macau. He is currently an Assistant Professor at the University of Macau. His current research interests include Nyquist ADC, mixed-signal circuits, comparator offset calibration, flash, and multibit SAR ADC.

Dr. Chan was a recipient of the Chipidea Microelectronics Prize and the Macau Science and Technology Development Fund (FDCT) Postgraduates Award (Master Level) in 2012 and 2011, respectively, the Macau FDCT Award for Technological Invention (Second Class), the Macao Scientific and Technological Research and Development for Postgraduates Award (Ph.D. Level) in 2014 for outstanding academic and research achievements in microelectronics, and the 2015 Solid-State-Circuit-Society (SSCS) Pre-Doctoral Achievement Award. He was a co-recipient of the 2011 ISSCC Silk Road Award and Student Design Contest Award in A-SSCC 2011.

Seng-Pan U (Ben) (S'94–M'00–SM'05–F'16) received the B.Sc. and M.Sc. degrees from the University of Macau (UM), Macau, China, in 1991 and 1997, respectively, and the dual Ph.D. degrees (Hons.) in high-speed analog IC design from UM and the Instituto Superior Técnico (IST), Lisbon, Portugal, in 2002 and 2004, respectively.

Since 1994, he has been with the Faculty of Science and Technology, UM, where he is currently a Professor and the Deputy Director of the State Key Laboratory of Analog and Mixed-Signal (AMS) VLSI. From 1999 to 2001, he was on leave from the Integrated CAS Group, Center of Microsystems, IST, as a Visiting Research Fellow. In 2001, he was a Co-Founder of the Synopsys Macau Ltd., Macau, where he has been the Engineering Director since 2003. He is also the Corporate Senior Analog and Mixed-Signal Design Manager and the Site General Manager of the Synopsys Macau Ltd. He has authored or coauthored over 140 publications, 4 books in Springer and China Science Press in the area of VHF SC filters, analog baseband for multistandard wireless transceivers and very high-speed TI ADCs. He co-holds 10 U.S. patents.

Dr. U is a member of the Science and Technology (S&T) Commission of China Ministry of Education. He was also elected as the Scientific Chinese of the Year 2012. He was a recipient of nearly 30 research and academic/teaching awards including the 2012 IEEE SSCS Outstanding Chapter Award, as the Macau founding Chairman, the S&T Innovation Award of Ho Leung Ho Lee Foundation in 2010 and The State S&T Progress Award in 2011, both at the first time from Macau, the 2012 and 2014 Macau S&T Invention and Progress Awards, and the Honorary Title of Value in 2010 by Macau SAR Government for the recognition of his contribution in academic research and industrial development. He was a co-recipient of the 2014 ESSCIRC Best Paper Award. He is also the Advisor for nearly 30 various international student paper award recipients including the SSCS Pre-Doctoral Achievement Award, the ISSCC Silk Road Award, the A-SSCC Student Design Contest, the IEEE DAC/ISSCC Student Design Contest, ISCAS, MWSCAS, and PRIME. He is currently the Founding Chairman of IEEE SSCS and the Chairman of CAS/COMM Macau chapter. He was the Program Committee Chair of the IEEJ AVLSIWS, IEEE APCCAS, ICICS, PRIMEAsia, and IEEE ASP-DAC'16. He is currently the TPC Chair of ISSCC, A-SSCC, and RFIT, and the Analog Sub-Committee Chair of VLSI-DAT, and an Editorial Board Member of the *Journal of Analog Integrated Circuits and Signal Processing.*From 2014 to 2015, he was the IEEE SSCS Distinguished Lecturer and the A-SSCC 2013 Tutorial Speaker. He has been with technical review committee of JOURNAL OF SOLID-STATE CIRCUITS, TRANSACTIONS ON CIRCUITS AND SYSTEMS, and the IEEE TVLSI.

Rui P. Martins (M'88–SM'99–F'08) was born in 1957. He received the bachelor's, master's, Ph.D., and the Habilitation for Full Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), University of Lisbon, Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

Since 1980, he has been with the Department of Electrical and Computer Engineering, IST. Since 1992, he has been on leave from IST, where he is with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macau, China, where he has been a Chair Professor since 2013. From 1994 to 1997, he was the Dean of the Faculty with FST. Since 1997, he has been the Vice-Rector of UM. In 2008, after the reform of the UM Charter, he was nominated after open international recruitment, and reappointed, in 2013, as Vice-Rector (Research) until 2018. From 2001 to 2002, he was a Co-Founder of Synopsys Macau Ltd., Macau. In 2003, he created the Analog and Mixed-Signal VLSI Research Laboratory, UM, elevated in 2011 to the State Key Laboratory of China (the first in Engineering in Macau), where he became a Founding Director. Within the scope of his teaching and research activities, he has taught 21 bachelor and master courses and has supervised or co-supervised 40 theses: Ph.D. (19) and master's (21). He has coauthored over 6 books and 12 book chapters, 400 papers, in scientific journals (126) and in conference proceedings (274), as well as other 62 academic works, in a total of 505 publications. He holds 23 USA patents and 2 Taiwan patents.

Dr. Martins was a Circuits and Systems Society (CASS) representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)–Director of the IEEE. He was a recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999 and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001, and the Best Associate Editor of T-CAS II from 2012 to 2013. He was the Founding Chairman of both the IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on CAS/Communications from 2005 to 2008 (2009 World Chapter of the Year of IEEE CASS). He was the General Chair of the 2008 IEEE Asia–Pacific Conference on CAS—APCCAS'2008 and the Vice President for Region 10 (Asia, Australia, and the Pacific) of IEEE CASS from 2009 to 2011. He was the Vice President (World) Regional Activities and Membership of IEEE CASS from 2012 to 2013, and an Associate Editor of the IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS from 2010 to 2013. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference—ASP-DAC'2016 and received the IEEE Council on Electronic Design Automation Outstanding Service Award 2016. He is a Nominations Committee Member of IEEE CASS from 2016 to 2017. He is currently the Chair of the IEEE CASS Fellow Evaluation Committee (Class 2018). In 2010, he was elected, unanimously, as a Corresponding Member of the Portuguese Academy of Sciences, in Lisbon, being the only Portuguese Academician living in Asia.