INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS
Int. J. Circ. Theor. Appl. 2013
Published online in Wiley Online Library (wileyonlinelibrary.com). DOI: 10.1002/cta.1933

LETTER

A 3.6-mW 6-GHz current-reuse VCO-buffer with improved load drivability in 65-nm CMOS

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ABSTRACT

A new current-reuse voltage-controlled oscillator (VCO)-buffer with enhanced load drivability is proposed. It incorporates a PMOS-based source follower stacked atop a NMOS-based LC VCO to share the bias current, while preventing the voltage stress at any oscillation node from exceeding the 1.2-V technology voltage limit. Also, ac-coupling networks are avoided between the VCO and buffer, improving the Q of the LC tank while minimizing parasitics. With internal buffering, the VCO can directly drive up a 50-Ω load for testing, or to withstand a large capacitive load in on-chip local oscillator distribution, particularly suitable for multi-band MIMO WLAN radios. The fabricated VCO-buffer in 65-nm CMOS measures 13.8% tuning range from 5.64 to 6.4 GHz, consumes 3.6 mW at 1.2 V and exhibits −108.84 dBc/Hz phase noise at 1-MHz offset.

Received 4 March 2013; Revised 13 May 2013; Accepted 16 May 2013

1. INTRODUCTION

Voltage-controlled oscillator (VCO) is the core circuit for generating a poly-phase local oscillator (LO) signal for most wireless transceivers [1] with image rejection, harmonic rejection or phased array architecture. The most widespread way to generate a number of LO phase is by frequency division. The frequency dividers [2] entail the VCO to deliver an adequate voltage swing, but its drivability and resonant frequency can be limited by the size of the resistive and/or capacitive load. Although VCO buffering can be added to enhance the drivability and reverse isolation (i.e. the effects of load pulling and load variation to the VCO), the power efficiency can be penalized. An example is given in Figure 1, where a multi-band MIMO WLAN transceiver features numerous receiver (RX) and transmitter (TX) paths distributed over a system-on-a-chip [3], involving heavy LO signal distribution. Since each divider has to drive a considerable load capacitance, their wide transistors impose a large capacitance to the VCO.

This Letter proposes a current-reuse VCO-buffer. Fabricated in 65-nm CMOS, it is capable to drive the 50-Ω port of equipment for direct testability, while maintaining adequate output swing and isolation between the load and the LC tank of the VCO. The achieved power consumption (3.6 mW) is highly comparable with other standalone VCOs.

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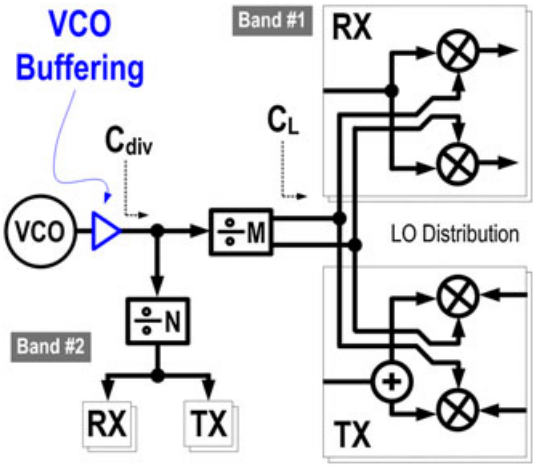

Figure 1. VCO in a multi-band MIMO transceiver requires high capacitive-load drivability.

2. PROPOSED CURRENT-REUSE VCO-BUFFER

Figure 2(a) depicts the schematic of the proposed current-reuse VCO-buffer. Designed for a 1.2-V supply (V_{DD}) in 65-nm CMOS, the power can be reduced by sharing the bias current between a NMOS-based *LC* VCO (bottom) and a PMOS-based source follower (top). The latter not only helps to bias the VCO in the current-limited operation region, but also matches its input common-mode level with that of the VCO's output. Thus, no ac-coupling network is entailed that would otherwise degrade the Q of the LC tank, while increasing the die area and parasitics. Aside, since V_X can be set midway the V_{DD}, the peak output swing of the VCO can be controlled within the reliable voltage limits of the cross-coupled transistors (M_1 and M_2), preventing voltage overstressing at all time. Decoupling capacitor (C_{dec} = ~3 pF) on V_x sufficiently avoids the noise coupling between the VCO and buffer. Thus, this topology also can simplify the need of a dedicated low-voltage V_{DD} (i.e. 0.6 V) that was commonly employed in prior art [4]. In the buffer, M_4 and M_5 are loaded with resistors (R_B) to lower their output resistance (i.e. better drivability). Furthermore, there is no nonlinearity due to the body effect since the body-source of M_4 and M_5 can be tied together. The output common-mode level of the buffer is one V_{GS} greater than that of the VCO, consuming certain voltage headroom and thereby limiting the voltage swing. Figure 2

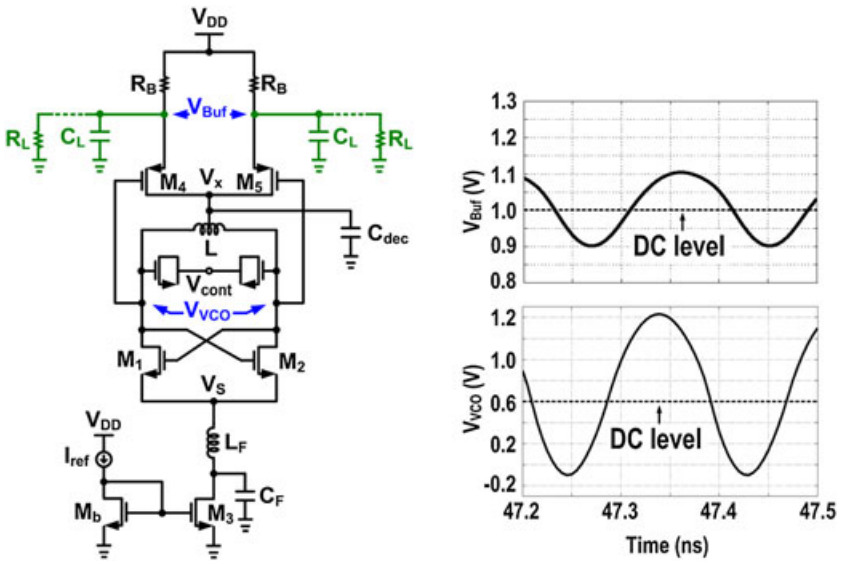

Figure 2. Proposed current-reuse VCO-buffer. (a) Schematic. (b) Simulated transient waveforms at V_{Buf} (upper) and V_{VCO} (lower).

DOI: 10.1002/cta

(b) shows the simulated output swings at V_{VCO} and V_{Buf}. Nevertheless, if each injection-locked frequency divider (see Figure 1) is properly designed to locate their self-resonant frequency close to the VCO's oscillation frequency (f_{osc}), a swing of a few hundreds of mV at V_{Buf} is already adequate [5], balancing the phase noise with the number of dividers that can be driven simultaneously.

Since V_x is only a portion of the V_{DD}, the sensitivity of the VCO to V_{DD}'s noise is different from the conventional NMOS-based *LC* VCO. Here, the V_{DD}'s noise coupled to the VCO is lower due to the voltage division between the buffer and VCO. Moreover, even if a 5% mismatch is set between M_4 and M_5, the simulated phase noise has very limited degradation of less than 1 dB up to 1-MHz offset as shown in Figure 3.

If the V_{DD} is well-regulated, a topology without additional bias current source can be used to minimize the phase noise and maximize the output swing. However, a NMOS current source (M_3) could still be exploited when the robustness is a priority. The noise induced by M_3 can be suppressed via adding a LC filter (L_F and C_F). With it, the noise of the VCO at the second harmonic and the current injection of the LC tank at zero crossing, are both reduced due to the increment of impedance at V_s and the absorption of an abrupt change of current. Hence, the phase noise and robustness of the VCO can be improved at the expense of certain chip area.

There exists a unique optimization process when sizing the buffer. Figures 4(a)–(c) show the simulated variations of phase noise, f_{osc} and output swing against the load capacitance and under different buffer's sizes. If M_4 and M_5 are sized as 200/0.24 μm (100/0.24 μm), the phase noise will vary by 4.4 dB (2.4 dB), f_{osc} will vary by 200 MHz (110 MHz) and the output swing will vary by 115 mV (160 mV) over a capacitive load from 0.5 to 1 pF. It is also observable that a bigger load capacitance benefits the phase noise at the expense of output swing in all cases. Thus, to leverage them while offering an output resistance of 50 Ω to ease the testing, the size of M_4 and M_5 was chosen as 140/0.24 μm to achieve $g_{m4} = g_{m5} = 12$ mS, and R_B was set as 120 Ω. This R_B also allows the V_{BUF} to stay at a common mode of ~1 V and deliver an output swing of 280 mV_{pp} up to a 1-pF load. The variations of f_{osc} and phase noise are within 140 MHz and 3.3 dB, respectively. The noise contribution of M_4 and M_5 is 15% of the total phase noise at 1-pF load, but can be increased to 35% if the load is as low as 200 fF. Thus, the phase noise can be optimized if the VCO-buffer and dividers are concurrently designed, so that the load capacitance and entailed output swing are known beforehand.

3. EXPERIMENTAL RESULTS

The VCO-buffer was fabricated in 65-nm CMOS (Figure 5). A differential inductor is designed for the *LC* tank to enhance the *Q* and area efficiency. The die size is around 580×285 μm^2 and the power is 3.6 mW at 1.2 V. With inherent buffering, it can directly drive the 50-Ω port of

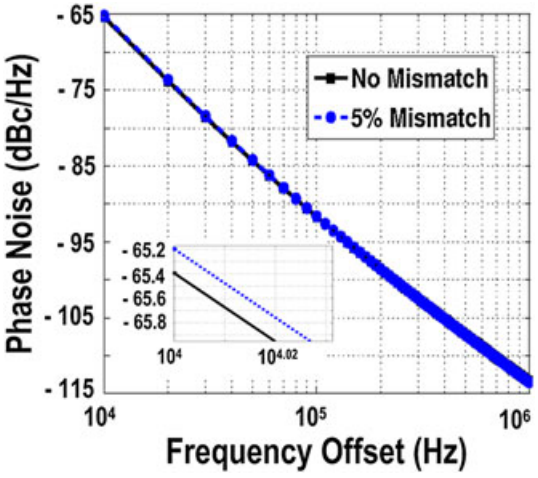

Figure 3. Simulated phase noise for 5% transistor mismatch between M_4 and M_5.

DOI: 10.1002/cta

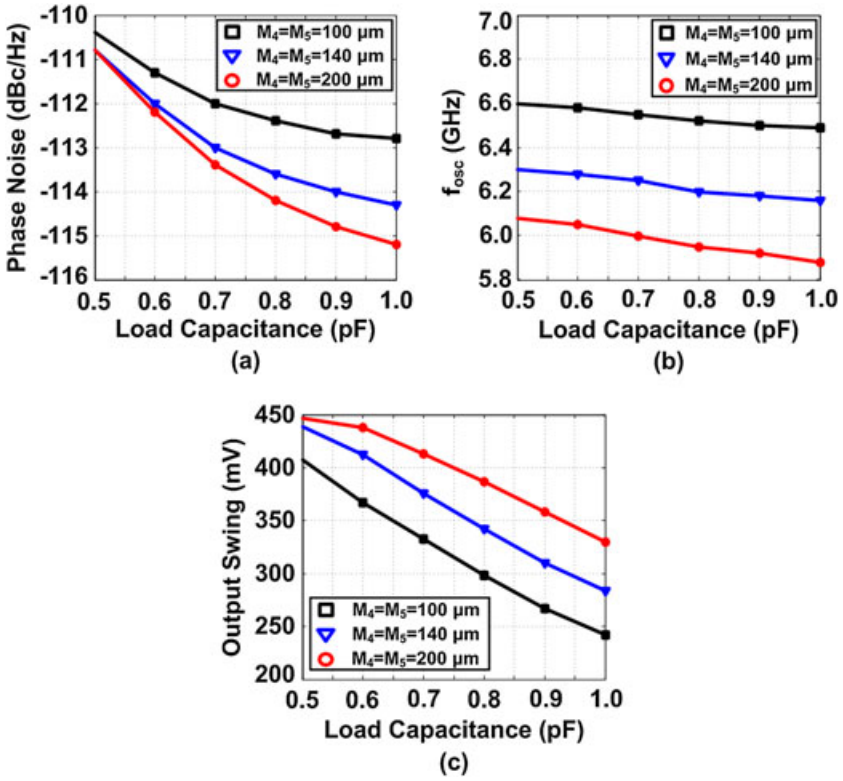

Figure 4. Simulated variations of (a) phase noise, (b) f_{osc} and (c) output swing against the load capacitance under different buffer's sizes.

the spectrum analyzer for measurements. The output capacitance is ~1 pF including the parasitics from the pad with ESD diodes and the PCB trace. The achieved tuning range is from 5.64 to 6.48 GHz. The output spectrum [Figure 6(a)] shows a signal power of −33.59 dBm at a 6.4 GHz carrier frequency, and the phase noise is −108 dBc/Hz at 1 MHz offset [Figure6(b)]. The single-ended output power varies between −33.59 and −48.2 dBm over the covered frequency range. The key performance metrics and a comparison with other VCOs are summarized in Table I. The proposed current-reuse VCO-buffer not only shows enhanced load drivability, but also maintains a comparable Figure-of-Merit (FoM) with respect to the prior art [6, 7].

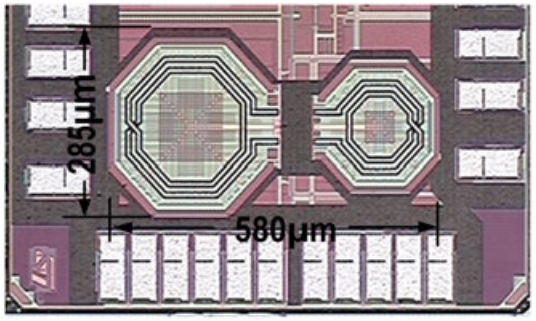

Figure 5. Die photo of the current-reuse VCO-buffer.

DOI: 10.1002/cta

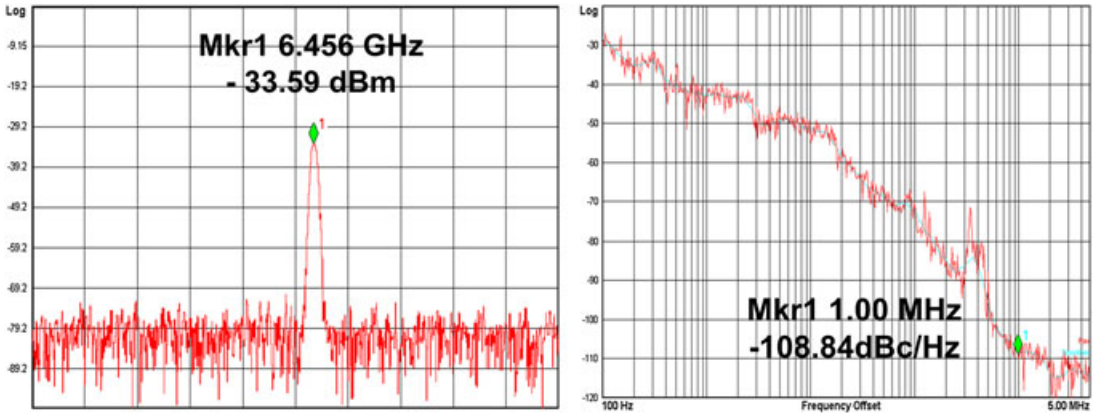

Figure 6. Measured results: (a) Output spectrum. (b) Phase noise at 6.4 GHz.

Table I. Performance summary and comparison.

Performance	[6]	[7]	This work
Technology	90-nm CMOS	65-nm CMOS	**65-nm CMOS**
Supply (V)	1.6	1.2	**1.2**
Power (mW)	14	20.4	**3.6**
Frequency (GHz)	5.6	6.67	**6.4**
Tuning range (GHz)	4.5–7.1 (45%)	5.9–7.8 (28.8%)	**5.64–6.48 (13.8%)**
Phase noise (dBc/Hz) @ 1 MHz offset	−108.5	−109.7	**−108.84**
FOM (dBc/Hz) *	−171.7 (VCO only)	−173 (VCO only)	**−180 (VCO + Buffer)**

$$*FoM = 10\log_{10}\left(\left(\frac{f_{osc}}{\Delta f}\right)^2 \frac{1}{L(\Delta f)P_{diss}(mW)}\right)$$

4. CONCLUSIONS

A current-reuse VCO-buffer using a PMOS-based source follower stacked atop a NMOS-based *LC* VCO has shown enhanced load drivability. It not only shares the bias current between the VCO and buffer for better power efficiency, but also avoids any ac-coupling network that reduces the die area and parasitics. Since the bias current is shared between the VCO and buffer, the key performance metrics (e.g. phase noise, f_{osc} and output swing) should be optimized concurrently with respect to the size and range of the load capacitance. With low output resistance, the VCO-buffer can directly drive the 50-Ω port of equipments for testing, or to drive a number of dividers in on-chip LO signal distribution. The 65-nm CMOS prototype measured 13.8% tuning range from 5.64 to 6.4 GHz, 3.6 mW of power and −108.84 dBc/Hz phase noise at 1 MHz offset. Although the achieved output swing is not as high as that of conventional designs, a proper co-design between the VCO-buffer and its succeeding injection-locked frequency dividers should render this work the potential capability of power savings in multi-band MIMO WLAN radios.

ACKNOWLEDGEMENTS

This research is funded by Macau Science and Technology Development Fund (FDCT) and University of Macau Research Committee.

DOI: 10.1002/cta

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DOI: 10.1002/cta