Thermal and Reference Noise Analysis of Time-Interleaving SAR and Partial-Interleaving Pipelined-SAR ADCs

Jianyu Zhong, *Student Member, IEEE*, Yan Zhu, *Member, IEEE*, Sai-Weng Sin, *Senior Member, IEEE*, Seng-Pan U, *Senior Member, IEEE*, and Rui Paulo Martins, *Fellow, IEEE*

***Abstract*—This paper analyzes the thermal and reference noises of two types of successive-approximation-register (SAR) analog-to-digital converters (ADCs): the time-interleaving (TI) and the partial-interleaving (PI) Pipelined. The thermal noise is investigated with accurate estimation by deriving closed-form expressions according to the noise equivalent models on different phases. Additionally, the design trade-off between power and noise for two ADC architectures is discussed in detail. On the other hand, the reference noise due to the large switching transient, which significantly degrades the conversion accuracy, is analyzed and verified through behavioral and circuit level simulations of two ADC architectures operating at 500 MS/s for 10-bit resolution. The simulated results show the supremacy of the PI Pipelined-SAR (PS) architecture over the TI-SAR because it exhibits less reference noise sensitivity.**

***Index Terms*—analog-to-digital converter (ADC), reference noise, successive-approximation-register (SAR) ADC, thermal noise.**

I. Introduction

TECHNOLOGY scaling benefits the digital circuitry, therefore, the SAR ADCs due to its highly digital nature and sequential operation achieve excellent power efficiency with a sampling rate lower than 200 MS/s and medium to high resolution [1]–[5]. To further boost its conversion speed to the GHz range, the SAR ADC can be designed with a TI scheme [6]–[8], where spurs due to gain, offset and timing mismatches limit both spurious free dynamic range (SFDR) and signal to noise ratio (SNR). The former two terms (gain and offset) can be compensated with low power and area costs and have been addressed extensively in the literature [9], [10], thus, the timing mismatch becomes the most critical limitation. Some previous works use TI-SAR ADCs with time-skew-calibrations [11], [12]; avoiding the time skews with the common T/H [13]; using architecture optimization such as the PI topology [14]. The designs achieve near 8.5ENOB with excellent FoM$<$100 fJ/conv.step. The timing-calibrated TI-SAR ADC removes the power and accuracy trade-off in the clock generator. As the ADC operates dynamically, its power increases linearly with the number of channels. The PI PS ADC avoids the time skew error by implementing a full-speed 2 b/cycle conversion at the 1st-stage, while interleaving the residue multiply digital-to-analog converter (MDAC) and the 2nd-stage SAR ADCs at the backend. As the sampling instant is only determined by the master clock, precise TI clock distribution is not required. Therefore, the clock generation can be designed with very low power to satisfy the jitter requirement only. Consequently, the PI PS ADC architecture maintains its superiority in power efficiency when compared with the timing-calibrated TI-SAR ADC.

Besides the mismatch errors, in high speed ADC designs the circuit thermal and reference noises are the ultimate limiting factors to the achievable SNR, especially when targeting for medium to high resolution. The kT/C noise can be suppressed by enlarging the array capacitance, while the reference noise is a challenging issue in SAR ADCs.

In practice, the analog circuitry is normally biased by a dedicated linear voltage regulator to isolate the large system digital noise. Also, the proper placement of decoupling capacitors can effectively attenuate the high-frequency noise. However, the on-die area budget for decoupling capacitors is limited in practical designs. Therefore, the reference ripple due to the switching transient becomes the main limitation in high-speed and high-resolution ADC designs. For example, targeting for a 12-bit resolution SAR ADC with V_{cm}-based switching, implies that the reference variation needs to be suppressed within $\pm$0.012% of the full scale [15], however, the high-speed SAR loop may not provide sufficient time for the reference to settle within the accuracy requirement before the next bit comparison. To relax the settling accuracy during large switch transients, some SA searching algorithms like the non-binary conversion [16] and the error-compensation [17] are effective approaches to relax this effect.

This paper investigates the effects of thermal and reference noises in two high-speed SAR-type architectures: TI-SAR and PI PS. According to the ADC operation, each circuit block is replaced by its equivalent noise model, which allows the derivation of the corresponding closed-form noise expression. Besides, for design considerations based on noise and power optimization in the two ADC architectures, the relationship between the noise and the power dissipation for the main analog building blocks (opamp and comparator) is analyzed. The corresponding power budget for two design examples of 500 MS/s 10-bit ADCs are provided. The thermal noise analysis is verified through transistor-level simulations with Cadence. Moreover, comparative analysis based

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J. Zhong, S.-W. Sin, and S.-P. U are with State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China. They are also with the Department of ECE, University of Macau, Macao, China (e-mail: jankeyzhong@gmail.com).

Y. Zhu is with State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China.

R. P. Martins was with State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China. He was also with the Department of ECE, University of Macau, Macao, China. He is on leave from Instituto Superior Técnico/Universidade de Lisboa, Lisboa 1649-004, Portugal (e-mail: rmartins@umac.mo).

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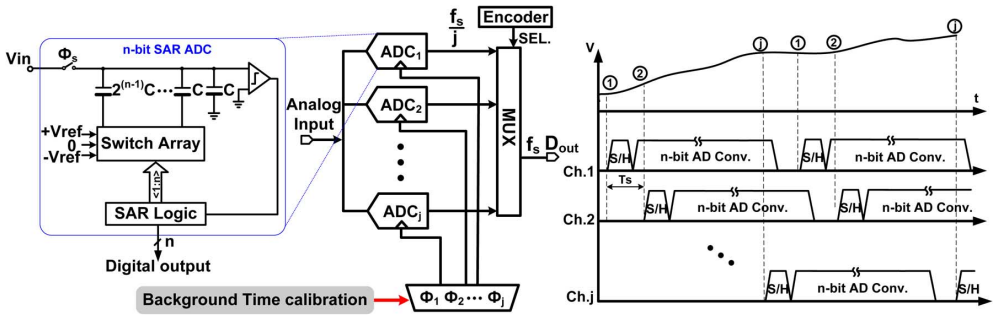


Fig. 1. TI-SAR ADC architecture and its timing diagram.

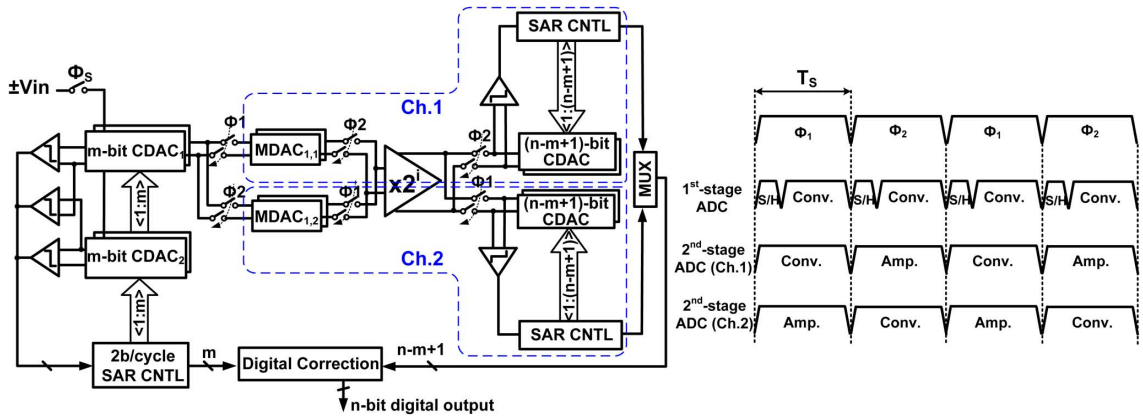


Fig. 2. PI PS ADC architecture and its timing diagram [14].

on the interference of reference noise among the sub-channels in the TI-SAR ADC as well as the sub-stages in the PI PS ADC is presented, which is verified by both behavioral and transistor-level simulations.

II. ADC Architecture

As mentioned in the introduction, the analysis is based on two high-speed architectures that are shown in Figs. 1 and 2. An n-bit j × TI-SAR ADC with corresponding timing diagram is described in Fig. 1, which consists of a number of j TI-SAR ADCs to achieve an aggregate sampling frequency f_S. The SAR ADC in each channel is built with an n-bit binary-weighted capacitive DAC (CDAC), a comparator and SAR control logic. The input signal is sampled passively onto the CDAC in each channel according to the time sequence $\Phi_1 \sim \Phi_j$, which is non-overlapped.

Fig. 2 shows the architecture of an n-bit PI PS ADC [14] with the corresponding timing diagram. The 1st-stage consists of a 2 b/cycle SAR ADC operating at full clock rate to determine the coarse m-bit in m/2 conversion cycles, which is shared by 2 × TI MDACs ($\mathrm{MDAC}_{1,1}$ & $\mathrm{MDAC}_{1,2}$) to perform the residue amplification. The opamp is shared between two channels due to low power consideration with a stage-gain of 2^i. The 2nd-stage contains 2 × TI-SAR ADCs to resolve the fine $(\mathrm{n}-\mathrm{m}+1)$-bit output. Two stages have one-bit overlapping for digital error correction (DEC) relaxing the conversion accuracy in the 1st-stage to $(\mathrm{m}+1)$-bit.

III. Thermal Noise and Power Analysis

This section discusses the overall input-referred noise in the TI-SAR and PI PS architectures mentioned in the above section. The thermal noise contributions from the main analog building blocks in two SAR-type ADCs, including the sampling network, the comparator and the opamp, are derived with closed-form expressions according to the noise equivalent models. Also, the power budget from the analog circuitries according to the noise requirement is quantitatively analyzed. The digital power from the SAR logic that is noise uncorrelated will be ignored in the discussion.

A. TI-SAR ADC

The noise analysis of the TI-SAR ADC (Fig. 1) is based on the noise contributions from kT/C and comparator in each individual channel. In a SAR ADC, the SNR including the quantization noise power N_Q is calculated as

$$\mathrm{SNR} = 10\log\left(\frac{\frac{V_{FS}^2}{8}}{N_{Cs}+N_{Cmp}+N_Q}\right), \tag{1}$$

where V_{FS} is the full-scale of the ADC, N_{Cs} and N_{Cmp} are the noise power from the sample-and-hold (S&H) network and the comparator, respectively. For an n-bit ADC, the quantization noise power is calculated as

$$N_Q = \frac{\Delta^2}{12} = \frac{\left(\frac{V_{FS}}{2^n}\right)^2}{12}, \tag{2}$$

where Δ indicates the least significant bit (LSB) of the ADC. The noise of sampling and comparator normalized to N_Q is $N_{Cs} = K_1 N_Q$ and $N_{Cmp} = K_2 N_Q$, respectively, which results in the total noise budget of $(1+K_1+K_2)N_Q$. As the noise generated from two differential DACs is uncorrelated, N_{Cs} is the sum of the kT/C noise power generated from the differential CDACs, and it is expressed as

$$N_{Cs} = \frac{2kT}{C_s}, \tag{3}$$

where k and T represent the Boltzmann constant and the absolute temperature, respectively, and C_s is the required minimum sampling capacitance in one of the differential CDACs. With $N_{Cs} = K_1 N_Q$, C_s can be calculated as

$$C_s = \frac{2kT}{N_{Cs}} = \frac{2kT}{K_1 N_Q}. \tag{4}$$

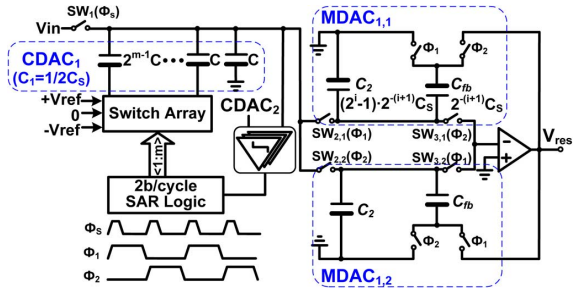


Fig. 3. The 1st-stage m-bit SAR ADC with opamp-shared TI-residue amplification.

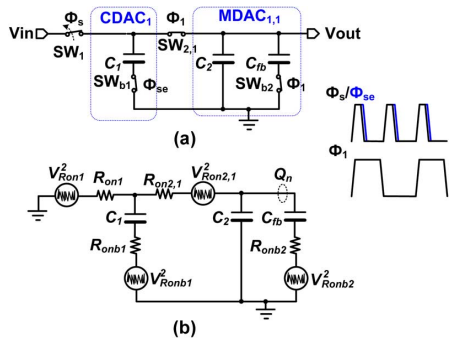


Fig. 4. S/H circuit with thermal noise sources.

The input-referred noise of the regenerative comparator is proven to have the kT/C-form [18], [19] and can be described by

$$N_{Cmp} = \frac{2kT\kappa\gamma}{C_{LC}}, \tag{5}$$

where γ is the thermal-noise factor (for a long-channel MOSFET in saturation, $\gamma = 2/3$, for a deep sub-micrometer MOSFET, $1 < \gamma < 2$ [20]), κ is an architecture-dependent parameter, and C_{LC} is the equivalent loading capacitance, whose minimum value C_{min} set by the minimum feature size is assumed to be 5 fF [21]. With $N_{Cmp} = K_2 N_Q$, the loading capacitance C_{LC} is derived as

$$C_{LC} = MAX\left(\frac{2kT\kappa\gamma}{K_2 N_Q},\ C_{min}\right). \tag{6}$$

In summary, the total noise power contribution in the TI-SAR ADC can be obtained by the summation of (2), (3), and (5)

$$\begin{aligned} N_{total} &= N_{Cs} + N_{Cmp} + N_Q \\ &= 2kT\left(\frac{1}{C_S} + \frac{\kappa\gamma}{C_{LC}}\right) + \frac{\Delta^2}{12}. \end{aligned} \tag{7}$$

Since the TI-SAR operation doesn't need residue amplification, the main analog circuitry is the comparator only. Next, the power dissipation in the comparator is discussed. The sampling frequency of each individual channel is f_S/j. It is assumed that the ratio of time allocation between sampling and n-bit conversion is 1:n, and the comparison time T_r occupies 1/4 of each bit cycling T_b. As the comparator is required to regenerate an input difference of $2^{-(n+1)}V_{FS}$ to V_{FS} within T_r, the time constant $\tau = C_{LC}/g_{m,Cmp}$, where $g_{m,Cmp}$ is the transconductance of the inverter in the latch stage, can be determined as

$$2^{-(n+1)}V_{FS} \cdot e^{\left(\frac{T_r}{\tau}\right)} = V_{FS}, \tag{8}$$

and thus $g_{m,Cmp}$ can be obtained as

$$g_{m,Cmp} = \frac{(n+1)\ln 2 \cdot C_{LC}}{T_r}. \tag{9}$$

I_D is defined as the minimum current drawn from V_{dd} to achieve the desired $g_{m,Cmp}$, which can be written as

$$I_D = g_{m,Cmp} V_{eff}, \tag{10}$$

where V_{eff} is the value that depends on the biasing condition and the inversion level [18], [22]. Accordingly, the energy dissipation per comparison during T_r will be

$$E_{Cmp} = g_{m,Cmp} V_{eff} V_{dd} T_r. \tag{11}$$

Since the conversion requires n comparison cycles, the average power of each individual channel is

$$P_{Cmp,ch} = \frac{n f_S E_{Cmp}}{j}. \tag{12}$$

Assuming $V_{dd} = V_{FS}$, the average power dissipation of the fully-differential comparator in the TI-SAR ADC P_{Cmp}, according to (6), (9), (11), and (12), can be obtained as

$$P_{Cmp} = 2n(n+1)\cdot \ln 2 \cdot f_S V_{eff} V_{FS} MAX\left(\frac{2kT\kappa\gamma}{K_2 N_Q},\ C_{min}\right). \tag{13}$$

By substituting (2) into (13), it can be observed that when $C_{LC} \neq C_{min}$, P_{Cmp} is proportional to 2^{2n}, which indicates that 1-bit accuracy improvement requires 4 × power consumption. The corresponding average power dissipation in the TI-SAR ADC has the comparator as its main contributor, as illustrated in (13).

B. PI PS ADC

The noise analysis of the PI PS ADC is more complex as its operation comprises multi-phases for conversion and residue amplification. As mentioned in Section II, the noise level of the 1st-stage comparator can be relaxed to $(m+1)$-bit due to DEC, which is easy to achieve. To simplify the analysis its noise contribution will be neglected in the following discussion. The analysis of the main noise sources, including the kT/C, the opamp and the comparator in the 2nd-stage, is presented. Normalizing these three noise portions to the quantization noise N_Q leads to $N_{Cs} = K_3 N_Q$, $N_{Op} = K_4 N_Q$ and $N_{Cmp2} = K_5 N_Q$.

Firstly, the noise performance will be investigated phase by phase under different noise sources. Fig. 3 shows the architecture of the m-bit 2 b/cycle SAR ADC with TI MDACs in the 1st-stage. Only the noise transfer in $\mathrm{CDAC_1}$ of Fig. 2 is analyzed, since the $\mathrm{CDAC_2}$ is used to assist the 2 b/cycle comparisons, and it is not involved in the residue amplification. Assuming two ADCs target the same kT/C noise, according to the PI operation, the sampling capacitance that contains the sum of the $\mathrm{CDAC_1}$ and the $\mathrm{MDAC_{1,1}}$ ($\mathrm{CDAC_1} = \mathrm{MDAC_{1,1}} = 1/2C_S$) in Fig. 2, is the same as the TI-SAR ADC. During the sampling phase ($\Phi_S = 1$ & $\Phi_1 = 1$), the input signal is sampled onto both top-plates of $\mathrm{CDAC_1}$ and $\mathrm{MDAC_{1,1}}$. The S/H circuit and its noise equivalent circuit are shown in Fig. 4. When the sampling switch $\mathrm{SW_1}$ is off, the noise charge Q_n on the top-plate of the three capacitors is frozen. Instead of using the noise transfer functions (NTFs), a simpler way to find out Q_n is to use thermal equilibrium from statistical mechanics [23], [24], which states that any energy storage element (or "degree of freedom") in the thermal equilibrium holds an average noise energy of kT/2. Thus the Q_n can be calculated as

$$\frac{1}{2}\frac{\overline{Q_n^2}}{(C_1 + C_2 + C_{fb})} = \frac{kT}{2} \Rightarrow \overline{Q_n^2} = kT(C_1 + C_2 + C_{fb}). \tag{14}$$

During the coarse conversion phase ($\Phi_S = 0$ & $\Phi_1 = 1$), the m-bit binary-searched approximation is performed in $\mathrm{CDAC_1}$, where the $\mathrm{MDAC_{1,1}}$ connected to $\mathrm{CDAC_1}$ serves as a reference divider [14]. Once the conversion is done, the residue is generated on both top-plates of $\mathrm{CDAC_1}$ and $\mathrm{MDAC_{1,1}}$. According to the PI operation, only the $\mathrm{MDAC_{1,1}}$ is involved in the residue amplification, while the $\mathrm{CDAC_1}$ connected to $\mathrm{MDAC_{1,2}}$ in Fig. 2 starts a new sampling. The noise charge sampled by $\mathrm{MDAC_{1,1}}$ is transferred and appears at the opamp's output. There is an intermediate phase between conversion and amplification phases, when the switch $\mathrm{SW_{2,1}}$ turns off ($\Phi_1 = 0$) to disconnect the $\mathrm{MDAC_{1,1}}$ to

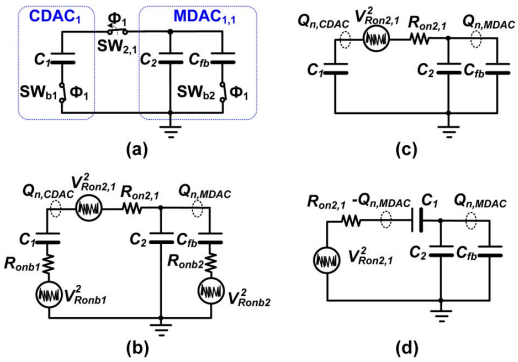


Fig. 5. Coarse conversion circuit model with thermal noise sources.

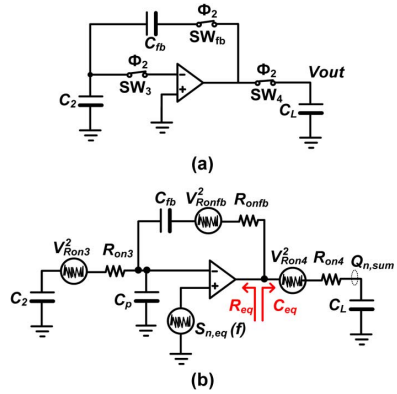


Fig. 6. Amplification circuit with thermal noise sources.

CDAC_1. Assuming zero noise contribution from the switch $\mathrm{SW}_{2,1}$ at the moment, the noise charge calculated from (14) are then separated into the CDAC_1 and $\mathrm{MDAC}_{1,1}$ according to the capacitor size, and the corresponding noise power of $\mathrm{MDAC}_{1,1}$ can be deduced as

$$N_{MDAC,1} = \frac{\overline{Q_n^2} \cdot \left(\frac{C_2+C_{fb}}{C_1+C_2+C_{fb}}\right)^2}{(C_2+C_{fb})^2} = \frac{kT}{C_1+C_2+C_{fb}}. \quad (15)$$

Now, the analysis of the noise contribution from the switch $\mathrm{SW}_{2,1}$ (Fig. 5) is proceeded by assuming zero noise contribution from the sampling phase Φ_S in Fig. 5. As both top-plates of CDAC_1 and $\mathrm{MDAC}_{1,1}$ in Fig. 5 are in high-impedance state, and the initial noise charge stored on them is zero before $\mathrm{SW}_{2,1}$ turns off, the total noise charge is constrained to 0 when $\mathrm{SW}_{2,1}$ turns off. As a result, CDAC_1 and $\mathrm{MDAC}_{1,1}$ hold the same amount of charge with opposite polarity,

$$Q_{n,MDAC} = -Q_{n,CDAC}, \quad (16)$$

where $Q_{n,MDAC}$ and $Q_{n,CDAC}$ correspond to the portions of the total noise charge distributed on $\mathrm{MDAC}_{1,1}$ and CDAC_1, respectively. As there is no noise injection from the noise sources of the bottom-plate switches SW_{b1} and SW_{b2} (since the top plates are in high-impedance state), the circuit model is simplified as shown in Fig. 5(c). Based on the Kirchhoff's voltage law (KVL), the equivalent circuit of Fig. 5(c) can be obtained as shown in Fig. 5(d). Obviously, CDAC_1 and $\mathrm{MDAC}_{1,1}$ are connected in series, and thus the noise charge $Q_{n,MDAC}$ can be derived as

$$\overline{Q_{n,MDAC}^2} = kT\frac{C_1(C_2+C_{fb})}{C_1+C_2+C_{fb}}, \quad (17)$$

accordingly, the corresponding noise power is equal to

$$N_{MDAC,2} = \frac{\overline{Q_{n,MDAC}^2}}{(C_2+C_{fb})^2} = kT\frac{C_1}{(C_1+C_2+C_{fb})(C_2+C_{fb})}. \quad (18)$$

As the noises generated from SW_1 and $\mathrm{SW}_{2,1}$ are uncorrelated, the total sampling noise power in the differential circuit doubles the sum of (15) and (18),

$$N_{Cs} = 2(N_{MDAC,1}+N_{MDAC,2}) = \frac{2kT}{C_2+C_{fb}} = \frac{4kT}{C_S}. \quad (19)$$

The same result can be obtained by using the thermal equilibrium directly on the final resulting top-plate of $\mathrm{MDAC}_{1,1}$ of Fig. 5(b). From the observation, the sampling noise can be suppressed by increasing the capacitance of C_2 and C_{fb}.

On the amplification phase ($\Phi_2 = 1$), the $\mathrm{MDAC}_{1,1}$ serves as a flip-around MDAC, which feeds back C_{fb} to the output of the opamp for $\times 2^{\mathrm{i}}$ residue amplification. All the noise charge stored on the capacitance C_2 and C_{fb} is transferred to C_{fb}. With $C_2 + C_{fb} = C_S/2$, and $C_{fb} = 2^{-(i+1)}C_S$ as indicated in Fig. 3, the total output sampling noise power is,

$$N_{out,Cs} = N_{Cs}\left(\frac{C_2+C_{fb}}{C_{fb}}\right)^2 = \frac{2^{2(i+1)}kT}{C_S}. \quad (20)$$

Fig. 6 indicates the circuit model with noise sources during Φ_2. Assuming that three switches SW_3, $\mathrm{SW}_{\mathrm{fb}}$ and SW_4 are designed sufficiently large, in order that the amplification bandwidth is dominated by the opamp, which is a usual design practice. Therefore, the circuit is treated as a single-pole RC network with the corner frequency $f_c = 1/2\pi R_{eq}C_{eq}$ defined by

$$R_{eq} = \frac{1}{\beta g_{m1}}, \quad (21)$$

$$C_{eq} = C_{fb}//(C_2+C_p)+C_L, \quad (22)$$

where $\beta = C_{fb}/(C_2+C_p+C_{fb})$ is the feedback factor of the amplification stage,which approximates $1/2^{\mathrm{i}}$ when the open-loop DC gain of the opamp is sufficiently large. C_p and C_L are the input parasitic capacitance and loading capacitance, respectively.

For a single-stage operational transconductance amplifier, the power-spectral-density (PSD) of the total input-referred noise can be deduced as

$$S_{n,eq}(f) = \frac{4kT\gamma}{g_{m1}}n_f$$
$$n_f = 1+g_{m2}/g_{m1}, \quad (23)$$

where g_{m1} and g_{m2} are the transconductances of the input pair and the current source load, respectively. If $g_{m1} \gg g_{m2}$ that implies the opamp noise has the input pair as its main contributor, the value of n_f will be close to 1. The input-referred noise is shaped by the close-loop bandwidth, giving rise to the output opamp noise power of

$$N_{out,Op} = \int_0^\infty S_{n,eq}(f)\cdot 2^{2i}\cdot\left|\frac{1}{1+j2\pi f R_{eq}C_{eq}}\right|^2 df = \frac{2^{\mathrm{i}}kT\gamma n_f}{C_{eq}}. \quad (24)$$

Note that the total opamp noise power is not a function of g_{m1} since the noise bandwidth is proportional to g_{m1}, while PSD is inversely proportional to g_{m1}. Besides, the noises from the on-resistances of SW_3 (R_{on3}) and $\mathrm{SW}_{\mathrm{fb}}$ (R_{onfb}) are amplified by C_2/C_{fb} and 1, respectively, and both of them are band-limited by $\pi f_c/2$. Thus, their noise contributions to the sampled output can be derived as

$$N_{out,sw3} = \int_0^\infty 4kTR_{on3}\cdot\left(\frac{C_2}{C_{fb}}\right)^2\left|\frac{1}{1+j2\pi f R_{eq}C_{eq}}\right|^2 df$$
$$= \frac{(2^i-1)^2}{2^i}\cdot\frac{kTg_{m1}R_{on3}}{C_{eq}}, \quad (25)$$

$$N_{out,swfb} = \int_0^\infty 4kTR_{onfb} \cdot \left| \frac{1}{1+j2\pi fR_{eq}C_{eq}} \right|^2 df = \frac{1}{2^i} \cdot \frac{kTg_{m1}R_{onfb}}{C_{eq}}. \quad (26)$$

Due to the fact that the on-resistances of the switches (R_{on3} and R_{onfb}) are usually designed much smaller than $(1/g_{m1})$, the terms of $N_{out,sw3}$ and $N_{out,swfb}$ are much smaller than $N_{out,Op}$. Also, the switch SW_4 has negligible noise contribution since its noise power is divided by 2^{2i} when referring to the ADC's input. Therefore, the output noise power on the amplification phase approximates $N_{out,Op}$. Referring $N_{out,Op}$ to the ADC's input gives

$$N_{Op} = 2^{(1-2i)}N_{out,Op}, \quad (27)$$

with the presumption that $N_{Op} = K_4N_Q$, the value of C_{eq} can be calculated as

$$C_{eq} = \frac{2^{1-i}kT\gamma n_f}{K_4N_Q}. \quad (28)$$

The input-referred noise from the 2nd-stage comparator can be derived similarly as the analysis in the previous Section III-A, i.e.

$$N_{Cmp2} = \frac{2^{1-2i}kT\kappa\gamma}{C_{LC2}}, \quad (29)$$

where the loading capacitance C_{LC2} of the 2nd-stage comparator can be calculated with the noise budget $N_{Cmp2} = K_5N_Q$,

$$C_{LC2} = MAX\left(\frac{2^{1-2i}kT\kappa\gamma}{K_5N_Q},\ C_{min}\right). \quad (30)$$

Consequently, the total input-referred noise can be obtained by the summation of (19), (27), and (29),

$$N_{total} = N_{Cs} + N_{Op} + N_{Cmp2} + N_Q = 2kT\left(\frac{2}{C_S} + \frac{\gamma n_f \cdot 2^{-i}}{C_{eq}} + \frac{\kappa\gamma \cdot 2^{-2i}}{C_{LC2}}\right) + \frac{\Delta^2}{12}. \quad (31)$$

By comparing the total input-referred noise power of the two ADC architectures obtained from (7) and (31), it can be concluded that due to the PI operation the PI PS ADC draws twice of the sampling noise power than the TI-SAR ADC. Also, the use of the opamp induces extra noise into the conversion, while it can relax the noise and accuracy requirements of the 2nd-stage comparator, leading to power reduction of the 2nd-stage comparator.

Secondly, the power budgets for the opamp and comparators in each stage are derived. The m-bit residue generated from the 1st-stage is amplified by 2^{i} times to the next stage, leading to the full-scale of the input signal for the 2nd-stage of $2^{-(m-i)}V_{FS}$. Since 1-bit DEC is considered, the conversion full-scale for the 2nd-stage is $2^{-(m-i-1)}V_{FS}$. As the 2nd-stage resolves $(\mathrm{n}-\mathrm{m}+1)$-bit, the $\mathrm{LSB_{2nd}}$ of the 2nd-stage is equal to $2^{-(n-i)}V_{FS}$. The maximum output voltage error induced by the gain error ε is required to be less than $1/2$ $\mathrm{LSB_{2nd}}$, and the gain error ε should be suppressed less than

$$2^{-(m-i)}V_{FS}|\varepsilon| < 2^{-(n-i+1)}V_{FS} \Rightarrow |\varepsilon| < 2^{-(n-m+1)}. \quad (32)$$

According to the timing diagram in Fig. 2, the amplification time is set to be $1/f_S$. Assuming it is equally divided into two parts: the slew time T_{sl} and linear settling time T_{se}, the settling error thus can be represented as $e^{-1/(2f_S\cdot\tau)}$, where $\tau = C_{eq}/\beta g_{m1}$ is the time constant of the opamp. According to (32), the current for linear settling I_{se} should be at least

$$I_{se} = g_{m1}V_{eff} = \frac{2^iC_{eq}V_{eff}\ln 2\cdot(n-m+1)}{T_{se}}. \quad (33)$$

Moreover, the current required to charge C_{eq} to a signal full-scale of $2^{-(m-i)}V_{FS}$ during T_{sl} can be calculated as,

$$I_{sl} = \frac{2^{-(m-i)}C_{eq}V_{FS}}{T_{sl}}. \quad (34)$$

Finally, according to (28), (33), and (34) the power consumption of the opamp is represented as

$$P_{Op} = 2(I_{se}+I_{sl})V_{FS} = \frac{8kT\gamma n_f f_S V_{FS}^2}{K_4N_Q}\left(\frac{V_{eff}}{V_{FS}}(n-m+1)\cdot\ln 2 + \frac{1}{2^m}\right). \quad (35)$$

As the 1st-stage performs a 2 b/cycle conversion, it requires three comparators to operate synchronously with $(\mathrm{m}+1)$-bit accuracy. If the regeneration time for each comparator is T_{r1}, the total average power dissipation from the three comparators in the 1st-stage, derived similarly as (8)–(13), will be

$$P_{Cmp1} = 3m(m+1)\cdot\ln 2\cdot f_S V_{eff}V_{FS} \times MAX\left(\frac{8\cdot 2^{2(m-n)}kT\kappa\gamma}{N_Q},\ C_{min}\right). \quad (36)$$

The conversion accuracy for the comparators in the 2nd-stage is $(\mathrm{n}-\mathrm{i}+1)$-bit, and two TI-SAR channels are implemented according to the timing sequence shown in Fig. 2, which leads to its total average power consumption that is

$$P_{Cmp2} = 2(n-m+1)(n-i+1)\cdot\ln 2 \cdot f_S V_{eff}V_{FS}MAX\left(\frac{2^{1-2i}kT\kappa\gamma}{K_5N_Q},\ C_{min}\right). \quad (37)$$

Consequently, the total average power from the opamp and comparators in PI PS ADC can be obtained by combining (35), (36), and (37) leading to

$$\begin{aligned} P_{total} &= P_{Op}+P_{Cmp1}+P_{Cmp2} \\ &= f_S V_{FS} \times \left[\frac{8kT\gamma n_f V_{FS}}{K_4N_Q}\left(\frac{V_{eff}}{V_{FS}}(n-m+1)\cdot\ln 2+\frac{1}{2^m}\right)\right. \\ &\quad + V_{eff}\ln 2\left(3m(m+1)MAX\left(\frac{8\cdot 2^{2(m-n)}kT\kappa\gamma}{N_Q},\ C_{min}\right)\right. \\ &\quad \left.\left. +2(n-m+1)(n-i+1) \times MAX\left(\frac{2^{1-2i}kT\kappa\gamma}{K_5N_Q},\ C_{min}\right)\right)\right]. \end{aligned} \quad (38)$$

C. Power Comparison of Two ADCs

This subsection provides the power optimization of PI PS ADC under different stage gains and number of bits allocation in each stage. Also, the power comparison of the TI-SAR and PI PS ADCs under the same noise budget and operation frequency will be illustrated. As the existing work of a PI PS ADC achieved the sampling frequency of 500 MS/s with 10-bit resolution [14], the two design examples referred here target the same specifications. The 10-bit single channel SAR can achieve a sampling frequency near 100 MS/s [25], [26], therefore, the number of channels of the TI-SAR ADC is set to be 5. The power comparison between TI-SAR and PI PS ADCs is based on the assumption that the same sampling capacitance and total input-referred noise budget are considered. The coefficients K_1 and K_2 in the TI-SAR ADC are assigned to be 1 and 3/2, respectively, which results in a total noise budget of $7/2N_Q$ corresponding to 5.4 dB SNR loss. Accordingly, in the PI PS ADC K_3 equals to $2K_1$ (according to (7) & (31)), and the noise contributions from the opamp and the 2nd-stage comparator are equally distributed as $K_4 = K_5 = 1/4$.

Fig. 7 illustrates the power dissipations of the PI PS ADC under different stage gains and number of bit allocations between two

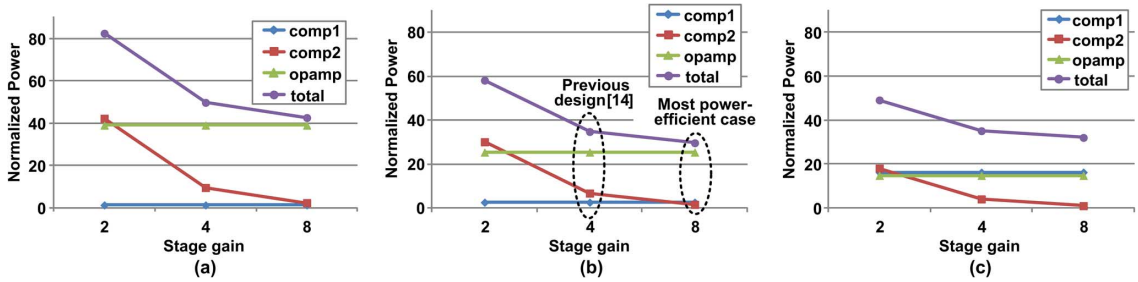


Fig. 7. Normalized power of 10-bit 500 MS/s PI PS ADC with different stage gains and number of bit allocations. (a) $m = 4$, $n - m + 1 = 7$; (b) $m = 6$, $n - m + 1 = 5$; (c) $m = 8$, $n - m + 1 = 3$.

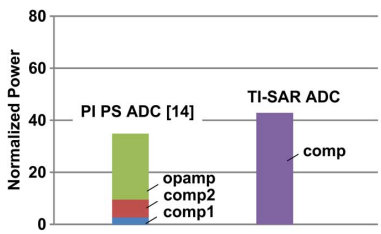


Fig. 8. Comparison of power dissipations between 10-bit 500 MS/s TI-SAR and PI PS ADCs.

stages, which are plotted according to the theoretical models in (13) and (38) (Some variables are set to be $\gamma = 1$, $n_f = 1$, $\kappa = 1$, $V_{FS} = 1.2$ V and $V_{eff} = 100$ mV [18]). In Fig. 7(a) and (b) the power dissipation is mainly dominated by the opamp. The opamp power consumption remains constant under different stage gains, since the equivalent loading capacitance C_{eq} set by the opamp noise is relaxed by the stage gain as indicated in (28). Further, unlike the pipeline ADC, the pipelined-SAR structure quantizes larger number of bits in the sub-stage. If C_{eq} is constrained by the achievable minimum unit capacitance [10] in the DAC, the power drawn from the opamp will rise linearly with the stage gain [3]. With a stage gain of 2 the 2nd-stage comparator consumes even larger power than the opamp. The power consumed in the 2nd-stage comparator is reduced exponentially as the stage gain increases. Comparing Fig. 7(a), (b), and (c) when the number of bits in the 1st-stage increases, the opamp's power dissipation scales down accordingly due to the reduction of both the gain accuracy and the output swing. In [14] the stage gain is set to be 4, and the bit allocation in the 1st- and 2nd-stage is 6:5, which is a comparatively power-optimized combination as illustrated in Fig. 7. The power dissipation of this PI PS ADC is compared with the 5 × TI-SAR ADC, where the power breakdown is plotted in Fig. 8. It can be seen that targeting for the same conversion accuracy and speed, the PI PS ADC is more power efficient than the TI-SAR ADC, where the total power consumed in the PI PS ADC is 20% less than in its counterpart.

IV. Reference Error Caused by Switching Transient

The SAR ADC relies on the CDAC to perform the binary-search feedback. When the capacitors in most significant bits (MSBs) are charged or discharged according to the switching nature, it causes large current-induced reference ripples degrading the conversion accuracy. The high-resolution SAR ADC has a stringent requirement for the precision of the reference voltages. For a low-speed SAR ADC the reference error due to switching transient is not problematic, as the SAR loop provides sufficient settling time for the DAC and references. However, this problem is critical in high-speed design, as the time spared for the reference recovery is limited. The reference errors become more significant in ADCs using the TI scheme such as TI-SAR and PI PS architectures, where the multi-channels share the same reference source and operate simultaneously. The conversion in each channel interacts via the reference source, finally leading to signal-dependent errors that are difficult to be calibrated.

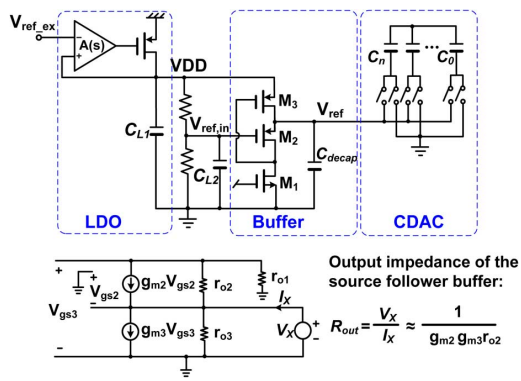


Fig. 9. Reference voltage generation network.

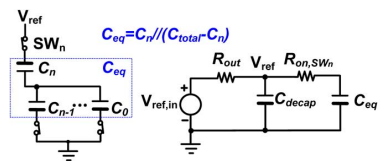


Fig. 10. Equivalent RC model of the reference network.

In practice, the analog circuitry is normally biased through a low noise and low dropout (LDO) supply voltage provided by a LDO regulator to isolate the large system digital noise. Fig. 9 shows the block diagram of the reference generation network for the CDAC. The LDO [27] delivers a low noise supply, which is used to generate the desired reference level $V_{ref,in}$ to the reference buffer. The buffer is built with the flipped voltage follower (FVF) topology to provide sufficiently low output impedance R_{out} for high-speed drive [28]. A decoupling capacitor C_{decap} of 3 pF is placed on the output node to suppress the noise, occupying a small die area close to 240 μm^2. It is assumed that the power supply rejection ratio (PSRR) and transient response of the LDO achieve sufficient accuracy, as referred in the following discussion. Fig. 10 shows the equivalent RC model when the MSB capacitor is charged by the reference voltage, which will also be used next.

A. Reference Errors in the Single Channel SAR ADC

The above reference generator is applied to the 10-bit 100 MS/s single channel SAR ADC with the same configuration as mentioned previously. The SAR ADC is built with a 9-bit binary-weighted capacitive DAC (CDAC) with V_{cm}-based switching [26]. The sampling capacitance of 700 fF is used, which is the same of the PI PS SAR ADC [14]. Assuming that the settling speed of each bit cycling is mainly dominated by the time constant $\tau = R_{out}C_{decap}$ of the reference buffer, the on-resistance of the switch connected to the bottom-plate of the DAC is designed to be sufficiently low, whose size scales down according to the ratio of the binary-weighted array.

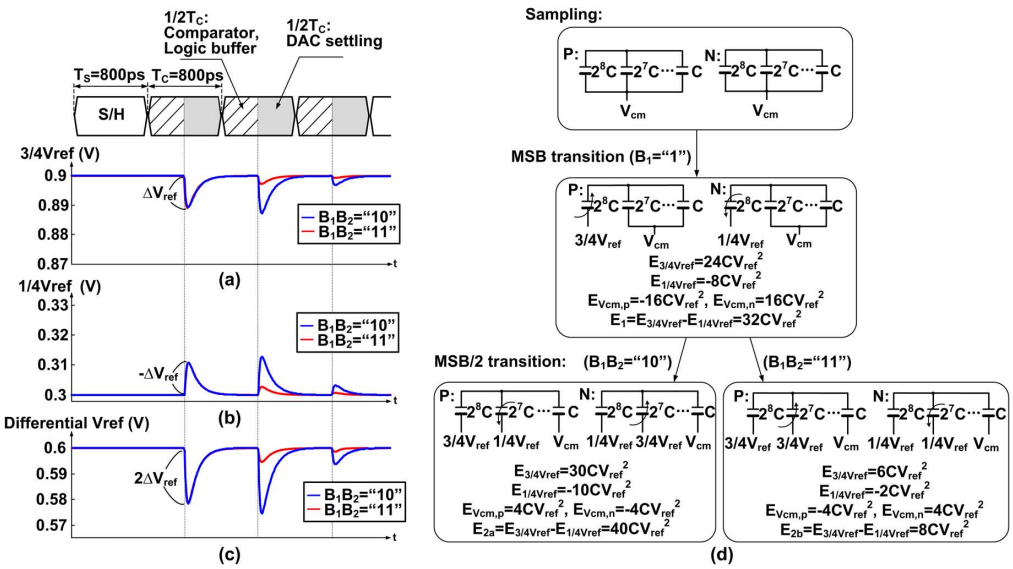


Fig. 11. 10-bit SAR ADC conversion with the switching energy and ΔV_{ref} variations in the first two bit transitions.

Fig. 11 shows the switching procedure and timing slot of the MSB and MSB/2 transitions. As the V_{FS} is 1.2 V_{p-p}, two corresponding reference levels ($3/4V_{ref}$ and $1/4V_{ref}$) of 900 mV and 300 mV are required. According to the timing allocation discussed in Section III, it is assumed that the sampling period is 800 ps, and it takes 8 ns to complete 10 conversion cycles. Accordingly, each bit cycling takes 800 ps for comparison, logic processing and DAC settling, where half of it is assigned for the first two terms. Therefore, the time spared for DAC settling is 400 ps.

According to the nature of the V_{cm}-based switching, once the decision is made, the MSBs in the two differential DACs are switched to $3/4V_{ref}$ and $1/4V_{ref}$, respectively, while the rest bits continue connected to V_{cm}. The reference ripple and the corresponding switching energy due to the MSB transition are illustrated in Fig. 11. Both charging and discharging the MSBs cause reference ripples, where the reference variations ΔV_{ref} from $3/4V_{ref}$ and $1/4V_{ref}$ exhibit the same amplitude with opposite polarity. Since the DAC operates differentially, the overall reference drop will be $2\Delta V_{ref}$. The switching energy drawn from $3/4V_{ref}$ and $1/4V_{ref}$ is $24CV_{ref}^2$ and $-8CV_{ref}^2$, respectively, which corresponds to a total switching energy of $32CV_{ref}^2$. Moreover, the energy drawn from V_{cm} is cancelled out differentially, therefore, the conversion is insensitive to V_{cm} variation. As charging or discharging the MSB in either of the DACs (B_1 = "0" or "1") consumes the same switching energy of $32CV_{ref}^2$, the reference error at the MSB transition is signal-independent. However, the reference ripple at the MSB/2 transition is code-dependent. From Fig. 11, when the first two bit decisions are B_1B_2 = "10," the MSB/2 in DAC_P and DAC_N are charged to $1/4V_{ref}$ and $3/4V_{ref}$, respectively, consuming switching energy of $40CV_{ref}^2$, while the complementary switching operation performed when B_1B_2 = "11" consumes switching energy of only $8CV_{ref}^2$. Correspondingly, the amplitude of the reference ripple at the MSB/2 transition is signal-dependent and the worst case happens when the first two bits are switched to a complementary logic decision (B_1B_2 = "10" or "01"), as shown in Fig. 11. Fig. 12 shows the switching power consumption in the SAR ADC versus each bit cycle. The consumed switching energy for each bit cycling is code-dependent, which reduces gradually as a less number of units are charged or discharged. Therefore, the reference ripples are much smaller during the LSBs' transitions.

To guarantee 10-bit conversion accuracy, the reference error ΔV_{ref} appearing at the DAC's output voltage error $|V_{err}|$ must be less than LSB/2 for each bit comparison, which can be represented as,

$$|V_{err}| = \frac{C_{ref}}{C_{sum}} \cdot \Delta V_{ref} \leq \frac{\Delta}{2} = 586\ \mu\text{V}, \tag{39}$$

where C_{sum} and C_{ref} are the total capacitance of the CDAC and the capacitors connecting to the reference voltage, respectively. As the maximum ΔV_{ref} happens at the MSB/2 transition when B_1B_2 = "10" or "01" and the transient response of the reference buffer depends on the time constant $\tau = R_{out}C_{decap}$, the value of R_{out} should be set properly to tolerate the settling error in the worst case. Fig. 13 plots the sweep of R_{out} versus the voltage error $|V_{err}|$ in the first two bit transitions. By choosing a R_{out} of 30 Ω, the settling error is controlled within the tolerance range of the ADC. Thus, considering the reference error only, and the circuit is otherwise ideal, the single channel SAR ADC can achieve a SNDR of 62 dB. Based on this settling condition, the reference errors in the TI-SAR ADC and the PI PS ADC will be further discussed.

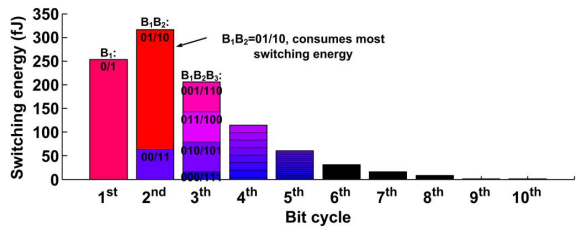


Fig. 12. Switching energy versus code in each bit-cycle of the SAR ADC.

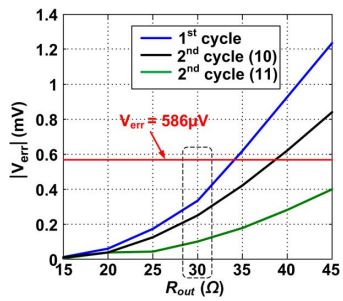


Fig. 13. Equivalent output impedance R_{out} versus top-plate voltage settling error $|V_{err}|$ in the first two bit transitions.

B. Reference Errors in the TI-SAR ADC

Based on the model of the reference generation discussed previously, which satisfies the settling accuracy requirement for the single channel SAR ADC, this sub-section quantitatively analyzes the conversion error due to the reference ripple in the 5 × TI-SAR ADC. The timing diagram of the TI-SAR ADC is shown in Fig. 14, where the time allocation for sampling and bit cycling in each channel follows the single channel SAR ADC as aforementioned. Accordingly, as illustrated in Fig. 14, when Ch.1 performs the MSB/2 transition (B_1B_2 = "10" or "01"), the reference ripple disturbs the comparison in Ch.3 and Ch.5, which are in the former half period of the bit cycling performing the comparison and logic processing. However, the operations in Ch.2 and Ch.4 are not influenced by the reference error, as Ch.2 is sampling the input signal and all the DACs are reset to *Gnd*, which is reference-independent. Also, Ch.4 in the later half period of the bit cycling is performing the 7th bit transition simultaneously. Therefore, only Ch.3 and Ch.5 suffer large residue errors ($|V_{err}| \gg 1/2$ LSB) at the end of the conversion. The largest quantization error in Ch.5 can go up to 4 LSB, as the 5th bit (B_5) rather than the 10th bit (B_{10}) in Ch.3 is determined. Moreover, the residue error V_{err} is signal-dependent. It results in a maximum V_{err} when the decisions of the 4 MSB bits ($B_1 - B_4$) of the fine conversion are "1111", as the largest number of bit capacitance ($\approx 93\%C_{sum}$) is connected to $+V_{ref}$. According to Fig. 14, the largest voltage drop of the reference $\Delta V_{ref,max}$ is 22.75 mV, which results in a residue error V_{err} of 17 mV for the comparison in Ch.5. The wrong decision ultimately leads to a 4 LSB quantization error at the digital output. The possible solution to alleviate the reference cross talk among the TI-SAR ADC would be to use an individual reference buffer in each channel. However, the ADC will be subjected to extra power dissipation as well as conversion error due to the reference mismatches.

C. Reference Errors in the PI PS ADC

In the PI PS ADC, the 1st-stage is implemented with a 2 b/cycle SAR for high-speed. Conventionally, to perform 2 b/cycle 3 DAC arrays are required to generate additional reference levels for 2 b comparison in each cycle. By using interpolation [29] as shown in Fig. 2, the number of the CDACs is reduced to two ($CDAC_1$ & $CDAC_2$). The $CDAC_1$ contains the same total sampling capacitance of 700 fF as TI-SAR ADC, and the total capacitance in the 2nd-stage CDAC is 176 fF, which is sufficient for the noise requirement in the 2nd-stage. Fig. 15 details the timing diagram of the 1st- and 2nd-stage SAR operations, where the same sampling time of 800 ps is set as the TI-SAR ADC, and each bit cycling in the 1st- and 2nd-stages is assigned to be 350 ps and 400 ps, respectively, where half of the bit cycling is spared for the DAC settling. During sampling, the input V_{in} is sampled onto the two CDACs in the 1st-stage, where the bottom-plates are all reset to *Gnd*. The first two bits are determined by comparing V_{in} with three reference levels: $\pm 1/4V_{FS}$ and *Gnd* via 3 comparators. Once the sampling is completed, the $CDAC_1$ and $CDAC_2$ generate two complementary reference levels by switching the MSB capacitor to $-V_{ref}$ and $+V_{ref}$, respectively. The corresponding switch logics are listed in the table of Fig. 15. For example, if $V_{in} > 1/4V_{FS}$, the determination of the first two bits B_1B_2 will be "11," the first two MSBs (C_{MSB} and the $C_{MSB/2}$) in $CDAC_1$ and $CDAC_2$ are both charged to $+V_{ref}$, resulting in the DAC output of $(V_{in} - 3/8V_{ref})$. Fig. 15 illustrates the worst case that causes the largest reference ripple when B_1B_2 = "01." Based on the logic, 12.5% of the total capacitance is discharged to $-V_{ref}$, thus the $C_{MSB/2}$ in $CDAC_1$ and C_{MSB}, $C_{MSB/2}$ in $CDAC_2$ are charged or discharged, accordingly. This leads to the largest reference ripple ($\Delta V_{ref,max} = -176$ mV) equivalent to 9 mV error at the DAC output. Since the 1st-stage resolves the coarse 6 b, the tolerable residue error is less than 9.3 mV (i.e. $1.2/2^7$). Therefore, the largest residue error in the 1st-stage conversion is acceptable.

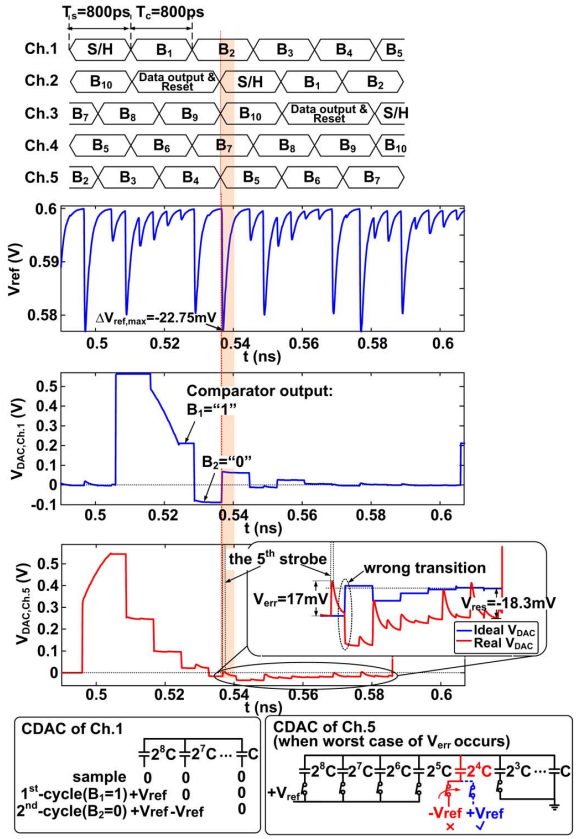


Fig. 14. The worst case of reference ripples in the TI-SAR ADC.

With the stage-gain of 4 and 1 bit overlapping, the reference voltage for the 2nd-stage SAR ADC is $\pm 1/16V_{FS}$ which is obtained by using a 5-bit split-DAC to scale down the reference voltage by 16 as shown in Fig. 15. In this way, two stages can share the same reference voltage to save extra power dissipation on the reference generator [3]. However, since two stages perform the conversion in a pipeline fashion, the reference ripples due to switch transient in the 1st-stage potentially affect the conversion accuracy of the 2nd-stage. Fig. 15 details the worst case of this effect. When the largest reference error occurs, the 2nd-stage SAR ADC in Ch.1 is performing the 4th-bit comparison (B_4). Similarly, the worst case of residue error happens when the first 3 MSBs ($B_1B_2B_3$) of the fine conversion are "111" (maximum capacitance $\approx 88\%C_{sum}$ is connected to $+V_{ref}$), which leads to a 9 mV DAC voltage deviation from the ideal value at the 2nd-stage DAC's output. Correspondingly, it finally results in a 2 LSB input-referred quantization error, which is smaller than in the TI-SAR ADC.

V. Simulation Results

The above thermal-noise analysis is validated by transient noise simulations in Cadence using a 65 nm CMOS technology. Two 10-bit 500 MS/s ADCs built with 5 × TI-SAR and PI PS architectures are demonstrated, where the control logic and comparator are ideal and the ADC is otherwise all transistor-level. The simulation results are obtained under typical-typical (TT) corner with the temperature of 27°C. In the TI-SAR ADC, the simulated kT/C noise with the sampling capacitance of 700 fF is 112 μV_{rms}, which closely matches the result of 109 μV_{rms} from (3). For the PI PS ADC, the simulated sampling noise voltage V_{MDAC} is 154 μV_{rms}, which also matches with the calculation result of 153 μV_{rms} based on (19).

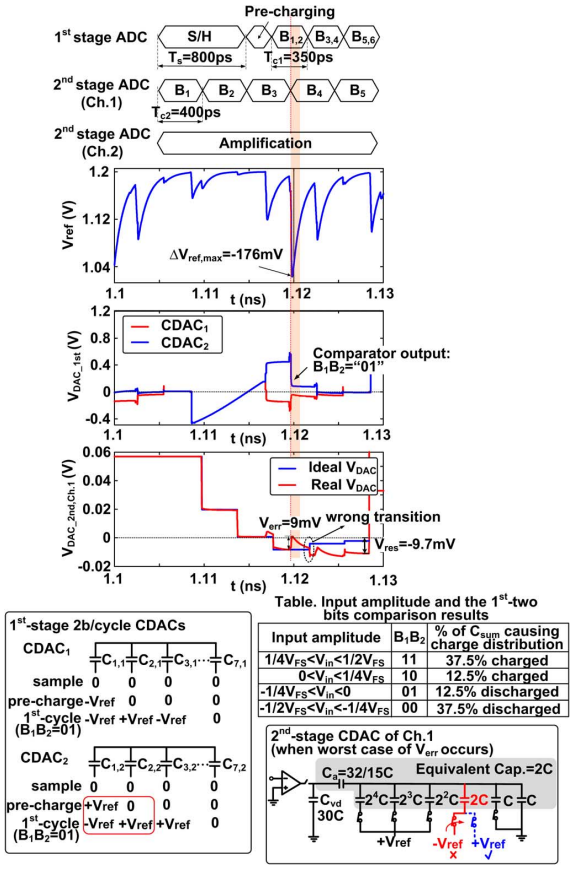
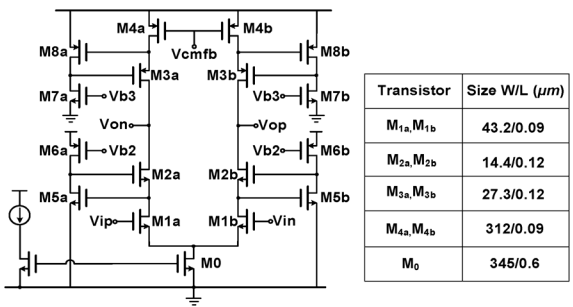


Table. Input amplitude and the 1st-two bits comparison results

Input amplitude	B_1B_2	% of C_{sum} causing charge distribution
$1/4V_{FS}<V_{in}<1/2V_{FS}$	11	37.5% charged
$0<V_{in}<1/4V_{FS}$	10	12.5% charged
$-1/4V_{FS}<V_{in}<0$	01	12.5% discharged
$-1/2V_{FS}<V_{in}<-1/4V_{FS}$	00	37.5% discharged

Fig. 15. The worst case of reference ripples in the PI PS ADC.



Transistor	Size W/L (μm)
M_{1a},M_{1b}	43.2/0.09
M_{2a},M_{2b}	14.4/0.12
M_{3a},M_{3b}	27.3/0.12
M_{4a},M_{4b}	312/0.09
M_0	345/0.6

Fig. 16. Opamp circuit schematic.

TABLE I
CALCULATED AND SIMULATED OUTPUT-REFERRED NOISE VOLTAGES IN THE PI PS ADC (NUMBERS ARE IN μV_{rms})

	Output-referred sampling noise voltage $V_{out,Cs}$	Output-referred Amplification noise voltage $V_{out,Op}$	Total noise voltage $V_{out,total}$
Calculation	613	634	883
Transient noise Sim.	616	642	890

The PI PS ADC contains additional noise from the opamp. With 6 b resolution at the 1st-stage and a stage-gain of 4, a maximum output voltage error in the 2nd-stage induced by the gain error ε is required to be less than half LSB of the 2nd-stage ADC, thus the acceptable gain error ε is calculated as

$$\frac{V_{FS}}{2^6}\cdot 4\cdot\varepsilon<\frac{V_{FS}}{8}\cdot\frac{1}{2^6}\Rightarrow\varepsilon<\frac{1}{2^5}. \tag{40}$$

Thus the open-loop gain A should be larger than 42 dB ($A=2^5/\beta$, $\beta=1/4$). Also, the linear settling time for the opamp T_{se} is

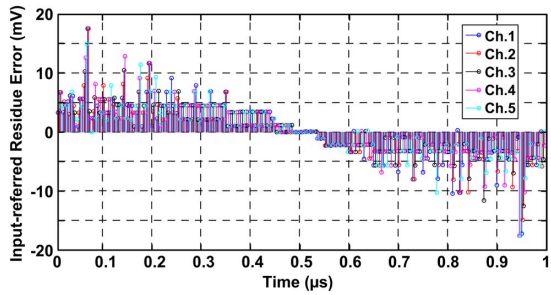


Fig. 17. Input-referred residue error of the TI-SAR ADC with a ramp input from $-V_{ref}$ to $+V_{ref}$.

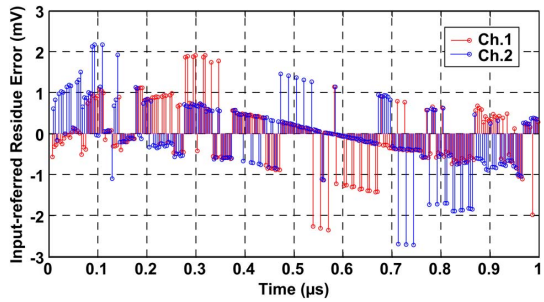


Fig. 18. Input-referred residue error of the PI PS ADC with a ramp input from $-V_{ref}$ to $+V_{ref}$.

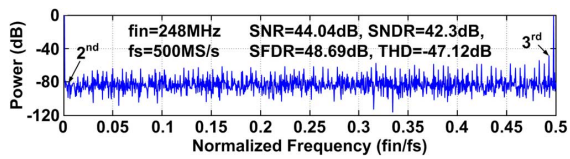


Fig. 19. Simulated ADC output spectrum of TI-SAR ADC with reference noise.

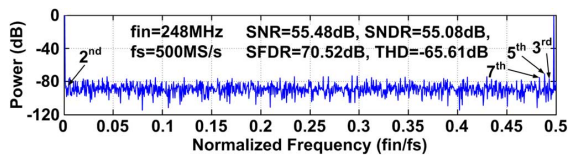


Fig. 20. Simulated ADC output spectrum of PI PS ADC with reference noise.

assigned to be half of the amplification period (i.e., 1 ns), the time constant τ can be derived as

$$e^{\frac{-T_{se}}{\tau}}<\frac{1}{2^5}, \tag{41}$$

where $\tau=R_{eq}C_{eq}=C_{eq}/g_{m1}\beta$. As aforementioned, the flip-around MDAC has a total capacitance of 350 fF, in which the feedback capacitance is 87.5 fF. Together with the loading capacitance C_L of 176 fF, the C_{eq} is equal to 242 fF, thus the minimum g_{m1} can be derived as

$$g_{m1}=\frac{5\ln 2\times C_{eq}}{\beta T_{se}}=3.4\ \text{mS}. \tag{42}$$

The opamp is designed with a gain-boosted telescopic topology [14], which achieves an open-loop gain of 68 dB and a GBW of 1.7 GHz (Fig. 16). The main noise sources in the opamp are the input pair M_{1a}/M_{1b} and the current source M_{4a}/M_{4b} with the corresponding transconductance $g_{m1}=g_{m4}=5$ mS, leading to $n_f=2$. By selecting the thermal-noise factor $\gamma=1.5$, the opamp noise power can be calculated based on (24). The calculated and simulated noise contributions from different phases in the PI PS ADC are summarized in Table I. The total output-referred noise voltage

TABLE II
SIMULATION RESULTS OF THERMAL AND REFERENCE NOISES IN TWO ADC ARCHITECTURES

	TI-SAR ADC	PI PS ADC
Input-referred thermal noise (μV_{rms})	154	227
Input-referred reference noise (mV)	17	2.3

$V_{out,total}$ is obtained by summing the noise voltage from both sampling phase $V_{out,Cs}$ and amplification phase $V_{out,Op}$ on the opamp's output node according to (20) and (24). It is shown that the above noise estimations match with the simulation results. The total noise voltage $V_{out,total}$ referred to the ADC input is 227 $\mu\mathrm{V_{rms}}$, corresponding to a SNR of 60.35 dB.

To demonstrate both the static and the dynamic errors in the overall ADC's performance due to the reference noise, the ADCs, including the equivalent RC model of the reference network shown in Fig. 10, are implemented. Also, to eliminate the other circuit non-idealities, except for the switches connected to the reference voltages, the sampling network, comparator, SAR logic and opamp are all ideal. The input-referred residue errors after 10 bit quantization of the two ADCs are illustrated in Figs. 17 and 18, respectively. The maximum residue error in the TI-SAR ADC (Fig. 17) can go up to ± 17 mV. However, benefitting from the stage-gain of 4 the PI PS ADC (Fig. 18) has much higher immunity to the reference error. Therefore, its maximum input-referred residue error is less than ± 3 mV. The dynamic performances of the two ADCs are illustrated in Figs. 19 and 20, respectively. The sampling total harmonic distortion (THD) at Nyquist input frequency is -90 dB in both designs. It is observed from Fig. 19 that the reference errors in the TI-SAR ADC give rise to odd harmonics and the spurs spread over the spectrum, which limits the SNDR to 42.3 dB. The SFDR is 48.69 dB that is dominated by the 3rd harmonic. While in the PI PS ADC the spurs due to reference errors in Fig. 20 are much lower than those in Fig. 19, the achieved SNDR and SFDR are improved by 13 dB and 22 dB, respectively, which reveals the advantage of the PI PS architecture. Table II summarizes the thermal and reference noise performances of the two ADC architectures.

VI. CONCLUSIONS

Thermal and reference noises in TI-SAR and PI PS ADCs have been analyzed and verified in two 10 b 500 MS/s design examples. The derived closed-form expressions lead to a complete and accurate thermal-noise estimation which match with the transistor-level simulations. It is shown that in the TI-SAR ADC, the comparator is a critical noise source, whose noise is required to be sufficiently low at the cost of spending large power. While in the PI PS ADC, the sampling noise, due to the reduction of the amplification capacitance, becomes one of the dominant factors in the overall noise performance. Moreover, as an additional noise source, the opamp also contributes with a significant portion to the system's noise, while it can greatly relax the noise requirement of the comparator in the sub-stage, thus leading to better power efficiency. On the other hand, the simulations of the reference noise demonstrate that the PI PS architecture, benefitting from the stage-gain, is >5 times less sensitive to the reference variation than the TI-SAR ADC.

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Jianyu Zhong (S'13) received B.Sc. degree and M.Sc. degree in electronic communication engineering from University of Nanchang, China, in 2006 and 2009, respectively. She is currently working toward the Ph.D. degree in electrical and electronics engineering from the University of Macau, Macao, China. She has studied in an internship program student with SEA (Science Engineering Associates) Corporation in Japan from 2007 to 2009. Her research interests include digital-assisted power-efficient high-resolution Nyquist A/D converter designs.

Yan Zhu (S'10–M'14) received the B.Sc. degree in electrical engineering and automation from Shanghai University, Shanghai, China, in 2006, and the M.Sc. and Ph.D. degrees in electrical and electronics engineering from the University of Macau, Macao, China, in 2009 and 2011, respectively. She is now an Assistant Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. She received the Chipidea Microelectronics Prize and Macao Scientific and Technological R&D for Postgraduates Award—Postgraduate Level in 2012 for outstanding Academic and Research achievements in Microelectronics, as well as the Student Design Contest award in A-SSCC 2011. Her research interests include low-power and wideband high-speed Nyquist A/D converters as well as digitally assisted data converter designs.

Sai-Weng Sin (S'98–M'06–SM'13) received the B.Sc., M.Sc., and Ph.D. degree (with highest honor) in electrical and electronics engineering from University of Macau, Macao, China, in 2001, 2003, and 2008, respectively. He is currently an Assistant Professor with the Faculty of Science and Technology, University of Macau, and is the Coordinator of the Data Conversion and Signal Processing (DCSP) Research Line in State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. He has authored one book, entitled *Generalized Low-Voltage Circuit Techniques for Very High-Speed Time-Interleaved Analog-to-Digital Converters* (Springer) and over 70 technical journals and conference papers in the field of high-performance data converters and analog mixed-signal integrated circuits. Dr. Sin has been a member of the Technical Program Committee of IEEE Sensors 2011 and IEEE RFIT 2011–2012 Conference, Review Committee Member of Prime Asia 2009 Conference, Technical Program, and Organization Committee of the 2004 IEEE AVLSI Workshop, as well as the Special Session Co-Chair and Technical Program Committee Member of 2008 IEEE APCCAS Conference. He is currently the Secretary of the IEEE Solid-State Circuit Society (SSCS) Macau Chapter and IEEE Macau CAS/COM Joint Chapter. He was the co-recipient of the 2011 ISSCC Silk-Road Award, Student Design Contest winner in A-SSCC 2011 and the 2011 State Science and Technology Progress Award (second-class), China.

Seng-Pan U (S'94–M'00–SM'05) received the B.Sc. and M.Sc degree in 1991 and 1997, respectively, and the joint Ph.D. degree from the University of Macau (UM), China, and the Instituto Superior Técnico (IST), Portugal, in 2002 with highest honor in the field of high-speed analog IC design.

Dr. U has been with Faculty of Science & Technology, UM since 1994, and is currently Professor and Deputy Director of State-Key Laboratory of Analog & Mixed-Signal (AMS) VLSI. During 1999–2001, he was on leave to the Integrated CAS Group, Center of Microsystems in IST, as a Visiting Research Fellow.In 2001, Dr. U co-founded the Chipidea Microelectronics (Macau), Ltd. as the Engineering Director, and since 2003 the corporate VP-IP Operations Asia Pacific for devoting in advanced AMS Semiconductor IP product development. The company was acquired in 2009 by the world leading EDA & IP provider Synopsys Inc. (NASDAQ: SNPS), currently as Synopsys Macau Ltd. He is also the corporate Senior Analog Design Manager and Site General Manager.

Dr. U authored and coauthored 140+ publications, 4 books in Springer and China Science Press in the area of VHF SC filters, analog baseband for multi-standard wireless transceivers, and very high-speed TI ADCs. He co-holds 9 U.S. patents.

Dr. U received ~30 research & academic/teaching awards and is co-recipient of 2014 ESSCIRC Best Paper Award. He is also the advisor for 30 various international student paper award recipients, e.g. SSCS Pre-doc Achievement Award, ISSCC Silk-Road Award, A-SSCC Student Design Contest, IEEE DAC/ISSCC Student Design Contest, ISCAS, MWSCAS, PRIME and etc. Dr. U as the Macau founding Chairman received The 2012 IEEE SSCS Outstanding Chapter Award. Both at the first time from Macau, he received the Science & Technology (S&T) Innovation Award of Ho Leung Ho Lee Foundation in 2010, and also The State S&T Progress Award in 2011. He also received both the 2012 and 2014 Macau S&T Invention and Progress Awards. In recognition of his contribution in academic research & industrial development, he was awarded by Macau SAR government the Honorary Title of Value in 2010. He was also elected as the "Scientific Chinese of the Year 2012."

Dr. U is currently IEEE Senior Member, the Industrial Relationship Officer of IEEE Macau Section, Chairman of IEEE SSCS and CAS/COMM Macau chapter. He is IEEE SSCS Distinguished Lecturer (2014–2015). He was A-SSCC 2013 Tutorial Speaker for Energy-Efficient SAR-Type ADCs and has also been with technical review committee of various IEEE journals, e.g. JSSC, TCAS, TVLSI and etc. He was the chairman of the LOC of IEEE AVLSIWS'04, the TPC co-Chair of IEEE APCCAS'08, ICICS'09 and PRIMEAsia'11. He is currently Financial Chair of IEEE ASP-DAC'16, TPC of ISSCC, A-SSCC, RFIT, VLSI-DAT, and Editorial Board member of the journal *AICSP*.

Rui Paulo Martins (IEEE M'88–SM'99–F'08), born April 30, 1957, received B.S. (5-years), M.S., and Ph.D. degrees, as well as Habilitation for Full-Professor in electrical engineering and computers from Department of Electrical and Computer Engineering (DECE), Instituto Superior Técnico (IST), University of Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively. He has been with DECE/IST since October 1980. Since 1992, he has been on leave from IST and is also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he is currently a Chair-Professor and Vice-Rector (Research). Within the scope of his academic activity he has taught 21 bachelor and master courses and supervised (or co-supervised) 38 theses, Ph.D. (17) and Masters (21). He has co-authored: 6 books and 4 book chapters; 13 US Patents; 314 papers, in scientific journals (80) and in conference proceedings (234); as well as 60 other academic works, for a total of 397 publications. He was a co-founder of Chipidea Microelectronics (Macao) [now Synopsys] in 2001/2002, and created in 2003 the Analog and Mixed-Signal VLSI Research Laboratory of University of Macau, elevated in January 2011 to State Key Laboratory of China (the 1st in Engineering in Macao), being its Founding Director.

Prof. Rui Martins was the Founding Chairman of IEEE Macau Section (2003–2005), and IEEE Macau Joint-Chapter on CAS/COM (2005–2008) [2009 World Chapter of the Year of IEEE CASS]. He was the Vice-President for the Region 10 of IEEE CASS (2009–2011) and the Vice-President (World) Regional Activities and Membership of IEEE CASS (2012–2013). Plus he was the Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS (2010–2013), nominated Best Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS for 2012 to 2013. Plus, he was member of IEEE CASS Fellow Evaluation Committee (Classes 2013 and 2014). He received 2 government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In July 2010 was elected, unanimously, as Corresponding Member of the Portuguese Academy of Sciences (in Lisbon), being the only Portuguese Academician living in Asia.