A Multichannel Power-Supply-Modulated Microstimulator With Energy Recycling

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Editor's notes:
This paper presents an energy recycling power-supply-modulated multichannel microstimulator with energy recycling. To improve the stimulation efficiency, the supply of the current driver is modulated according to the instantaneous electrode voltage. Multichannel stimulation together with energy recycling is achieved through decoupling the electrode array from the power supply. A digital pulse-skipping PWM quasi-PID (D-PS-PWM-QPID) controller is proposed to improve the stimulation efficiency.
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ELECTRICAL STIMULATOR HAS been playing an important role in both disclosing secrets of the biological sensory system and recovering functions of various impaired sensory organs, such as ear, eye, and vestibular organ. Apart from that, it has also been exploited in therapeutic applications, as demonstrated in functional electrical stimulation (FES) for the upper limb, lower limb, proprioceptor, dorsal loop ganglia for relief of low back pain, and subthalamic nucleus for treatment of Parkinson's disease.

Electrical stimulators are devised to deliver charge packets to the axon hillock regions inside the neurons by an amount that can instigate the excitatory postsynaptic potential to a voltage level exceeding the threshold (normally between 11 and 29 nC). Due to the wide varying parasitic electrode impedance in different application scenarios (from tens of ohms to tens of kiloohms), there exists a wide array of designs covering distinct requirements and specifications [1]–[9]. Yet, improving the stimulation efficiency still remains a challenging research problem that needs to be resolved as a result of the limited energy available in such applications, especially for those requiring multiple electrode stimulation. In this article, we propose a multichannel power-supply-modulated microstimulator capable of energy recycling. By tracking the instantaneous electrode voltage, the thermal dissipation of the current drivers is reduced. Multichannel stimulation is achieved through decoupling the electrode array from the power supply, which can also provide the isolation required for improved safety. The digital pulse-skipping PWM quasi-PID (D-PS-PWM-QPID) controller is proposed to deliver the required charge for regulating the modulated power supply under various stimulation scenarios without parameter tuning or external passive components.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.
Digital Object Identifier 10.1109/MDAT.2016.2533359
Date of publication: 23 February 2016; date of current version: 17 June 2016.

 2168-2356/16 © 2016 IEEE

This article is organized as follows. Next, we summarize and discuss various existing microstimulator topologies and their limitations. Then, we describe the proposed microstimulator topology and its operation. We follow with the explanation of circuit implementations on different building blocks and the presentation of measurement results from the prototype chip.

Stimulator power supply topologies

In this section, we first summarize various microstimulator topologies. Existing microstimulators can be mainly classified into three different categories according to how the electrode energy is supplied: 1) fixed voltage (FV); 2) dynamic voltage scaling (DVS); and 3) direct voltage forming (DVF).

FV supply

The simplest method of powering electrode drivers is through a regulated voltage, which should be higher than the electrode voltage plus a compliance voltage (headroom required for the current controlling transistors). Figure 1a shows the FV microstimulator topology as demonstrated in [2]. The alternating current (ac) power across the inductor (L_1) is rectified through the full wave rectifier which is composed of two diodes and two capacitors (C_2, C_3) to generate the intermediate power rails V_{DDr} and V_{SSr}. They are then regulated as the biphasic supplies V_{DD} and V_{SS} by the low dropout regulators (LDOs). Despite its simple implementation and straightforward regulation scheme, the FV topology can introduce excessive heat loss in the current driving stage, especially when the magnitude of the electrode voltage is much less than that of V_{DDr} and/or V_{SSr}.

DVS supply

To tackle the efficiency overhead in the current driving stage in the FV topology, DVS strategy is demonstrated in [1], [4], and [9] to adjust the supply rails for the current drivers and hence reduce the energy wasted across the current controlling transistors.

In [1], a multilevel shunt regulator for adjusting the supply rail is employed, as shown in Figure 1b. In this topology, a closed-loop control including an external power transmitter is accomplished by reporting the instantaneous electrode and supply voltages back to the wireless power transmitter. Even though DVS can reduce the current driver overhead by adaptively reducing the supply voltage, energy is still wasted due to the change in the electrode voltage during stimulation, which triggers the development of DVF topologies.

DVF supply

To further reduce the thermal dissipation across the current-controlling transistors between the power rail and the electrode, a voltage waveform, which is derived from the instantaneous electrode voltage for driving a specific amount of current, can be generated and applied to the electrode with a DVF supply [3], [5]–[7]. Figure 1c shows the inductor-based dc–dc converter with DVF supply introduced in [3]. It comprises the power transistors M_{P1} and M_{N1}, the fast voltage controller/pulse generator, the current sensor/slow current controller, and an LC output filter for generating a smooth voltage waveform on the electrode. One of the additional benefit of this topology is that the part of energy transferred to the electrode is recovered back to the power source. However, this scheme exhibits individual electrode control, which ultimately limits its scalability for multiple electrode applications.

Proposed microstimulator design

From the discussions in the previous section, it can be observed that both the FV- and DVS-based stimulators can have excessive heat loss that cannot be reduced. Also, even though existing DVF-based stimulators can minimize the heat loss in the current drivers, the requirement for a separate switched-mode power supply (SMPS) per electrode results in limited scalability. The direct coupling of the power stage and the electrode may also lead to tissue damage in case of failure in the power stage.

Proposed stimulator system

The proposed power-supply-modulated microstimulator topology with energy recycling is shown in Figure 2. It employs a global SMPS that can be shared among all the electrode drivers to achieve an online DVS according to the electrode voltage. The SMPS modulates the voltage at the intermediate energy storage capacitor (C_{IESC}), either to feed the charge into the electrodes in the anodic stimulation phase, or to drain the charge from the electrodes in the cathodic stimulation phase. When compared to the DVF-based stimulator topologies that also employ an SMPS for driving the charge

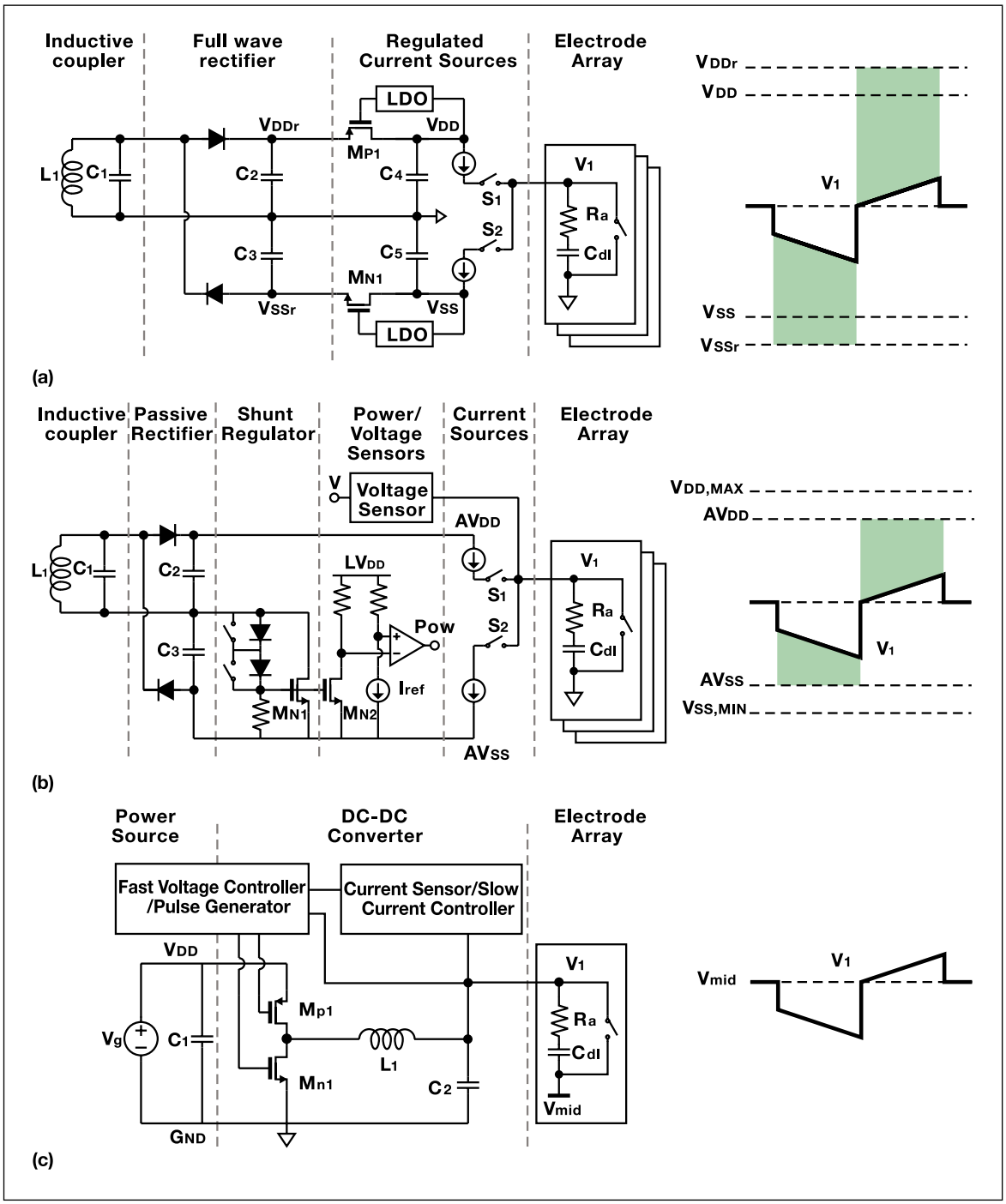

Figure 1. Stimulator topologies based on (a) the FV supply with LDOs [2]; (b) DVS supply with an external control loop [1]; and (c) DVF supply with energy recycling [3].

to/from the electrodes, the use of C_{IESC} as an intermediate charge reservoir allows the proposed topology to decouple the individual electrode drivers from the power supply. As a result, an optimal electrode voltage across electrodes can be obtained by simply regulating the voltage across C_{IESC}, enabling our proposed topology to drive an arbitrary number of electrodes. An adiabatic energy recycling approach similar to [3] but with a reduced control overhead for multiple electrode applications is also introduced to further improve the stimulation efficiency. Apart from that, direct

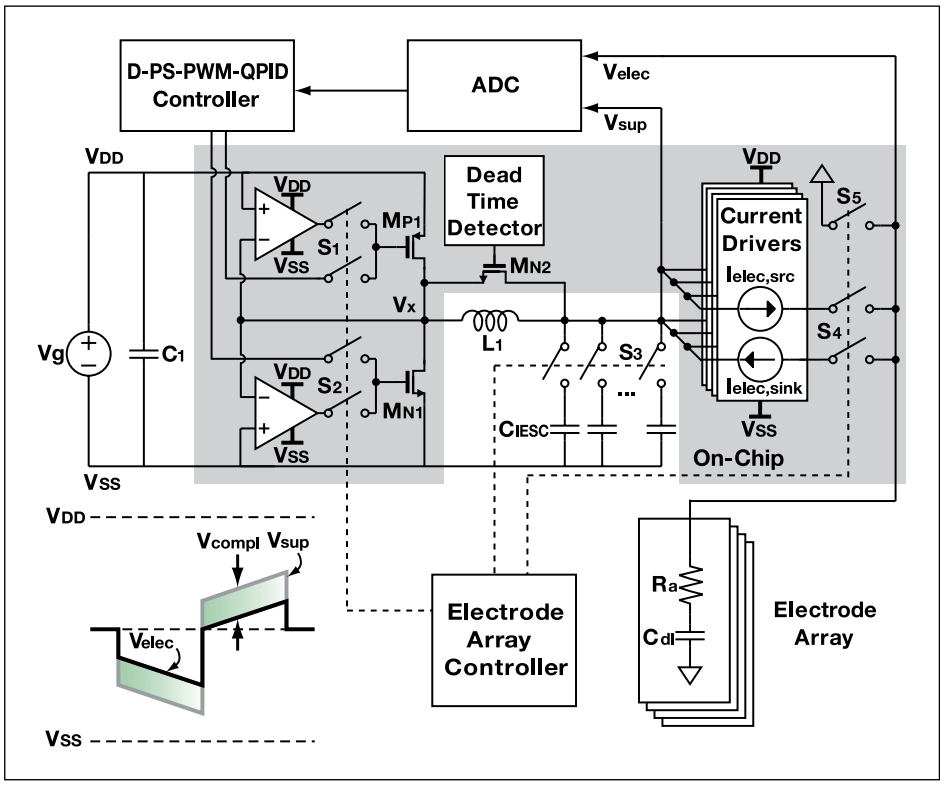

Figure 2. Block diagram of the proposed power-supply-modulated microstimulator system and its output waveform during a biphasic stimulation cycle.

current (dc) flowing from the source V_g to the electrodes can be blocked even if the current-controlling transistors fail.

System topology. The system is powered by a 6-V dc source V_g. M_{P1} and M_{N1} serve as power switches and perform as an active diode (together with the comparators) to reduce the voltage drop across the body diodes in the power switches down to the millivolt level. M_{N2} is controlled by the dead time detector (DTD) for suppressing the voltage ringing across the inductor. The D-PS-PWM-QPID controller takes V_{sup} and V_{elec} as inputs and servos V_{sup} to continuously track $V_{elec} \pm V_{compl}$, where V_{compl} is the headroom requirement of the current drivers. The D-PS-PWM-QPID controller (synthesized using FPGA) and the ADC (AD7658 by Analog Devices) are off-chip components for improved flexibility during measurement.

Operating principle. Similar to [3], the proposed microstimulator transfers energy from the energy source (V_g) into the double-layer capacitance (C_{dl}) of the electrode array in the forward buck mode, and later on recollects the charges stored in C_{dl} back into the source in the reverse boost mode. In the cathodic stimulation phase, M_{N1} is turned on. I_L rises and the magnetic energy is gradually built up in the inductor L. When I_L falls down to zero, M_{N1} is turned off. M_{P1} is turned on when $V_x > V_{DD}$, recovering the energy stored on C_{dl} back to the source V_g. During the anodic stimulation phase, the charge is transferred from V_g via C_{IESC} to the electrode array, with V_{sup} ramping up to track the transient of V_{elec}. Upon $V_x < V_{SS}$, M_{N1} is turned on (i.e., L is energized) and M_{P1} is cut off. The dead time detector turns on M_{N2} at the end of the energizing and de-energizing cycles to prevent the EMI effect caused by LC resonance at V_x.

Performance comparison

Equations for comparison. The stimulation efficiency (η_{stim}) is utilized for comparing the proposed topology with the existing designs introduced above, and is defined as [7]

$$\eta_{stim} = \frac{E_{elec}}{E_{sup}} \tag{1}$$

where E_{elec} and E_{sup} are the energy consumed in the electrode and drawn from the source V_g, respectively. In current-source (CS)-based stimulator designs, typically the losses can be summarized as: 1) E_{Ra}, the thermally dissipated energy across R_a; 2) E_{Cdl}, the energy dissipated in C_{dl}; and 3) E_{drive}, the energy dissipated over the current driver. They are defined as

$$E_{Ra} = V_{Ra} I_{stim} N_{elec} T_{stim} \tag{2}$$

$$E_{Cdl} = \frac{1}{2} V_{Cdl} I_{stim} N_{elec} T_{stim} \tag{3}$$

$$E_{drive} = V_{drive} I_{stim} N_{elec} T_{stim} \tag{4}$$

where T_{stim} is the duration of the anodic/cathodic stimulation phase; I_{stim} is the stimulation current per channel; N_{elec} is the number of simultaneously

driven electrodes; and V_{Ra}, V_{Cdl}, and V_{drive} are the voltage across R_a, C_{dl}, and the current driver, respectively. For comparison, note that all the designs exhibit the same E_{elec}, which is defined as

$$E_{elec} = 2(E_{Ra} + E_{Cdl}). \quad (5)$$

In case of E_{sup}, as it is directly related to how the stimulation currents are delivered, its definition varies according to the particular implementations. For the FV supply, as the stimulation current I_{stim} is drawn through the current driver from V_{DD} during each stimulation phase, the corresponding energy consumed is

$$E_{sup,FV} = 2(E_{Ra} + 2E_{Cdl} + E_{drive}) \quad (6)$$

which is fixed and proportional to V_{DD} (as $V_{DD} = V_{Ra} + V_{Cdl} + V_{drive}$). E_{Cdl} is multiplied by 2 due to the triangular waveform across C_{dl}. With the same assumptions, the energy consumed by a CS stimulator using a DVS supply is given by

$$E_{sup,DVS} = \left(\frac{2}{\eta_{sup}}\right)(E_{Ra} + 2E_{Cdl} + E_{drive}) \quad (7)$$

where η_{sup} is the efficiency of the SMPS used in the corresponding topology. Note that as the supply voltage is modulated by DVS, the E_{drive} term in (7), which is limited by V_{compl}, is less than that in (6), resulting in an improvement in the stimulation efficiency. The $2/\eta_{sup}$ term in (7) is the multiplication factor that accounts for the stimulation energy consumed by the SMPS for converting the source energy into the energy delivered to the electrodes.

Similarly, the energy consumed by a CS stimulator powered by a SMPS DVF supply presented in [3] can be formulated as

$$E_{sup,DVF} = \left(\frac{1}{\eta_{sup}} - \eta_{sup}\right)(E_{Cdl} + E_{mid}) + \left(\frac{2}{\eta_{sup}}\right)E_{Ra} \quad (8)$$

with

$$E_{mid} = V_{mid} I_{stim} N_{elec} T_{stim} \quad (9)$$

where E_{mid} is the energy loss due to the electrode baseline potential V_{mid}. The first term in (8) denotes the energy from E_{Cdl} and E_{mid} being consumed by the SMPS during both the anodic and cathodic stimulation phases. Similarly, the second term is the energy consumed by the SMPS due to R_a.

Finally, the energy consumed by the proposed stimulator can be expressed as

$$E_{sup,PRO} = \left(\frac{2}{\eta_{sup}}\right)(E_{Ra} + E_{compl}) + \left(\frac{1}{\eta_{sup}} - \eta_{sup}\right)(E_{Cdl} + E_{lESC}) \quad (10)$$

with

$$E_{compl} = V_{compl} I_{stim} N_{elec} T_{stim} \quad (11)$$

$$E_{lESC} = \frac{1}{2} C_{lESC}(V_{Ra} + V_{Cdl} + V_{compl})^2 \quad (12)$$

where E_{compl} and E_{lESC} are the energy loss due to the current source compliance voltage V_{compl} and C_{lESC}, respectively. In (10), the first term defines the energy dissipation that cannot be recovered, while the second term denotes the energy stored in C_{dl} and C_{lESC} that can be restored to the source adiabatically.

Biphasic stimulation scenarios. We contrived two scenarios to show that the proposed stimulator topology can be favorably applied in stimulators both for low-density electrode array (LDEA) applications such as deep brain stimulation and for high-density electrode array (HDEA) applications such as retinal prosthesis. In the LDEA scenario, we used an electrode model made up of a series RC circuit with $R_a = 1$ kΩ and $C_{dl} = 1$ μF. These electrode parameters were set based on the iridium oxide electrode used in [5]. In the HDEA scenario, R_a is scaled up to 25 k Ω with reference to retinal prosthesis applications; and the corresponding C_{dl} can be approximated as 20 nF [8].

For fair comparison among various topologies, we normalized the input rail-to-rail voltage $V_{DD} + |V_{SS}|$ to 10 V for covering both the anodic and cathodic stimulation phases. The maximum electrode voltage $V_{elec,MAX}$ is defined by $V_{Ra,MAX} + V_{Cdl,MAX}$, where $V_{Ra,MAX}$ and $V_{Cdl,MAX}$ are the maximum voltage across R_a and C_{dl}, respectively. With the stimulation period $T_{stim} = 1$ ms, the corresponding $I_{stim,MAX}$ is referenced to be 2 mA [4] and 53 μA [8] for LDEA and HDEA, respectively. In both cases, these parameters lead to $2 \times V_{elec,MAX} = 8$ V, which is within the supply rails for all the topologies. With a refresh rate of 60 frames/s for a 1024-electrode array in the HDEA scenario,

all the electrodes should be stimulated once within a 16.6-ms time frame. By considering a 2-ms biphasic stimulation pulse, eight time slots can be obtained within one time frame of 16.6 ms, and the number of concurrent stimulating electrodes N_{elec} can be calculated to be 128 for a 1024-electrode array. For the case of LEDA where, in total, 32 electrodes are considered, N_{elec} is assigned to be 4 so a full scan can be achieved in one time frame.

Comparison of stimulators. Figure 3 shows how the stimulation efficiency (η_{stim}) varies according to I_{stim}, R_a, and N_{elec}, with other parameters as defined in the Biphasic stimulation scenarios section. For all the calculations, it is assumed that $\eta_{sup} = 70\%$ and the worst case $V_{compl} = 500$ mV. From Figure 3a, it can be observed that the proposed topology is compared favorably to the other designs except when I_{stim} is very small. For the case of varying R_a, as shown in Figure 3b, the proposed topology generally achieves the best η_{stim}, and is only surpassed by FV with a large R_a (mainly due to the reduction of the voltage across current-controlling transistors). This increasing R_a also increases the V_{Ra}/V_{Cdl} ratio which η_{stim} is heavily dependent on [8]. Figure 3c demonstrates that η_{stim} of the proposed topology increases with an increased N_{elec} under both the LDEA and HDEA scenarios, demonstrating that the energy overhead caused by the charging and discharging of C_{IESC} can be distributed over the channels as N_{elec} increases.

Circuit implementation

In this section, we outline the choice for passive components, as well as describe the core building blocks of the proposed system: the current driver, the active diode, the dead time detector, and the D-PS-PWM-QPID controller.

Design consideration for passive components

Inductor. Figure 4a and 4b shows the evolution of V_{sup} and V_{elec} during one switching period of the power MOSFETs (M_{P1} and M_{N1}) both in the forward buck and reverse boost modes, respectively. ΔV_{ripple} and ΔV_{ref} indicate the maximum allowable voltage excursion for the modulated supply V_{sup} and its change during one period (T_s), respectively.

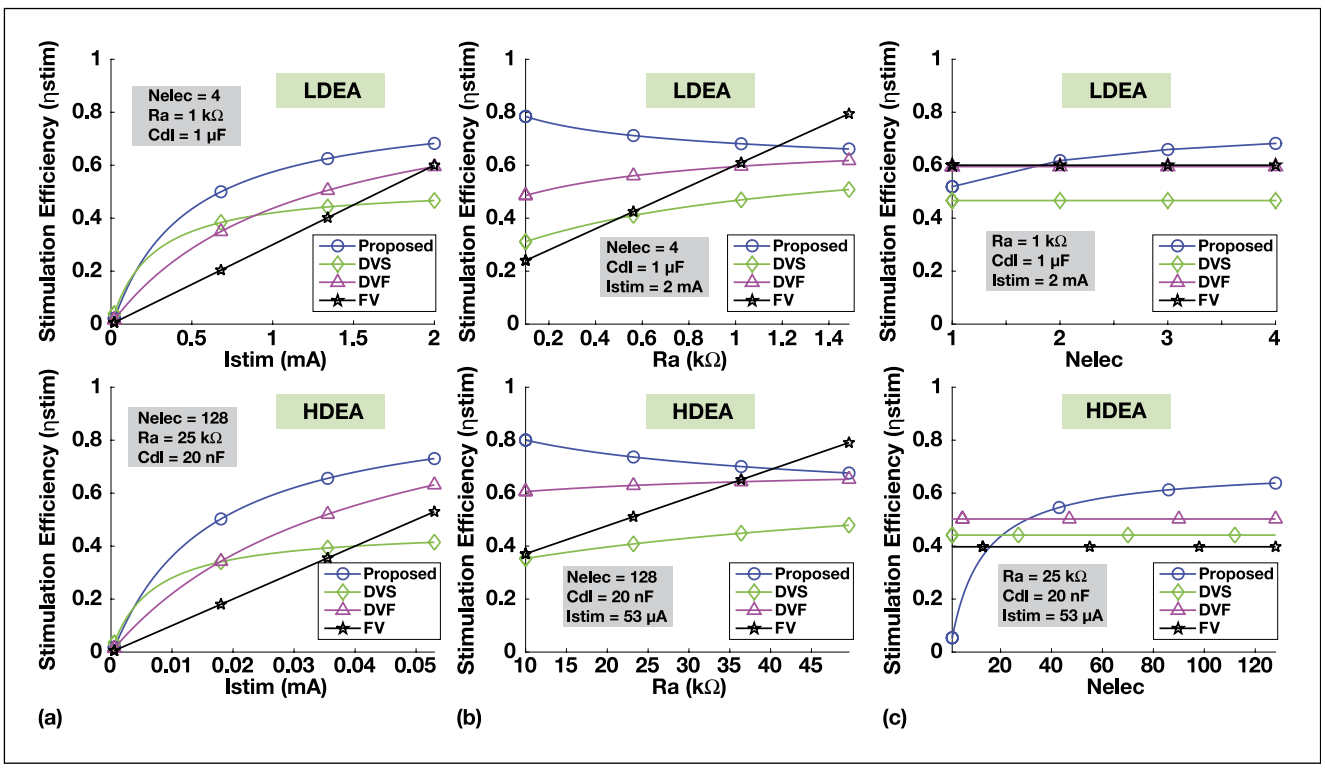

Figure 3. Stimulation efficiency (η_{stim}) in both LDEA and HDEA scenarios for various topologies as a function of (a) I_{stim}; (b) R_a; and (c) N_{elec}.

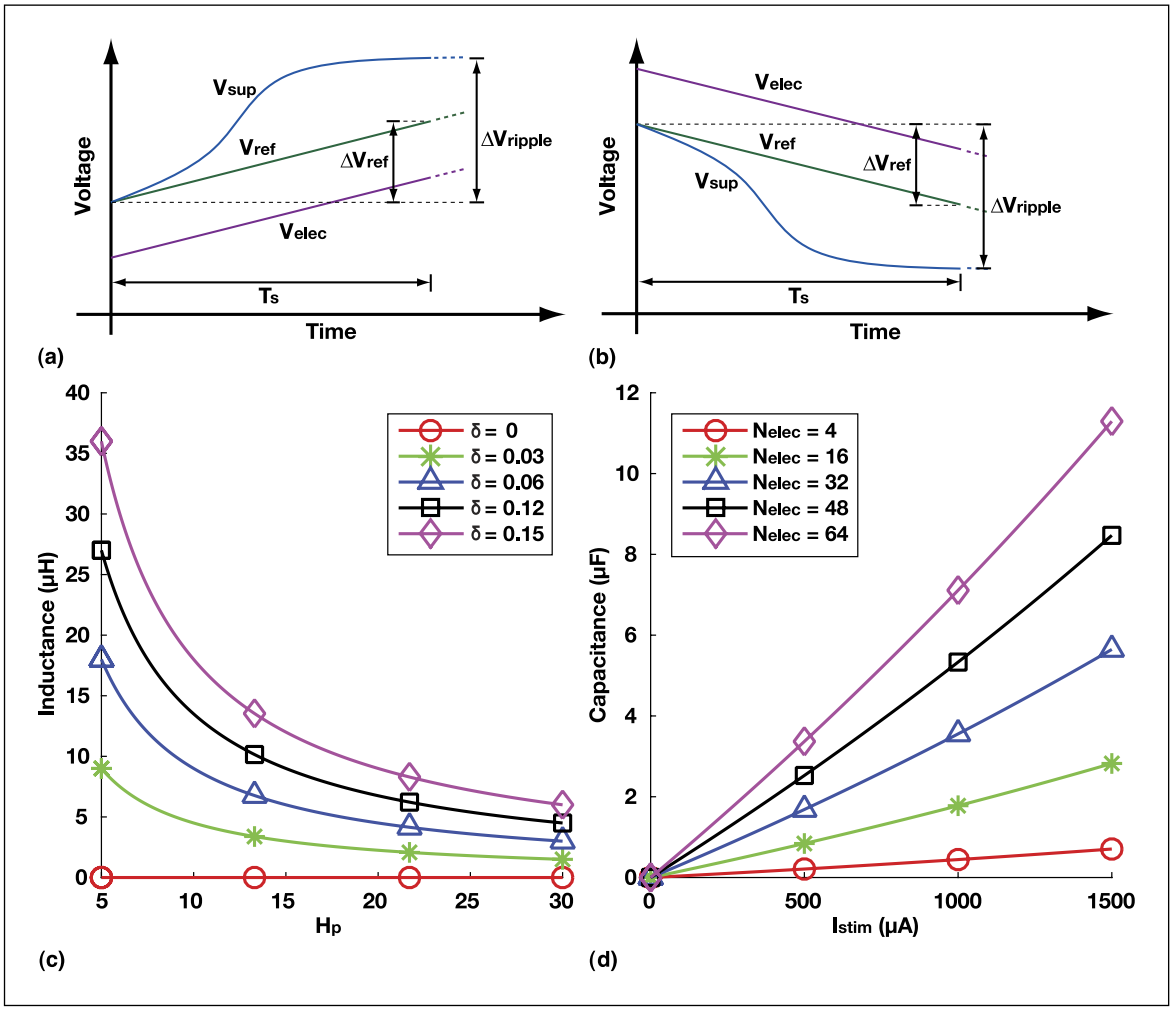

Figure 4. Conceptual timing diagram during one switching cycle for the calculation of the required capacitance in (a) forward buck operation; and (b) reverse boost operation. Simulation results of the required (c) inductance; and (d) capacitance under different operation parameters.

The inductor (L) relays energy from V_g to C_{IESC}, and should be chosen to have an adequate peak-to-average current ratio, $H_p = I_{\text{pk}}/I_{\text{avg}}$, where

$$I_{\text{pk}} = \delta \cdot T_s(V_g - V_{\text{sup}})/L \tag{13}$$

$$I_{\text{avg}} = \frac{\delta(\delta + \delta')T_s(V_g - V_{\text{sup}})}{2L} = C_{\text{IESC}} \cdot \Delta V_{\text{ripple}}/T_s \tag{14}$$

where δ is the duty cycle and δ' is the ratio of the discharging time to T_s. As a result, the required L can be expressed as a function of H_p as follows:

$$L = \frac{T_s^2 \cdot \delta \cdot (V_g - V_{\text{sup}})}{C_{\text{IESC}} \cdot \Delta V_{\text{ripple}} \cdot H_p}. \tag{15}$$

Figure 4c shows L as a function of H_p, with $V_g = 6$ V, $T_s = 5$ μs, $V_{\text{sup}} = 3$ V, and $\Delta V_{\text{ripple}} = 50$ mV, respectively. As the system mainly operates in discontinuous conduction mode (DCM) with $\delta \leq 0.15$, the value of L is chosen to be 10 μH, which results in a H_p close to 20.

Intermediate energy storage capacitor (IESC). Based on the voltage dynamics during a switching period as shown in Figure 4a and 4b, we can derive the required C_{IESC} for driving a specific load ($N_{\text{elec}}, I_{\text{stim}}$). Note that the charging voltage amplitude during T_s is $\Delta V_{\text{ripple}} - \Delta V_{\text{ref}}$. As a result, the required C_{IESC} to restrict ΔV_{ripple} while concurrently stimulating N_{elec} electrodes

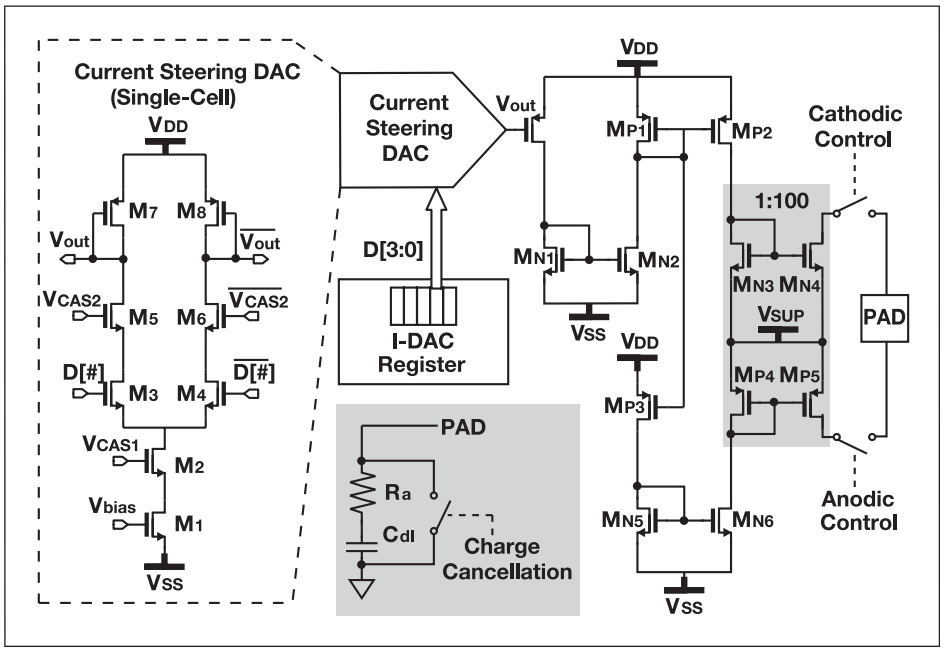

Figure 5. Schematic of the electrode current driver.

with a current I_{stim} per channel can be determined as

$$C_{IESC} = \frac{I_{stim} N_{elec} T_s}{\Delta V_{ripple} - \Delta V_{ref}} = \frac{C_{dl} I_{stim} N_{elec} T_s}{C_{dl} \Delta V_{ripple} - I_{stim} T_s}. \quad (16)$$

By using the relationship between the required capacitance as a function of I_{stim} as shown in Figure 4d, a C_{IESC} value of 1 μF was chosen for $\Delta V_{ripple} = 50$ mV, when driving $I_{stim} < 1.5$ mA and $N_{elec} = 4$.

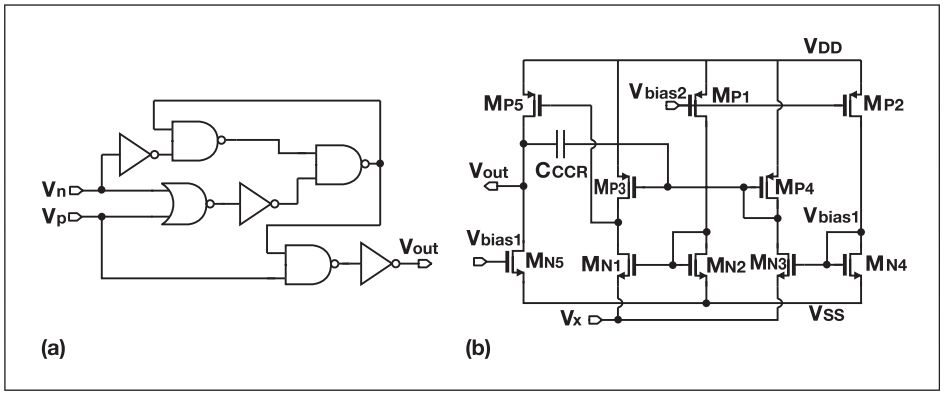

Figure 6. Schematic of (a) the DTD logic for reverse boost opeartion; and (b) the comparator for active diode operation of the power NMOS.

Current driver

Each stimulation channel requires a dedicated current drivers to steer the current into and out of the electrodes. Figure 5 shows the schematic of the implemented current driver block that can provide a current driving range from 0 to 1.2 mA in a step of 75 μA. The current steering digital-to-analog converter (DAC) generates a binary weighted current (controlled by V_{bias}) with M_{3-4} steering the current through each of the current steering DAC cell. M_2 forms a cascoding stage to regulate the drain-to-source voltage of M_1, while M_{5-6} are utilized to protect the current cell from the high voltage at the drains of M_{7-8}. For improved energy efficiency, the current mirror ratio formed by M_{N3-4} and M_{P4-5} is set to 1:100. Both M_{N3-4} and M_{P4-5} are implemented using long channel transistors with a channel length of 2 μm. Charge cancellation is implemented with a simple switch for electrode shorting to the bulk tissue potential.

Dead time detector and active diodes

DTD circuit. To suppress the inductor ringing during the forward buck operation, a DTD logic similar to [10] is adopted to insert a brief dead time between the conduction of the power switches M_{P1} and M_{N1} as shown in Figure 2. The DTD logic was devised for preventing M_{N2} from turning on at the dead time of power transistors during switching instants for additional power savings. The DTD is further extended for reverse boost operation by exchanging the gate control polarity for M_{P1} and M_{N1} using the logic control as shown in Figure 6a.

Active diode circuit. M_{P1} in Figure 2 can be converted into an active diode during the reverse boost operation by introducing a PMOS driving

comparator to form a CMOS-control rectifier (CCR) as described in [11] so as to reduce the forward-voltage drop for improving the efficiency. To accommodate for the use of forward buck operation, a complementary CCR topology that can drive both M_{P1} and M_{N1} in Figure 2 is adopted. Similar to [11], the source of M_{N1-4} in Figure 6b is utilized to serve as inputs of subcomparators. High slew rate is achieved through the cross-coupled subcomparators formed by M_{N1-2} and M_{N3-4} in Figure 6b, with the help of a 50-fF coupling capacitor C_{CCR}, which provides the transient latching action.

D-PS-PWM-QPID controller

In microstimulator applications, the power-stage parameters and the output voltage slew rate requirements are highly varying under different phase and loading conditions. As a result, the SMPS controller should: 1) exhibit robust operation under varying power-stage transfer function; 2) accommodate a broad output power dynamic range; 3) possess fast tracking capability, especially during reference voltage discontinuity at the interphase boundary; and 4) dissipate low power consumption for improved light load efficiency. The hysteretic controller, which can be simply implemented using two comparators, can only operate in buck converters with resistive load, and is therefore not suitable in our application. Autotuning PWM controller acquires the knowledge about the power stage from either the response to the perturbed test signal or the compensated error signal. Although online parameter adjustment is highly desirable, achieving fast response for the large-signal time-varying reference voltage with linear PWM controllers can be problematic as they are

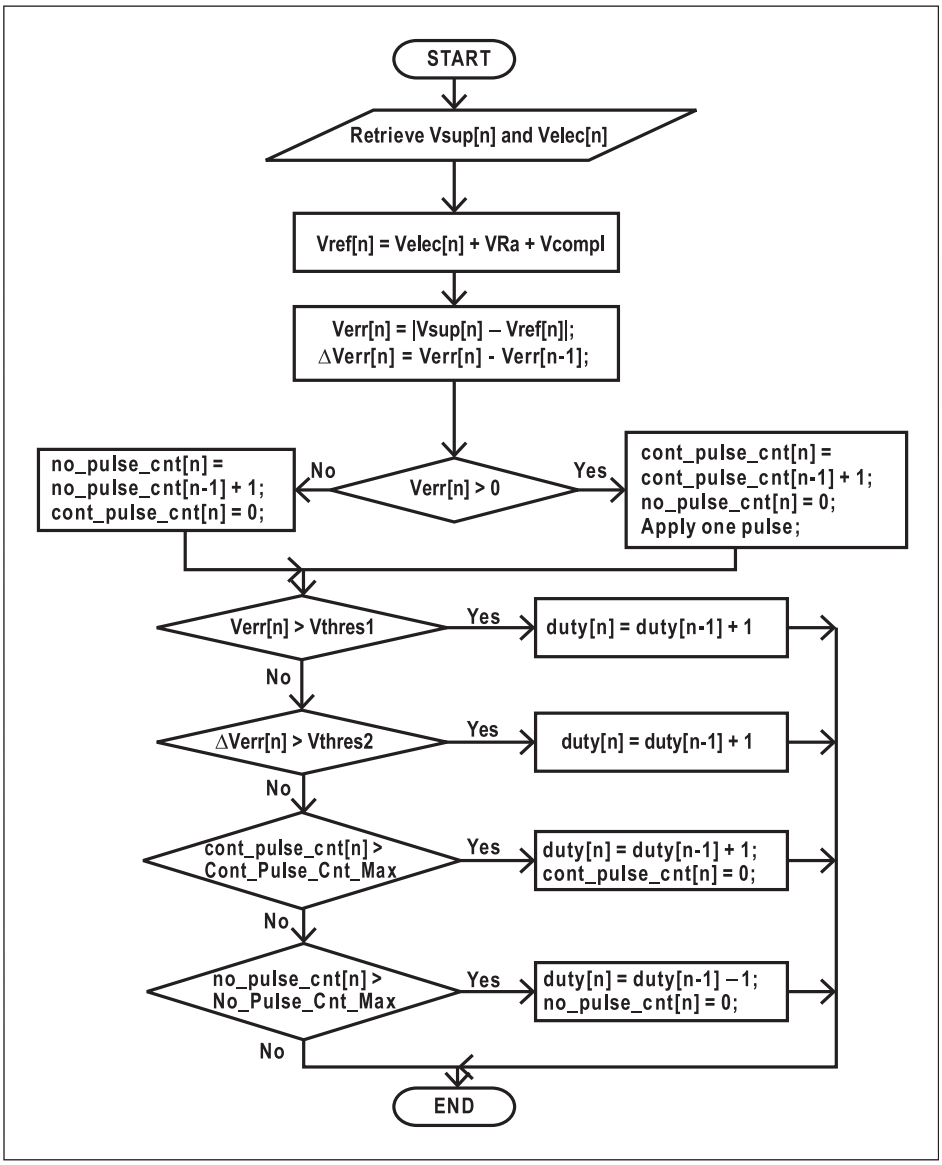

Figure 7. Flowchart of the D-PS-PWM-QPID controller.

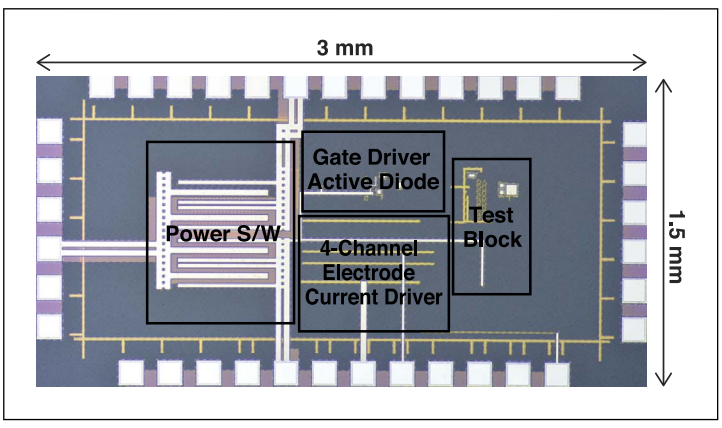

Figure 8. Microphotograph of the prototype chip.

optimized for small-signal response. For the sliding mode controllers, even though they can guarantee unconditional stability over wide line and load configurations with varying system parameters, the associated high design complexity and implementation cost to fulfill the hitting, existence, and stability conditions can be undesirable.

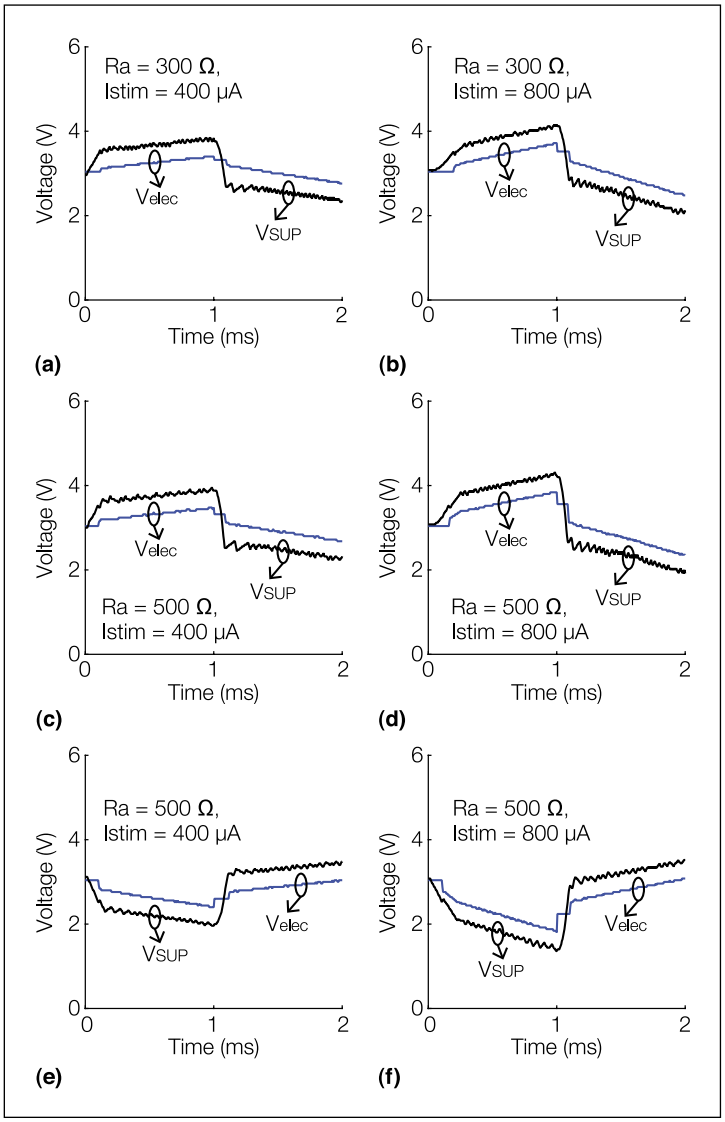

Figure 9. Measured voltage waveforms of the prototype chip during a biphasic, anodic-first stimuli, with $V_{compl} = 0.5$ V and $N_{elec} = 4$ driving (a) $I_{stim} = 400\ \mu$A through $R_a = 300\ \Omega$; (b) $I_{stim} = 800\ \mu$A through $R_a = 300\ \Omega$; (c) $I_{stim} = 400\ \mu$A through $R_a = 500\ \Omega$; (d) $I_{stim} = 800\ \mu$A through $R_a = 500\ \Omega$. Measured waveform during biphasic, cathodic-first stimuli, with $V_{offset} = 0.5$ V and $N_{elec} = 4$ driving (e) $I_{stim} = 400\ \mu$A through $R_a = 500\ \Omega$; (f) $I_{stim} = 800\ \mu$A through $R_a = 500\ \Omega$.

Figure 7 shows the flowchart of the proposed D-PS-PWM-QPID controller. Similar to pulse skipping controllers, it uses the target reference voltage (V_{ref}) as a reference sliding plane to determine the power stage operation to achieve robust control under wide power stage dynamics with low power consumption. V_{ref} is set to $V_{elec} + V_{compl} + V_{Ra}$ at the beginning of each phase transition boundaries, where V_{compl} is as shown in Figure 2. Similar to traditional PID controllers, the proposed controller updates the duty cycle to improve the tracking speed. The error value (V_{errror}) and the differential error value ($\Delta V_{error}[n] = V_{error}[n] - V_{error}[n-1]$) represent the proportional and derivative information, respectively. As shown in the flowchart (Figure 7), if the error (V_{error}) between the target reference voltage and the current V_{sup} deviates more than V_{thres1}, or ΔV_{error} increases, it swiftly updates the duty, thereby making V_{sup} to move faster toward the target voltage level. Note that the output voltage resolution is not restricted by the DPWM resolution, and the proposed controller is free from limit cycle oscillation. *no_pulse_cnt* stores the history of the consecutive pulse-skipping cycles, while *cont_pulse_cnt* shows the history of the consecutive cycles requiring pulses. These two parameters convey the time integral information of the controller. The stability of the proposed D-PS-PWM-QPID is ensured during the design stage over the targeted input/output dynamics using both the state space and transfer function models. The system stability is also verified from the chip prototype with various stimulation settings.

Experimental setup and results

The proposed microstimulator is implemented in a standard 0.18-μm BCDLite CMOS process with 6-V tolerance. As shown in Figure 8, the total die area is 4.5 mm^2 (including pads), with an active area of 0.18 mm^2 per each stimulation channel. The process provides isolated high-voltage 6-V CMOS cells, which are utilized for implementing the transmission gates, power switches, and current controlling transistors in the design. The current design is pad limited due to the requirement for various test circuits. The area consumption per channel is mainly limited by the use of large current controlling transistors and switches for delivering a maximum stimulation current of 1.2 mA. In HDEA scenario where the stimulation current can

be relaxed (as in [2]), a comparable area consumption per channel is achievable, demonstrating the feasibility of the proposed design in HDEA applications. The control signals are generated using a field-programmable gate array (FPGA). Figure 9 shows the typical stimulation waveform under varying stimulation conditions, with $V_{compl} = 0.5$ V. From the waveforms, we can notice that V_{sup} successfully tracks V_{elec} and rapidly transits to appropriate voltage levels at the interphase boundaries. The fluctuation of V_{sup} is mainly caused by the switching activities of the power MOSFETs at 200 kHz, especially during the anodic–cathodic phase transition boundaries where swift duty cycle updates occur.

For the D-PS-PWM-QPID controller, we estimate its power consumption using Synopsis Prime Time static timing analyzer. With an area of 0.022 mm^2, it only dissipates a small power of 52 μW. The test bench used for power estimation generates two separate continuous serial bit streams from the ADC outputs. These bit streams represent the ADC conversion results of V_{sup} and V_{elec}, which are updated at the rising edge of the sampling clock running at 200 kHz. The serial bit streams are synchronized at 4 MHz and subsequently fed into the digital controller. For the multichannel ADC, although it was not integrated in the current prototype, a column parallel 9-b ADC consuming a small power of 1.27 μW and a small area of 7.4 μm $\times$ 490 μm per channel can be added with small overhead [12].

We measured three different I_{stim} levels (400 μA, 800 μA, and 1.2 mA) driving four electrodes with $R_a = 300\ \Omega$, 500 Ω, and 1 kΩ. As shown in Figure 10, the measured η_{stim} are compared with the predicted results calculated in the Performance comparison section. It can be observed that the trend of η_{stim} matches well with the mathematical model. In the prototype system, η_{stim} is limited by the SMPS efficiency (η_{sup}) due to the increased conduction loss along the board traces and off-the-shelf components. In our proposed microstimulator, η_{sup} is mainly limited by the switching loss due to power MOSFETs. This can be caused by: 1) a small E_{sup}; 2) a large voltage excursion at V_{sup}; and 3) a small difference between V_{sup} and V_{DD} or V_{SS}. As shown in Figure 9b, when driving $N_{elec} = 4$, $R_a = 300\ \Omega$, and $I_{stim} = 800\ \mu$A, the voltage excursion amplitude of V_{sup} is approximately 1 V. This prevents excessively high switching activities, leading to a high η_{sup} of 0.75, as shown in Figure 10a. It can also be observed that η_{sup} improves as I_{stim} increases. In contrast, as shown in Figure 10b, where R_a is increased to 500 Ω, the V_{sup} excursion amplitude gets larger. Together with a relatively low E_{sup}, only a lower η_{sup} of 0.6 is achieved. Figure 10c shows the measurement result when $R_a = 1$ kΩ and $I_{stim} = 800\ \mu$A. In this case, a relatively high E_{sup} and a small V_{sup} excursion leads to a moderate η_{sup} close to 0.7.

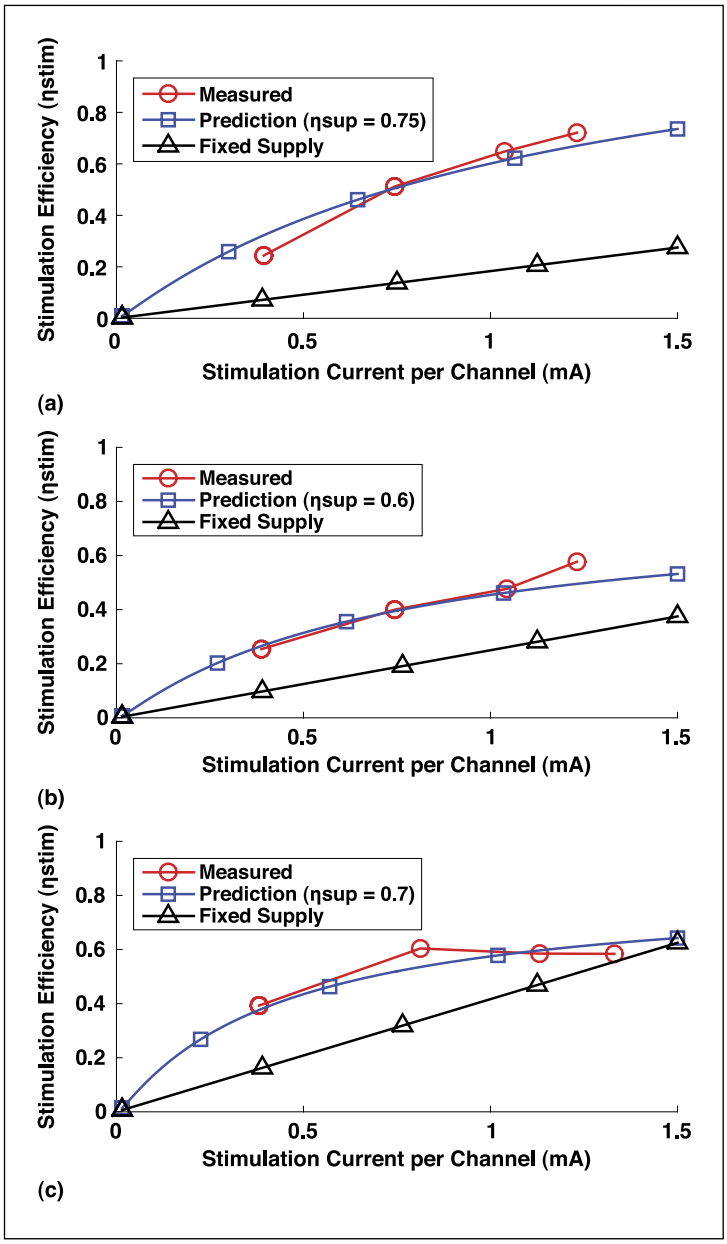

Figure 10. Measured stimulation efficiency when driving four electrodes of which (a) $R_a = 300\ \Omega$, (b) $R_a = 500\ \Omega$, and (c) $R_a = 1$ kΩ.

Table 1 Performance comparison with the state of the art.

Year / Reference	2011 [5]	2012 [3]	2013 [6]	2013 [9]	2013 [4]	2013 [2]	2012 [1]	2015 [7]	This Work
Technology	1.5 µm	0.35 µm	0.18 µm	0.18 µm	0.5 µm	0.18 µm	0.35 µm	0.18 µm	0.18 µm
Power Delivery Method	Switched Capacitor AC-DC Converter based DVF	Bidirectional DC-DC Conveter based DVF	AC-DC Conveter based DVF	Switched Capacitor DC-DC Converter based DVS	AC-DC Power Converter based DVS	AC-DC Power Converter based FV-supply	AC-DC Power Converter based DVS	DC-DC Converter based DVF without Output Filter	Bidirectional DC-DC Converter based IESC Voltage Modulation
Power Supply Control	Internal	Internal	Internal	Internal	Internal	N/A	External	Internal	Internal
Power Saving^	~66%	~62%	20~75%	~50%	58~68%	N/A	N/A	~60%*	~70%
Efficiency of the SMPS	N/A	50~90%	N/A	~82%	72~87%	N/A	N/A	N/A	60~75%
Stim. Current Range	0~136µA	0~450 µA	20~1,000µA	2~504µA	~2,480 µA	3~500µA	4~1,000µA	~10,000µA	0~1,230µA
Electrode Configuration	Split Supply	Single Supply	Split Supply	Split Supply	Split Supply	Single Supply	Single Supply	Split Supply	Single Supply
Supply Voltage Shape	4 Step Stairs	Continuous	Continuous	3 Step Stairs	8 Step Stairs	Fixed	Continuous	HF Pulses	Continuous
Energy Recycling	Yes	Yes	N/A	N/A	N/A	N/A	N/A	N/A	Yes
Voltage Compliance	2.5 V	3 V	3.3 V	11.5 V	4.6 V	20 V	20 V	20 V	6 V
High Density Electrode Array Support	Unscalable	Unscalable	Unscalable	Scalable	Scalable	Scalable	Scalable	Time Multiplex	Scalable

* Estimated from the corresponding literature.
^ Power Saving Percentage compared to FV supply based stimulators

Table I compares the proposed stimulator system with the state of the art. When compared to the FV-supply-based topology, our work can achieve a power saving of 70% which is well comparable with the existing DVF-supply-based systems [3], [5]–[7]. By decoupling the power supply from the electrode using C_{IESC}, the scalability problem as a result of the requirement for a dedicated SMPS per stimulation channel as in [3], [5], [6] or a complex time multiplexing scheme as in [7] can be eliminated, enabling a highly scalable stimulator design suitable for HDEA applications. Extra power saving is also achieved when compared to the DVS-based stimulators as in [1], [4], and [9]. Our proposed system is capable of generating a continuous V_{sup} while supporting energy recycling. Further performance improvement of η_{stim} is expected with an increase in η_{sup} and N_{elec}.

An energy-efficient multichannel power-supply-modulated microstimulator capable of energy recycling is presented. It enhances the stimulation efficiency by reclaiming the charge from electrodes during the cathodic stimulation phase. The system incorporates a D-PS-PWM-QPID controller which can accommodate a broad dynamic range of the output loading conditions, while supporting a fast transient tracking capability. An improved η_{stim} is achieved in various stimulation conditions when compared with the conventional FV-based stimulators. By adjusting C_{IESC} for increasing the charge handling capacity, the proposed topology can be extended to high-density electrode array applications while preserving the energy recycling capability. The stimulation efficiency in various loading conditions is experimentally verified and improved over the conventional FV-supply-based stimulators. ■

Acknowledgments

This work was supported in part by the Hong Kong University of Science and Technology under the RGC research Grant 610412, and by the Research Committee of the University of Macau (MYRG115-FST12-LMK).

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