Process compensated bipolar junction transistor-based CMOS temperature sensor with a ±1.5°C (3σ) batch-to-batch inaccuracy

Dapeng Sun, Tan-Tan Zhang, Man-Kay Law✉, Pui-In Mak and Rui Paulo Martins

A bipolar junction transistor (BJT)-based CMOS temperature sensor exploiting the piecewise BJT process spread compensation property of the base recombination current is proposed to reduce the process variations of the base–emitter voltage (V_{be}). The weighted combinations of different on-chip resistors are explored to minimise their associated process spread. Fabricated in standard 0.18-μm CMOS, the chip prototype occupies an active area of 0.036 mm^2 and draws 3 μA from a 1.2 V supply, with a measured maximum inter-/intra-die variation in V_{be} of <1.5 mV from −40 to 125°C from two batches. Using the measured V_{be}, ΔV_{be} and the first-batch-only calibration parameters, the chip prototype demonstrates an untrimmed batch-to-batch inaccuracy of ± 1.5°C (3σ) within the same temperature range (24 samples from 2 batches).

Introduction: CMOS temperature sensors exhibit great potential for various emerging applications, such as smart home and clinical monitoring. The popular bipolar junction transistor (BJT)-based temperature sensors suffer from process variation in the saturation current I_s due to the non-uniform doping concentration [1]. It is challenging to tackle the inter/intra-die variations for high sensing accuracy without costly trimming process. By exploiting the base recombination current compensation for reducing the I_s and V_{be} spread in [2, 3], this work proposes a process compensated temperature sensor with a measured V_{be} standard deviation (STD) reduction at room temperature from 3.24 mV (15 standalone BJT samples from one batch) to 1.1 mV (24 samples from 2 batches, 12 samples each). Measurement results also show that a batch-to-batch temperature sensing accuracy of ± 1.5°C (3σ) from −40 to 125°C can be achieved using the extracted V_{be}, ΔV_{be} and the first-batch-only calibration parameters.

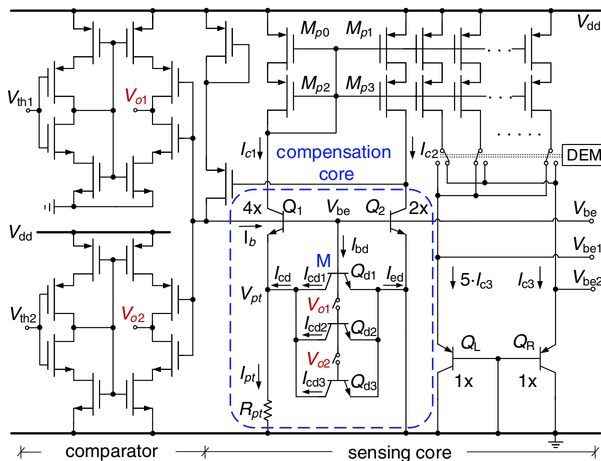

Fig. 1 *Schematic diagram of proposed temperature sensor*

Temperature sensor implementation: Fig. 1 shows the schematic diagram of the proposed temperature sensor. We harness the negative correlation between the base recombination current of a BJT operating in the saturation region to compensate for the process variation of I_s, which is involved in the collector current I_{cd} in Fig. 1. Vertical NPNs Q_1 and Q_2 (with an emitter area ratio 4:2) are forward biased via their collectors, and the V_{be} is independent of the forward current gain β_F. To achieve simultaneous optimal compensation for both process and temperature, the composite compensation BJTs Q_{d1-3} biased in the deep saturation region are designed with configurable emitter areas (i.e. 4, 5 and 6 units) for piecewise compensation from −40 to 35, 25 to 95 and 85 to 125°C, respectively. Before compensation, $|\partial V_{be}/\partial I_s| \approx V_T/I_s$[2], where V_T is the thermal voltage. With piecewise compensation, $|\partial V_{be}/\partial I_s|$ becomes

$$\left|\frac{\partial V_{be}}{\partial I_s}\right| \simeq \frac{V_T}{I_s} \cdot \frac{I_{pt}}{I_{pt} + MI_s/\beta_R} \qquad (1)$$

where β_R is the inverse current gain. To alter the value of M, we adopt a process and temperature independent inverter-based comparator [4] as shown in Fig. 1. We obtain the control signals $V_{o1,2}$ by comparing V_{be} with $V_{th1,2}$ (provided externally for flexibility) to change M for different temperature ranges.

Since the process parameters like the base doping concentration can vary with different processes [1], we verify the validity of this approach in various standard CMOS processes, including ST Microelectronics (ST) 65-nm, Austria Microsystems (AMS) 0.18-μm, and GlobalFoundries (GF) 0.18-μm. As shown in Fig. 2, it can be observed that the V_{be} spread can be effectively reduced by 80, 96 and 75% from 250 MC runs, respectively.

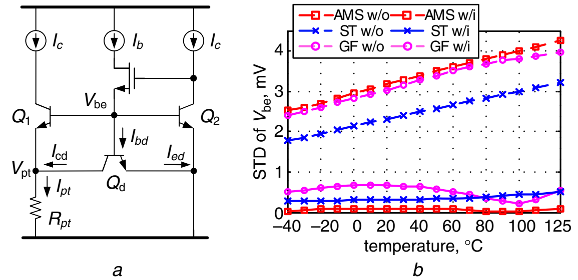

Fig. 2 *Proposed compensation circuit with ideal bias (I_c and I_b)*

a Simplified schematic diagram
b Simulated V_{be} STD with and without compensation over different processes from 250 Monte Carlo runs

Error sources: We identified and analysed different major error sources to improve the achievable accuracy which can be summarised as

- *Comparator offset*: Despite using a common centroid layout, the comparator offsets will lead to temperature hysteresis during the selection of M. Results from 250 MC runs show that the hysteresis voltage in comparator is ~7 mV, corresponding to a ~3.2°C temperature hysteresis and a ± 0.15°C temperature sensing error with the wrong selection of M. To resolve this problem, an overlapping range of 10°C is realised, which can tolerate variations of up to 20 mV between V_{be} and $V_{th1,2}$ in simulation.
- *Bias current variation*: As depicted in Fig. 1, the mismatches between I_{c1-3} can increase the spread of the measured V_{be} and ΔV_{be}. Consequently, we use large transistor sizes (18 μm/9 μm) for M_{p0-3}. Also, all the BJTs are implemented by a careful layout with dummies. Dynamic element matching is applied to achieve an accurate 1:5 ratio in I_{c3} for ΔV_{be}.
- *Resistor spread*: The spread in R_{pt} and its temperature coefficient (i.e. ΔR_{pt}, TC) also introduce variation in $I_{c1,2}$ as well as V_{be}. The induced change in V_{be} is $V_T \cdot \ln(p\Delta R_{pt}/R_{pt})$ with $p = I_{pt}/I_{c1}$. From the simulation, a ± 10% spread in R_{pt} (nominal ≈220 kΩ) corresponds to a ± 2.5 mV spread in V_{be}. This issue is resolved with a weighted combination of various types of resistors [2], effectively reducing the overall simulated resistor spread to 2.28% (~0.5°C).
- *Curvature in V_{be}*: In this work, the residual curvature of ~2 mV from −40 to 125°C can result in a maximum non-linear temperature error of ~0.5°C. The resistor TC spread also induces extra curvature spread in V_{be}. With a resistor first-order TC (i.e. TC1) of 1×10^{-3}, a ± 30% TC1 variation can result in an inter-die V_{be} curvature spread of ± 0.2 mV. Therefore, both positive and negative TC1 resistors are combined to form the composite resistor R_{pt}, reducing the overall TC1 and its spread to 0.015×10^{-3} and 0.005×10^{-3}, respectively.

Measurement results: The chip prototype is fabricated in the GF 0.18-μm standard CMOS process. Fig. 3 shows the chip photo and measurement setup. A total of 24 samples from 2 batches are tested inside the thermal chamber (SU-241, ESPEC). The calibrated Pt-100 thermometer with a calibrated accuracy of ± 0.05°C serves as the temperature reference. Both V_{be} and ΔV_{be} are measured by Agilent 3458A synchronously and post-processed to obtain the instantaneous temperature off-chip. The measured V_{be} STD at room temperature reduces from 3.24 mV (15 standalone BJT samples from one batch) to 1.1 mV (24 samples from 2 batches, 12 samples each). Fig. 4*a* plots the simulated and measured STD of V_{be} due to the variations in BJTs, R_{pt}, and MOSFETs. The maximum measured STD of V_{be} is 1.5 mV over −40

to 125°C. Fig. 4*b* shows the histogram of the simulated V_{be} variation at 25°C, showing that variations of R_{pt} and MOSFETs induce extra STDs of 0.5 and 0.2 mV on V_{be}, respectively.

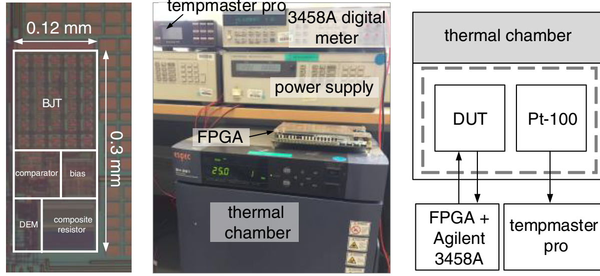

Fig. 3 *Chip micrograph (left) and measurement setup (right)*

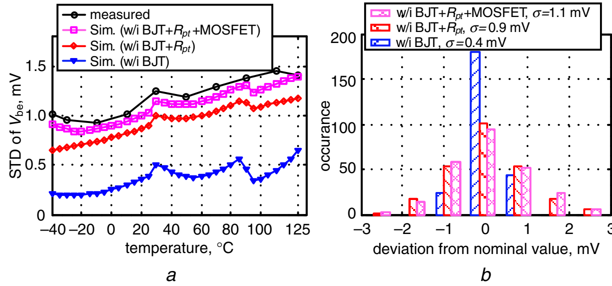

Fig. 4 *Experimental results for the proposed circuit*

a Measured and simulated STD of V_{be} at different temperatures
b Simulated histogram of V_{be} deviation at 25°C

To determine the sensing error, the ratio $X = \Delta V_{be}/V_{be}$ is utilised to extract the temperature output $D_{out}(T)$. We directly apply piecewise second-order polynomial fit to X, i.e. $D_{out} = C_1 \cdot X^2 + C_2 \cdot X + C_3$. The calibration parameters C_1, C_2, and C_3 are extracted from 12 samples within the first batch. Fig. 5 shows the measured temperature errors of the proposed temperature sensor, demonstrating inter/intra-die spread and sensing error reduction using the proposed piecewise process spread compensation method. Within the overlapping ranges from 25 to 35°C and 85 to 95°C, two sets of calibration parameters from adjacent ranges are used to determine the comparator offsets induced sensing error (±0.2°C). Without additional trimming, a measured batch-to-batch inaccuracy of ± 1.5°C (3σ) is obtained over the range from −40 to 125°C (lower temperature limited by the temperature chamber). Table 1 lists the performance comparisons with prior BJT-based untrimmed works. Compared with [5], this work exhibits 2× better untrimmed accuracy benefited from the proposed piecewise compensation technique. Although the authors of [6, 7] achieve higher accuracies, the results are from individual batch calibration. Overall, this work achieves accurate wide range temperature sensing using only calibration parameters from one batch.

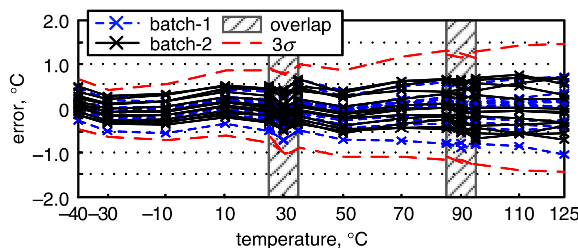

Fig. 5 *Measured 3σ temperature errors (24 samples from 2 batches). The shaded area indicates the overlap regions of 10°C each*

Table 1: Comparison with BJT-based untrimmed sensors

Parameter	**This work**	[6] EL'14	[5] T-VLSI'17	[7] EL'18
Type	**BJT**	BJT	BJT	BJT
Process (µm)	**0.18**	0.18	0.065	0.13
3σ error (°C)	**± 1.5**	± 0.7	± 3	± 1.1
No. of Batches	**2**	1	1	1
Calibration	**one-batch[a]**	Individual batch[b]	Individual batch[b]	Individual batch[b]
Samples	**24**	25	12	14
Range (°C)	**−40~125**	0~125	25~100	−10~100
Area (mm^2)	**0.036**	0.048	0.009	0.073
Supply (V)	**1.2**	1~1.5	N/R	1.8~3.5
Power (µW)	**3.6**	22	200	30.6
Output	**Voltage**	Voltage	Voltage	Digital

[a]All batches use the same calibration parameters from one-batch.
[b]Each batch uses the calibration parameters from individual batch.

Conclusion: A process compensated BJT-based temperature sensor has been implemented in 0.18-µm CMOS. Inter-/intra-die variations in V_{be} over a wide temperature range are effectively reduced with the proposed piecewise compensation technique. Measurement from two batches demonstrates a single-batch calibrated inaccuracy of ± 1.5°C (±3σ) from −40 to 125°C, presenting a potential low-cost CMOS temperature sensor solution.

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One or more of the Figures in this Letter are available in colour online.

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