0.013 mm^2, kHz-to-GHz-bandwidth, third-order all-pole lowpass filter with 0.52-to-1.11 pW/pole/Hz efficiency

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A third-order all-pole analogue lowpass filter (LPF) with kHz-to-GHz bandwidth tunability is proposed. It embeds a current-reuse active inductor into a current-scalable source follower to realise three concurrently tunable poles in a single branch. The LPF fabricated in 0.18 µm CMOS measures a tunable -3 dB cutoff from 0.8 kHz to 1.2 GHz, under a scalable power of 1.25 nW to 4.01 mW. Owing to no tuning capacitor, the die area is extremely compact (0.013 mm^2) and the achieved filter efficiency is 0.52 to 1.11 pW/pole/Hz.

Introduction: Continuous-time analogue lowpass filters (LPFs) with high scalability on bandwidth can find extensive applications in multi-standard wireless transceivers as they can enable flexible band selection (e.g. VHF and UHF bands in TV tuners [1]) or channel selection from kHz (e.g. GSM) to GHz (e.g. IEEE 802.15.3c) ranges. Among the existing analogue LPF topologies, the $g_m - C$ solution was most common in GHz-range filtering, as they can leverage in a better manner the power and area efficiencies than the others, such as the active-RC. Yet, for all the cases, the tuning of the bandwidth still relies on capacitor banks, which is an area-hungry option (e.g. 0.9 mm^2 in [1]). Furthermore, it is highly desirable to scale the power according to the required bandwidth for a better system efficiency. To achieve such goals, while ensuring small die area and power, a single-branch third-order all-pole LPF with a continuous and wide-scalable bandwidth with power is developed. It functions as a third-order source follower (SF)-based LPF, with an embedded active inductor (AI). The circuit details are presented next.

Single-branch third-order all-pole LPF: The schematic is depicted in Fig. 1. Its basis is a differential NMOS-only SF, where the transconductance of $M_{1p,n}$ (g_{mM1}) and $C_1/2$ contribute one real pole that is linearly tunable by the bias current I_{tune}. To extend the number of poles in one branch, we insert an AI into the SF. By adding the capacitor $C_3/2$, a third-order 'capacitor–inductor–capacitor' ladder is synthesised vertically in a current-reused branch, showing high stopband attenuation. More importantly, this LPF topology ensures that all the devices share the same I_{tune} for consistent scaling of all the poles.

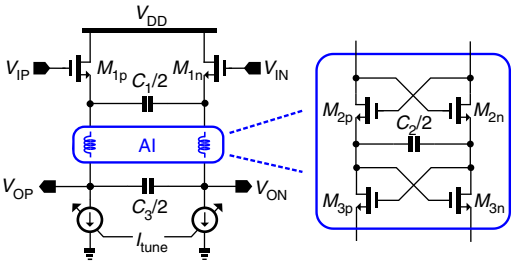

Fig. 1 *Proposed bandwidth-tunable third-order LPF. No tuning capacitor is entailed, as three poles can be scaled concurrently via I_{tune}*

The AI involves only two pairs of cross-diode-connected metal oxide semiconductor field effect transistors (MOSFETs) ($M_{2p,n}$ and $M_{3p,n}$) in cascode, and one untuned capacitor $C_2/2$. Thus, the parasitic effect is low, and it can be stacked with other circuitry for current reuse. The AI uses two positive-feedback impedance converters for admittance transformation from capacitive into inductive. Fig. 2 depicts the half-circuit equivalent of the LPF. With circuit analysis, the equivalent circuit of the AI can be obtained, where $M_{2p,n}$ and $M_{3p,n}$ are all equally sized for the same transconductance ($g_{m2} = g_{m3} = g_{mL}$) and output resistance ($r_{o2} = r_{o3} = r_{oL}$). On proper sizing, $g_{mL}^2 \gg 1/r_{oL}^2$ can be set to obtain the simplified expression of each component given in Fig. 2. One can note that the complex poles can be tuned with g_{mL} linearly since $L_{act} \propto 1/g_{mL}^2$. Hence, together with the real pole of the SF core ($M_{1p,n}$ and C_1), a third-order all-pole transfer function can be achieved. The bandwidth is easily scalable by I_{tune}, avoiding any tuning capacitors that degrade the area efficiency. According to R_s and L_{act}, the quality factor ($Q_{L_{act}}$) of the AI is $Q_{L_{act}} = \omega r_{oL} C_2/2$, which is, to the first order, independent of g_{mL}.

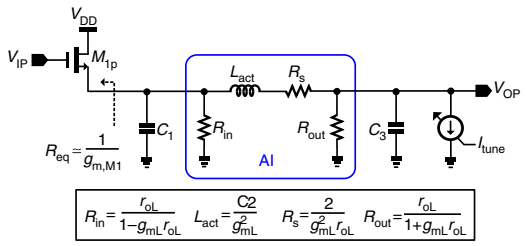

Fig. 2 *Half-circuit equivalent of proposed LPF*

For simplicity in deducing the filter transfer function, the parasitic capacitances and output resistance of all the MOSFETs are ignored. The parameters in Fig. 2 are substituted by $R_s = 0$, $R_{in} \simeq -1/g_{mL}$ and $R_{out} \simeq 1/g_{mL}$. The transfer function of this LPF is written as

$$H(s) = A_{DC} \frac{1}{s^3 a_3 + s^2 a_2 + s a_1 + 1} \quad (1)$$

$$\text{where } A_{DC} = 1 \; a_3 = \frac{C_2}{g_{mL}^2} \frac{C_1 C_3}{g_{m1}}$$

$$a_2 = \frac{C_2}{g_{mL}^2} \frac{g_{mL} C_1 + (g_{m1} - g_{mL}) C_3}{g_{m1}}$$

$$a_1 = \frac{C_2}{g_{mL}^2} \frac{g_{mL}(g_{m1} - g_{mL}) C_2 + (C_1 + C_3) g_{mL}^2}{g_{m1} C_2}$$

Of course, the DC gain (A_{DC}) will be lower than unity if the output conductance of each MOSFET is accounted for. By conducting 100 × Monte Carlo simulations, the variation of bandwidth with respect to process variation and mismatches can be assessed (Fig. 3), where the -3 dB cutoff frequency ($f_{-3\,dB}$) is set at 1 kHz, 100 kHz, 10 MHz and 1 GHz. The standard deviation of all the cases is maximally 1.26% of their mean values.

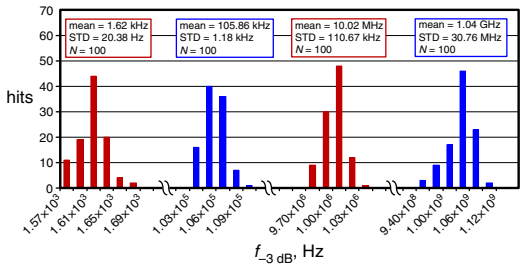

Fig. 3 *100 × Monte Carlo simulations of $f_{-3\,dB}$ variation when set at 1 kHz, 100 kHz, 10 MHz and 1 GHz*

Experimental results: The proposed LPF was fabricated in a 0.18 µm CMOS technology (Fig. 4). The die size is 0.013 mm^2. All the MOSFETs were sized with $L = 0.5$ µm for a larger output resistance, improving the DC gain, linearity and accuracy of the frequency response. The sizes of the key components are: $M_{1p,n} = 160/0.5$, $M_{2p} = M_{3p,n} = 164/0.5$, $C_1 = 0.64$ pF, $C_2 = 0.69$ pF and $C_3 = 0.54$ pF. The selected V_{DD} is 3 V to extend the bandwidth tunability as the device overdrive voltages will vary with the bias current. The measured f_{-3B} is tuned from 0.8 kHz to 1.2 GHz (Fig. 5) with the power rises from 1.25 nW to 4.01 mW. The passband gain varies between -5 and -4 dB.

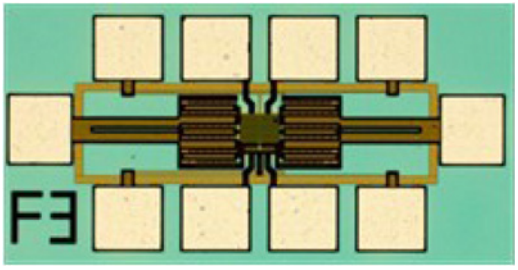

Fig. 4 *Chip photo of proposed LPF*

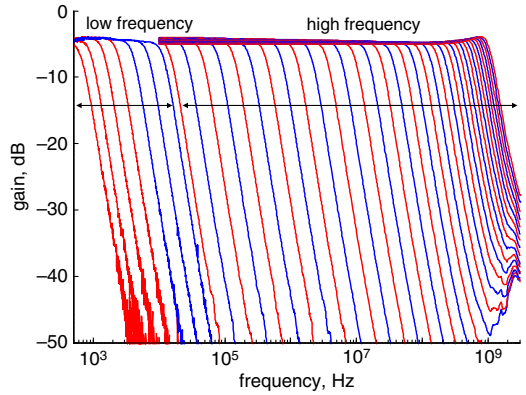

Fig. 5 *Measured kHz-to-GHz gain response with two equipments for low (< 10 kHz) and high (> 10 kHz) frequency ranges*

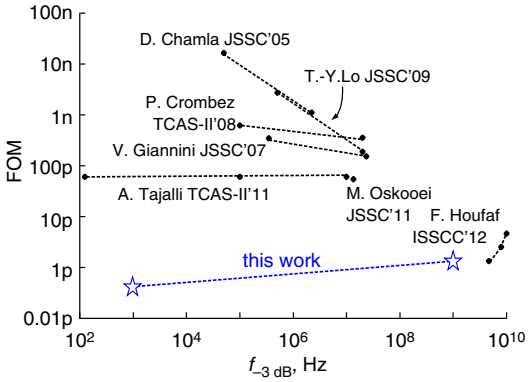

Fig. 6 *Benchmark with prior art*

Table 1: Performance summary

Parameters	This work	ISSCC 2012 [2]
Order, type	Third-order, Butterworth	Third-order, Chebychev-I
$f_{-3\ dB}$ tuning	Current ↔ bandwidth	Voltage ↔ bandwidth
$f_{-3\ dB}$ range	0.8 kHz to 1.2 GHz	0.9–10 GHz
$f_{-3\ dB}$ tunability ($f_{-3\ dB,max}/f_{-3\ dB,min}$)	1 500 000	16.7
Power at $f_{-3\ dB}$	1.25 nW at 0.8 kHz	19 mW at 4.7 GHz
	4.01 mW at 1.2 GHz	140 mW at 10 GHz
DC gain	− 5 to − 4 dB	1.3–2.7 dB
$IIP3_{in\text{-}band}$	+ 12 to + 24 dBm	+ 7 to + 8 dBm
IRN at $f_{-3\ dB}$	5.2 $\mu V_{rms}/\sqrt{Hz}$ at 0.8 kHz	6.61 $nV_{rms}/\sqrt{Hz}$ at 4.7 GHz
	3.9 $nV_{rms}/\sqrt{Hz}$ at 1.2 GHz	5.02 $nV_{rms}/\sqrt{Hz}$ at 10 GHz
Die area	0.013 mm^2	0.01 mm^2
V_{DD}	3 V	1–1.4 V (to tune $f_{-3\ dB}$)
Technology	0.18 µm CMOS	65 nm CMOS
FOM = power/($f_{-3\ dB}$ × number of poles)	0.52 pW/pole/Hz at 0.8 kHz	1.34 pW/pole/Hz at 4.7 GHz
	1.11 pW/pole/Hz at 1.2 GHz	4.66 pW/pole/Hz at 10 GHz

The chip summary and performance benchmark are given in Table 1. The $f_{-3\ dB}$ tunability is significantly wider, but due to the parasitic limit of the employed 0.18 µm CMOS technology, the $f_{-3\ dB}$ is not as high as [2] that is in the 65 nm CMOS technology. According to the figure of merit (FOM) = power/($f_{-3\ dB}$ × number of poles) [2], this work favourably compares with the prior art (Fig. 6) over a wide range of bandwidths.

Conclusion: We have proposed a continuous-time single-branch third-order LPF suitable for flexible band/channel selection from kHz-to-GHz ranges in multi-standard wireless transceivers. The achieved cutoff frequency experimentally verified in the 0.18 µm CMOS technology ranges from 0.8 kHz to 1.2 GHz, with the required power scales up from 1.25 nW to 4.01 mW. The filter efficiency is 0.52 to 1.11 pW/pole/Hz.

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One or more of the Figures in this Letter are available in colour online.

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