A 76.6-dB-SNDR 50-MHz-BW 29.2-mW Multi-Bit CT Sturdy MASH With DAC Non-Linearity Tolerance

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***Abstract*— This article presents a dual-loop noise-coupling (NC)-assisted continuous-time (CT) sturdy multistage noise-shaping (SMASH) ΔΣ modulator (DSM), employing 1.5-bit/4-bit quantizers. The proposed SMASH can equivalently work as an overall fourth-order DSM with 4-bit internal quantization. The NC applied in this CT SMASH DSM whitens the 1.5-bit quantization noise (QN) and further reduces its in-band tone power, while a finite-impulse response (FIR) filter integrated into the outermost feedback path suppresses the out-of-band (OOB) noise power of the multibit digital-to-analog converter (DAC) input. Together, they avoid any linearization technique for the multibit DAC. Sampled at 1.2 GHz, the 28-nm CMOS experimental prototype measures a signal-to-noise-and-distortion ratio (SNDR) of 76.6 dB and a spurious-free dynamic range (SFDR) of 87.9 dB over a 50-MHz bandwidth (BW), consuming 29.2 mW from 1.2-V/1.5-V supplies and occupying an active area of 0.085 mm^2. It exhibits a Schreier figure-of-merit (FoM) (SNDR) of 168.9 dB.**

***Index Terms*— Analog-to-digital converter (ADC), continuous time (CT), digital-to-analog converter (DAC) linearization, excess loop delay (ELD) compensation, filter, finite-impulse response (FIR), multibit quantization, noise coupling (NC), sturdy multistage noise-shaping (SMASH), successive-approximation register (SAR).**

I. Introduction

NOWDAYS, wireless communication applications are highly developed, thus setting stringent design specifications to the analog-to-digital converters (ADCs). For instance, the long-term evolution advanced (LTE-A) direct conversion receiver requires at least 50-MHz signal bandwidth (BW) with a minimum analog baseband complexity [1]. Driven by the wide cellular BW, continuous-time (CT) ΔΣ modulators (DSM) [1]–[17] have been developed comprehensively owing to its decent power efficiency, resistive input impedance, and inherent signal filtering features. Generally, with a demanding signal BW, the oversampling ratio (OSR) used for a CT DSM is restrained. To achieve the desired resolution while keeping high power efficiency, a CT DSM needs to put efforts into the following two directions together.

First, the wideband CT DSM aims to achieve an aggressive noise-shaping. However, a higher order DSM suffers from stability issues in the single-loop topology. Instead, the multistage noise-shaping (MASH) [18] architecture could be used to overcome the instability issue. Nevertheless, noise leakage is detrimental in CT MASH topologies [1], [8], [19]–[21] since the resistor and capacitor (*RC*) products determine the scaling coefficients. To reduce the noise leakage, [1] dissipates a large amount of power consumption. Alternatively, the sturdy MASH (SMASH) [6], [22] topology exhibits high potential as it has relaxed matching requirements to eliminate the quantization noise (QN) of preceding stages.

Second, a multibit quantizer is often employed to improve the DSM resolution, to relax the dynamic requirements of the loop filter, to enhance stability, and to increase the maximum stable amplitude (MSA). However, a multibit feedback (FB) digital-to-analog converter (DAC) is non-linear due to the element mismatch, dictating a DAC linearization technique. The DAC linearization can be performed by using either the dynamic element matching (DEM) or calibrations. In wideband DSMs with multi-gigahertz sampling frequencies, DEM becomes less effective due to the low OSR [4], while the associated delays impose challenging to handle as they add to excess loop delay (ELD). Thus, employing DEM is neither power nor speed friendly [5] and most recent wideband multibit DSMs did not use DEM. Instead, DAC calibrations have been commonly performed to address the DAC non-linearity issue by using cross correlation [3], [4], digital noise-shaping [5], sine-wave fitting [9], and current copier [6]. Nevertheless, the on-chip DAC calibrations as, e.g., employed in [4] and [6] require significant additional power and area consumptions. Moreover, off-chip DAC foreground calibration [3], [5], [9] is not able to track the current source

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mismatch error over temperature and supply variations, which is obviously not desirable in a high-performance CT DSM.

To address both challenges, aggressive noise-shaping with high order and multibit internal quantization operating at a low OSR, a dual-stage noise-coupling (NC)-assisted CT SMASH DSM using 1.5-bit/4-bit quantizers in both stages [16] is presented in this article. By effectively eliminating 1.5-bit QN from the first stage, the SMASH DSM enjoys all benefits provided by multibit operation of a DSM. The NC technique [23] applied in the SMASH not only improves the noise-shaping order by one but also works as dithering for the highly tonal 1.5-bit QN and further reduces its in-band tone power. Meanwhile, a finite-impulse response (FIR) filter [7], [10], [24] is incorporated into the outermost FB path to reduce the out-of-band (OOB) noise power for the nonlinear DAC input to alleviate QN folding. Both features significantly mitigate the requirement for a highly linear multibit DAC, thus avoiding any DAC linearization in this article while achieving the state-of-the-art (SoA) linearity.

This article is organized as follows. Section II introduces the SMASH topology in detail and its design considerations. Section III presents the proposed SMASH architecture. Section IV covers the prototype modulator circuit design, followed by the measurement results included in Section V. Finally, Section VI concludes this article.

II. SMASH Design Considerations

A. Dual-Loop MASH and SMASH

Fig. 1 shows a basic dual-loop MASH architecture. Two independent low-order single-loop DSMs are cascaded to address the stability issue associated with higher order noise-shaping. The QN of the first loop E_{q1} is extracted and passed to the input of the second loop. In the backend, the digital outputs are combined using a digital cancellation logic to produce the final output, which is given by

$$V_{\text{MASH}} = \text{STF}_{1a}\text{STF}_{2d}V_i + (\text{NTF}_{1a}\text{STF}_{2d} - \text{NTF}_{1d}\text{STF}_{2a})E_{q1} - \text{NTF}_{1d}\text{NTF}_{2a}E_{q2} \quad (1)$$

where STF_i, NTF_i, and E_{qi} denote signal and noise transfer functions (NTFs) and quantization errors of the ith loop, respectively, and subscripts "a" and "d" represent analog and digital transfer functions, respectively. As shown in (1), an adequate matching between the analog and digital filters must be satisfied to properly cancel E_{q1}. Apparently, such a matching requirement is critical as the RC values in CT loop filters suffer from process and temperature variations.

To address the stringent matching existing in CT MASH topologies, the SMASH topology was first proposed in a discrete-time (DT) implementation in [22] and further developed as CT implementation in [6]. Fig. 2 depicts a dual-loop SMASH architecture, which is modified from the MASH. The digital filters are removed while the digital outputs directly perform the subtraction to generate the final output. Moreover, the global FB is given from the final output to the first loop such that E_{q1} and the output of the second loop are further

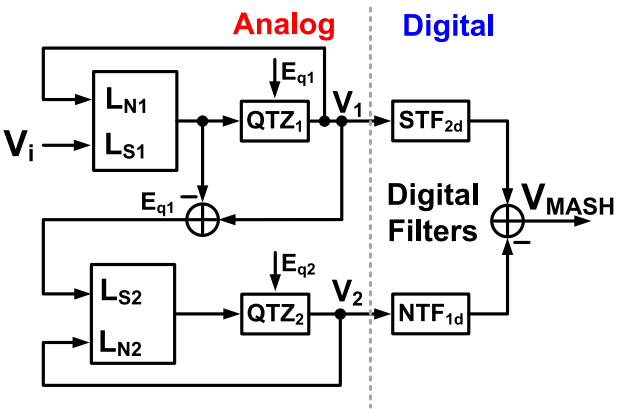

Fig. 1. Block diagram of a traditional dual-loop MASH.

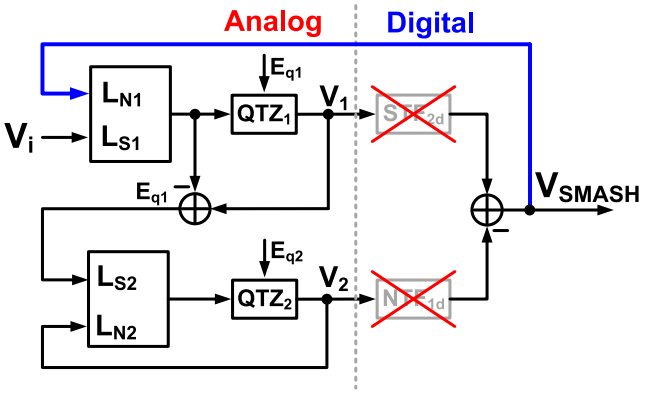

Fig. 2. Block diagram of a general dual-loop SMASH.

shaped by the NTF_1. As a result, the overall output is given by

$$V_{\text{SMASH}} = \text{STF}_{1a}V_i + (1 - \text{STF}_{2a})\text{NTF}_{1a}E_{q1} - \text{NTF}_{1a}\text{NTF}_{2a}E_{q2} \quad (2)$$

As stated in (2), $\text{STF}_2 = 1$ assures that the QN from the first loop can be eliminated. Obviously, such a matching requirement is much more relaxed when compared with the digital–analog filters matching in the MASH topology.

B. Signal Transfer Function of the Second Loop

In the SMASH DSM, the second stage not only improves the noise-shaping order further for the QN but also needs to implement a unity-gain signal transfer function (STF) to effectively eliminate the QN from the first loop. For a common second loop with a given order (at least one) in the SMASH DSM, it is obviously impossible to implement an STF keeping a unity-gain over the whole Nyquist band. Instead, the overall signal-to-quantization-noise ratio (SQNR) would not be affected if the in-band STF_2 is delay-less unity-gain [6]. Therefore, it is desired to select an appropriate topology as the second loop to minimize the in-band delay and keep the gain as close to unity as possible in the band of interest. To achieve such a goal, Yoon *et al.* [6] employed the first-order topology with an input feedforward (FF) as the second loop. Nevertheless, the QN E_{q1} at OOB frequencies cannot be eliminated completely with this architecture. The leaked OOB QN E_{q1} manifests itself in the time domain with increasing

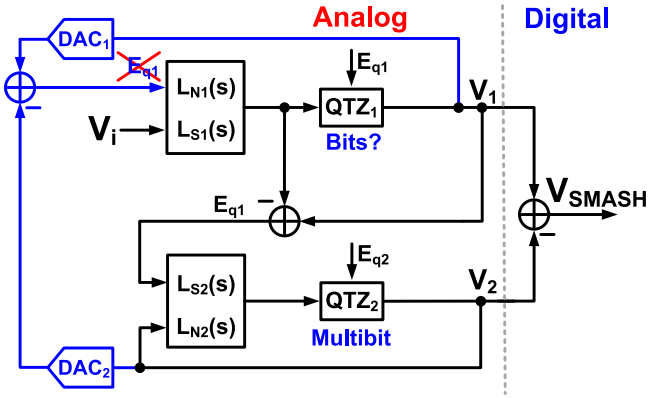

Fig. 3. Practical implementation of the CT dual-loop SMASH.

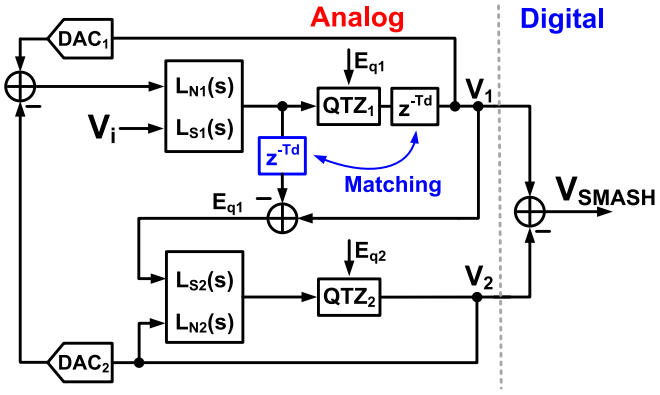

Fig. 4. Extraction of QN E_{q1} in CT SMASH DSM.

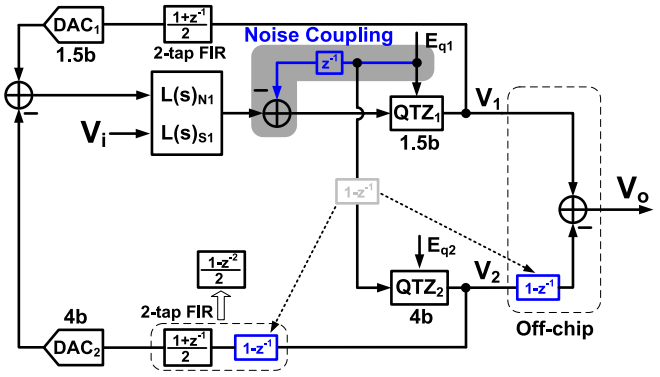

Fig. 5. Block diagram of the proposed CT dual-loop SMASH.

the output swing of the integrators in the first stage. In [6], such OOB noise leakage can be well tolerated since the first stage also employs a 4-bit quantizer as in the second stage.

On the other hand, by removing any integrators in the second stage, a zeroth-order topology can be employed as the second loop to implement an almost perfect unity-gain STF over the whole Nyquist band. However, this would disadvantageously not contribute any further noise-shaping order for the QN from the second loop.

C. Considerations on Internal Quantization in SMASH DSM

In practice, to get rid of the delay of the digital adder inside the FB loop, as shown in Fig. 3, the subtraction is implemented through DAC_1 and DAC_2 in parallel to the front end. After the analog subtraction, E_{q1} is removed inside the first loop filter. As a result, the MSA and the OOB gain (OBG) of the SMASH DSM are merely determined by the number of bits of the quantizer used in the second loop. Since the OSR is low for wideband applications, multibit quantization is advantageously used for the second quantizer to achieve large MSA and OBG. Theoretically, the resolution of the first stage quantizer does not impact the resolution of the SMASH. Still, the previous CT SMASH implementation as in [6] also applied multibit quantization for the first quantizer. A multibit quantizer used in the first stage allows introducing a larger inter-stage gain, which improves the SQNR further without saturating the second loop, which is in contrast to using a single-bit quantization in the first stage. Nonetheless, multibit quantization in the first stage also results in using a multibit DAC that is non-linear owing to element mismatch, and whose non-linearity directly deteriorates the DSM performance. In the MASH topology, it is known that using single-bit quantization in the first and multibit in the later stages is advantageous for DAC linearity. This is because the single-bit DAC would be intrinsically linear, while the multibit-DAC non-linearity in the higher stages would be suppressed in the digital cancellation logic. Nevertheless, the QN leakage from the first stage would be related to single-bit, which is much worse than multibit QN leakage. This leakage argument is still true for SMASHs. More unfortunately, in contrast to the MASH, since DAC_2 is fed back to the most sensitive input node of the overall DSM, using a multibit DAC_2 would anyhow need DAC linearization. This occurs because the single-bit QN E_{q1} is highly tonal (will be demonstrated in Fig. 7), rather than an approximate white noise as the multibit QN. In the SMASH, such highly tonal signal E_{q1} would go through the nonlinear DAC_2 located in the sensitive input front end, thus introducing harmonic distortions (HDs). Moreover, the large OOB QN of the second stage is mixed by the non-linearity of DAC_2 and would thereby increase the in-band noise floor. Thereby, the linearization of DAC_2 is compulsory for a multibit quantization in the second stage of the SMASH. Thus, combining an intrinsically linear single-bit quantization in the first with a multibit quantization in the second stage is not advantageous in the SMASH topology.

This issue is consequently seen in the SoA SMASH DSMs and it will be addressed in this article.

D. QN Extraction in CT SMASH

Another problem exists in the CT implementation of SMASH DSM regarding the QN extraction from the first stage. The first quantizer intrinsically comes with a propagation delay. With a CT input and a delayed DT output for the quantizer, the correct extraction of the QN E_{q1} from the first quantizer becomes problematic. Straightforwardly, as shown in Fig. 4, the same delay must be generated for the CT input of the first quantizer such that E_{q1} can be correctly extracted. Theoretically, a sample and hold circuitry can be employed

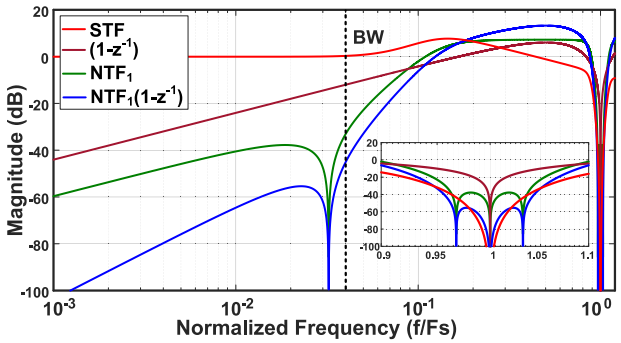

Fig. 6. Magnitude response of STF and NTF of the proposed SMASH from behavioral simulations.

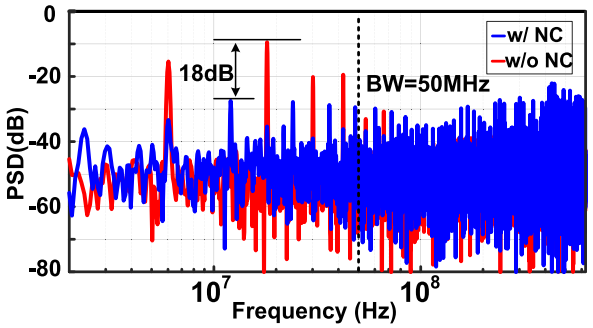

Fig. 7. Simulated E_{q1} FFT spectrum of the cases with and without NC.

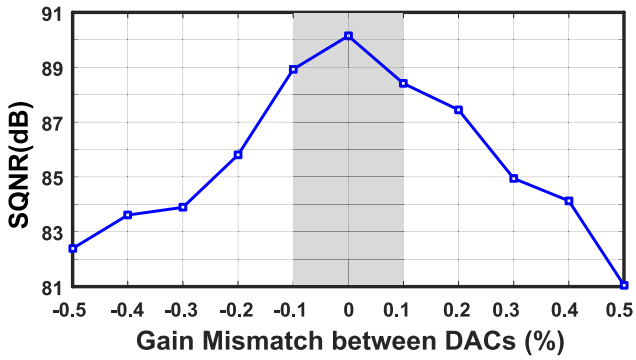

Fig. 8. Simulated SQNR versus the mismatch between outermost DACs.

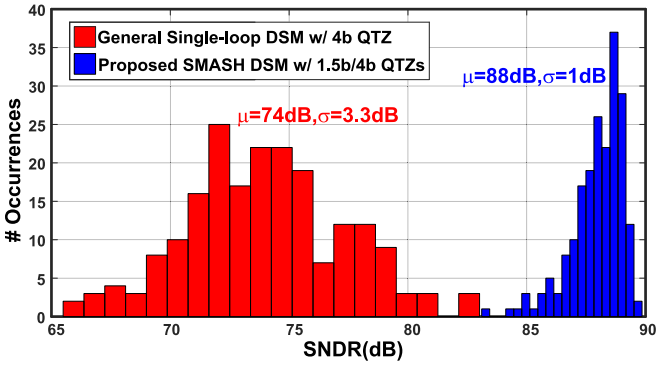

Fig. 9. Monte Carlo simulation with 0.2% mismatch for outermost DACs.

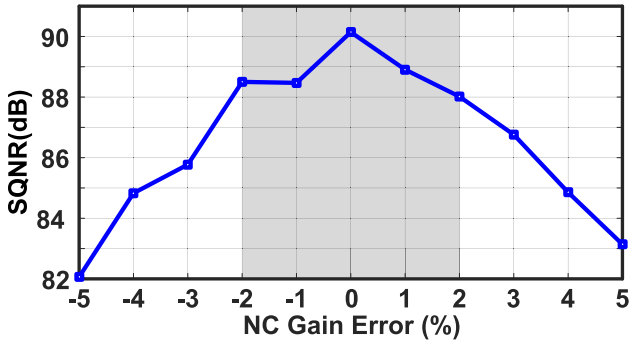

Fig. 10. Simulated SQNR versus the NC gain error.

to generate such a delay. However, the sample and the hold topology would process a full-scale signal, which comes with a high power consumption at the intended multi-gigahertz clock frequency. Instead, Yoon *et al.* [6] proposed to utilize an *RC* low-pass filter (LPF) to generate such a delay, which is feasible owing to the oversampling property. However, since the LPF attenuates the high-frequency component, the discrepancy between the LPF output and the first quantizer output results in a second peaking in the STF [6].

E. Design Goals of This Article

After reviewing the SMASH DSM and its design considerations, the design goals of this article are given as follows. We would like to present a more robust CT SMASH DSM in terms of the QN extraction as well as its cancellation. Also, we would like to employ a multibit quantization to gain good stability, relaxed dynamic requirements of the loop filter, large MSA and OBG while achieving high linearity, but avoiding any linearization technique for all multibit DACs to reduce power and area consumptions.

III. Proposed SMASH DSM

A. Overall Architecture

As shown in Fig. 5, the overall proposed SMASH DSM employs a basic dual-loop 3-0 architecture using 1.5-bit/4-bit quantizers in the first and second loops, respectively. As a result, effective 4-bit QN remains to be processed inside the loop filter of the first stage, thus obtaining decent stability, large MSA, and OBG. Moreover, a first-order NC is applied in the first loop. Note that since the QN E_{q1} is injected back into the first 1.5-bit quantizer, the MSA of the modulator is reduced. However, since the NC is only first-order, such loss is acceptable, which is also verified in the experimental result. It stays true because the non-overload input range of one quantizer is FS + Δ [18], where FS is the full scale of the quantizer and Δ is the LSB size. It is worth noting that the non-overload input range of the quantizer includes Δ, which could just accommodate the first-order injected QN whose peak-to-peak swing is Δ. In other words, although the peak-to-peak swing of the injected 1.5-bit QN seems large, the tolerance to saturation of 1.5-bit quantizer is also large, which inversely cancels out the injected effect owing to the first-order NC. To account for the applied NC in the first loop and effectively eliminate the first-order noise-shaped E_{q1},

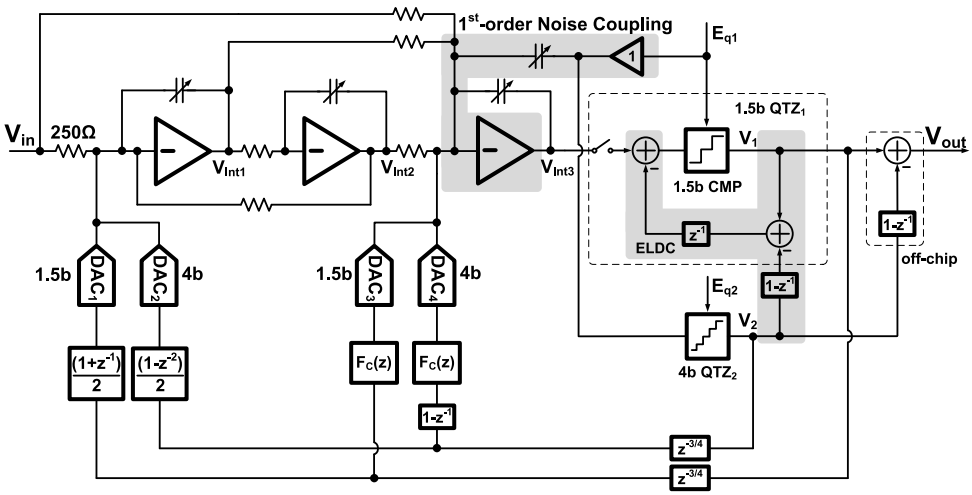

Fig. 11. Overall schematic of the proposed CT SMASH DSM.

a corresponding filter $(1 - z^{-1})$ must be implemented after the extraction of E_{q1}. As depicted in Fig. 5, we move this filter from the input (analog-domain) of the second stage to its output (digital domain), which allows implementing it more accurately and further increase one noise-shaping order for E_{q2}. Although the digital filter $(1 - z^{-1})$ is integrated into the output of the second stage, the feature of the proposed SMASH is still the same with a conventional one. The QN E_{q1} is extracted from the 1.5-bit SAR into the second stage of the SMASH. In the first stage, E_{q1} is implicitly high-pass filtered by the NC branch. Thus, by choosing a proper unity-gain STF_2, E_{q1}—after being explicitly high-pass filtered by the digital filter $(1-z^{-1})$—can be eliminated. In the back end, the two digital outputs V_1 and V_2 are combined to generate the final output V_O. All outputs V_1, V_2, and V_O are given by, respectively,

$$V_1 = \text{STF}_1 V_i + \text{NTF}_1(1 - z^{-1})E_{q1} \tag{3}$$

$$V_2 = \text{STF}_2 E_{q1} + E_{q2} \tag{4}$$

$$V_O = \text{STF}_1 V_i + (1 - \text{STF}_2)\text{NTF}_1(1 - z^{-1})E_{q1} - \text{NTF}_1(1 - z^{-1})E_{q2}. \tag{5}$$

As observed in (5), the QN E_{q2} would be finally suppressed by the combination of the NTF_1 (implemented by the first stage) and $(1 - z^{-1})$ that is implemented through the digital filter in the second stage. Fig. 6 shows the simulated STF magnitude response of the proposed SMASH DSM. Due to the use of FF paths (illustrated in Fig. 11), there exists a peaking in the STF with a maximum gain of 7.6 dB. Such peaking may be problematic with the presence of the OOB blockers in wireless communication applications. Nevertheless, this article can distribute input paths [12] to maximumly flatten the STF around the peaking and further employ a simple first-order filter that is integrated with the transimpedance amplifier that drives the ADC in the receiver application [17] to suppress the remaining STF peaking if necessary. Besides, as foreseen, the CT SMASH DSM could provide at least 50-dB anti-aliasing around the sampling frequency before the input signal being sampled by the quantizer.

B. Noise Leakage Reduction

Due to the use of the 1.5-bit quantizer in the first loop, in the case of an imperfect in-band cancellation, the 1.5-bit QN E_{q1} would leak to the final output, thus deteriorating the final performance. Besides, an incomplete cancellation of OOB 1.5-bit QN would significantly increase the output swing of the integrators in the first stage, thus posing challenges for high linearity. To alleviate both concerns, a unity-gain STF_2 must be achieved as accurately as possible over the whole Nyquist range. Therefore, instead of using a first-order FF topology as in [6], as shown in Fig. 5, a zeroth-order topology is selected for the second loop in this article. This effectively makes the proposed SMASH DSM a two-stage architecture where the first stage provides the noise-shaping order, while the second stage determines the effective quantization bitwidth. Therefore, it allows multi-bit loop-filter scaling in the first stage, which yields larger MSA and OBG, reduced dynamic loop-filter requirements, etc.

C. Multibit DAC Non-Linearity Mitigation

In the proposed SMASH DSM, by using the 1.5-bit/4-bit combination for both quantizers, the 1.5-bit DAC_1 would be intrinsically linear, while the 4-bit DAC_2 is unavoidably nonlinear. It is noteworthy that using NC not only helps to increase the noise-shaping order but also works as dithering [23] for the highly tonal 1.5-bit QN E_{q1}, thus significantly reducing its idle tones and harmonic spurs. Here, we study the fast Fourier transform (FFT) spectrum of 1.5-bit QN E_{q1} through the simulations in the behavioral model. Note that the input is a sinusoid wave with a zero dc bias level. As observed in Fig. 7, owing to the dithering introduced by the NC, the 1.5-bit QN E_{q1} becomes less tonal compared with the case without the NC. The highest tone of power gets reduced by as much as 18 dB. In addition, after the dithering, the 1.5-bit E_{q1} would be shaped by the digital filter $(1-z^{-1})$, which replicates the NC in the first stage. Then, the in-band tonal and noise power of the 1.5-bit E_{q1} would be further suppressed before it goes through the nonlinear 4-bit DAC_2.

As a result, both features significantly alleviate the linearity requirement on the outermost 4-bit DAC_2.

However, with the presence of the 4-bit DAC_2 mismatch and non-linearity, due to the cross-modulation of large OOB QN, the in-band noise floor would still get increased, thus degrading the obtained SNR. To mitigate this, a two-tap FIR LPF is inserted before the nonlinear 4-bit DAC_2 to reduce the OOB noise power. Advantageously, the two-tap FIR LPF can be merged with the digital filter $(1 - z^{-1})$ to the result $(1 - z^{-2})/2$, without requiring additional hardware, as shown in Fig. 5. The same two-tap FIR LPF is also applied in the 1.5-bit DAC FB path of the first stage, thus matching the two outermost DAC paths for E_{q1} cancellation. Meanwhile, applying a two-tap FIR LPF would reduce the jitter sensitivity of the outermost DACs. In the behavioral simulation, with applying a 0.05% of a clock period as rms clock jitter for the outermost FB DACs, the in-band noise power stays around −90-dB FS, which almost does not influence the desired resolution. With a sampling frequency of 1.2 GHz in this article, the rms clock jitter requirement corresponds to ≈417 fs, which can be reliably achieved.

Finally, this combination of the NC technique for the 1.5-bit quantizer in the first stage and an FIR LPF allows the proposed SMASH DSM to avoid any linearization technique for the outermost multibit DAC_2 since large in-band tones and large OOB QN are highly suppressed before they are non-linearly processed by the DAC_2.

D. Mismatch Considerations

For the outermost DACs (DAC_1 + DAC_2) in Fig. 5, any gain mismatch between both DACs would result in the leakage of 1.5-bit QN E_{q1}, thus degrading the final signal-to-noise-and-distortion ratio (SNDR), thereby both DACs must share the same DAC slices to minimize their gain mismatch. Fig. 8 shows the matching requirement between the outermost DACs. It is observed that 0.1% gain matching requirement must be obtained to almost keep the ideal SQNR.

Even though the introduced techniques highly alleviate the required DAC non-linearity, still the amount of DAC non-linearity must be investigated, which can be tolerated. Therefore, the achievable SNDR depending on the matching accuracy for the DAC_2 unit cell was determined by running 200 Monte Carlo simulations with a Gaussian distributed random mismatch in MATLAB. As indicated in Fig. 9, the proposed NC and FIR-filtering SMASH can achieve a mean SNDR of 88 dB with a relative mismatch as large as 0.2% for the outermost DACs. Note that the DAC unit relative mismatch in the outermost DACs (DAC_1 + DAC_2) not only introduces HDs but also generates a gain error between DAC_1 and DAC_2in the proposed SMASH DSM. Such a gain error would result in the leakage of 1.5-bit QN E_{q1}, thus making the SNDR distribution (shown as a blue histogram) not exactly as Gaussian distribution. To illustrate the great improvement by the proposed architecture, we also simulated a general single-loop DSM with 4-bit quantization including the result in Fig. 9 to make a comparison. For the sake of fairness, the single-loop DSM uses completely the same loop filter including the NC and FIR filter as the first loop of the proposed SMASH to obtain an equivalent NTF. As shown, with the presence of the DAC mismatch, the mean SNDR is improved by 14 dB with less standard deviation by using the presented architecture. Besides, considering similar hardware for quantization, the same single-loop DSM but with 5.5-bit quantization is also simulated. Despite an additional 9-dB QN suppression, with the presence of DAC mismatch, the final SNDR is limited by HDs with only achieving a mean value of 75.6 dB with 3.2-dB standard variation, which is almost same with the case of the single-loop DSM with 4-bit quantization. The observation leads to the conclusion that the proposed SMASH achieves the same multi-bit quantization with a general single-loop DSM, while the multi-bit DAC linearity requirement in the proposed SMASH is significantly mitigated compared with a single-loop DSM. It makes the proposed SMASH highly potential to avoid any DAC linearization techniques and thereby save power and area consumptions, avoid foreground calibration with the necessary interruptions in the operation, or avoid any on-chip test-signal generation.

In this article, a tri-level complementary current steering DAC is used with cascode current sources. The 0.2% matching accuracy for the DAC unit cells could be intrinsically obtained by moderately sizing the tail transistors, thus escaping any DAC linearization technique. Moreover, by sharing the same DAC slice for DAC_1 and DAC_2 and 0.2% matching accuracy for all DAC slices, the 0.1% gain matching requirement between both DACs can be satisfied simultaneously.

As described beforehand, the NC technique in the proposed SMASH contributes to alleviating the linearity requirement of the multibit DAC_2. Nevertheless, careful considerations must be taken into account for the specific implementation of the analog NC branch. This is because any mismatch between the analog NC path and the digital filter $(1 - z^{-1})$ would also give rise to the leakage of 1.5-bit QN E_{q1}. As presented in Fig. 10, to obtain the desired resolution (SQNR > 88 dB), the gain error of the analog NC path should stay within ±2%. This can be reliably satisfied by implementing the analog NC branch through a switched-capacitor (SC) circuitry, which will be described in detail in Section IV-B.

IV. Circuit Implementation

A. Overall Proposed SMASH Schematic

Fig. 11 illustrates the overall schematic of the proposed NC-assisted dual-loop 3–0 SMASH DSM, employing a 1.5-bit successive-approximation register (SAR) and a 4-bit flash ADC for both quantizers, respectively. All DACs use a non-return-to-zero (NRZ) tri-level topology, thus resulting in less unit DAC cells as well as less preceding drivers. The first loop employs a third-order mixed FF/FB topology, with an OBG of 2.3. The FF/FB combination separates the high-gain and high-speed requirements into the first and third integrators [7], respectively, which allows a better operational amplifier (op-amp) power efficiency. In addition, a local resonator path generated by the first and second integrators introduces one zero in the NTF to further suppress the in-band noise. The two FF paths can effectively decrease the swings of the

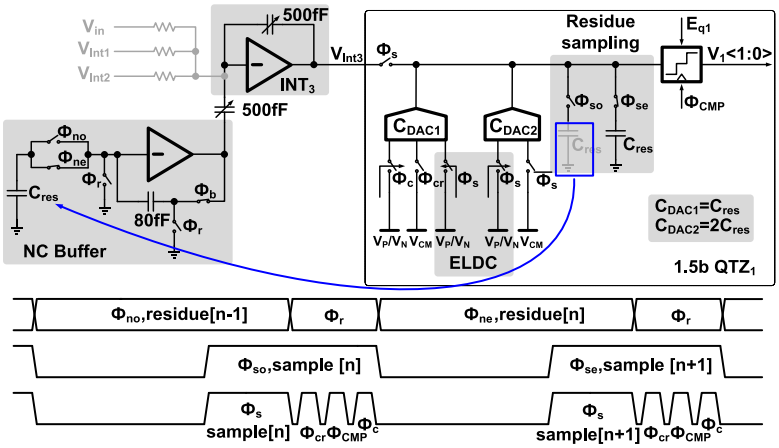

Fig. 12. Implementation of the 1.5-bit SAR ADC with the corresponding timing diagram.

first and second integrators. To compensate the introduced outermost two-tap FIR filter, a simple FIR compensation filter $F_C(z)$ is incorporated into the inner FB branches, thus restoring the original NTF [24]. Considering all non-ideal effects, the coefficients of the compensation filter are determined and updated iteratively from the behavioral model to post-sim level by using the impulse response matching method described in [25]. To compensate for process variation, the integration and NC capacitors are digitally programmable with a 4-bit trimming accuracy, which can cover $\pm 40\%$ *RC* variations.

By utilizing a 1.5-bit SAR ADC for the first quantizer, the QN E_{q1} is naturally produced on the summing node by the end of the charge redistribution. Therefore, the extraction of QN E_{q1} is only determined by the capacitor ratio, which is robust over process and temperature variations. After the SC extraction, the residue is injected into the last integrator through an SC buffer, generating the first-order NC branch [9]. Meanwhile, the SC buffer also directly drives the second stage. In order to close the SMASH loop, this architecture uses 0.75 T_S as an overall ELD. To compensate for the ELD, a unity-gain zeroth-order path with one cycle delay [2] is integrated inside the 1.5-bit SAR ADC.

This proposed SMASH DSM renders a fourth-order 1.5-bit quantization first loop combined with zeroth-order 4-bit-quantization second loop into an equivalently operating overall fourth-order DSM architecture with 4-bit quantization. With an OSR of 12 used in this article, the proposed SMASH DSM obtains an ideal SQNR of 90 dB.

B. Noise Consideration

In the proposed SMASH DSM, we set an SNR ∼of 80 dB as our design target, where we left about ∼2-dB margin for other external error sources. The DSM performance is thermal noise limited. The input-referred thermal noise contributions from the input resistor, the first op-amp, and the outermost NRZ DACs are designed to be −87.2, −88.4, and −87.5-dB-FS, which finally sums up to −82.9-dB FS for the first integrator. The values of the first and second input resistors are chosen as 250 and 500 Ω, respectively, to satisfy the thermal noise requirement. Other resistors, integrators, and the inner DACs in the following stages are correspondingly scaled down to make their thermal noise contributions negligible compared with the input front end. Together with clock jitter noise and QN, the simulated overall noise power of the proposed SMASH DSM is −81.3-dB FS.

C. Implementation of the 1.5-bit SAR and NC Branch

Fig. 12 depicts the specific implementation of the 1.5-bit SAR ADC with the corresponding timing diagram, integrating the ELD compensation as well as the residue sampling. During the Nth sampling phase, the bottom plates of the DAC capacitors C_{DAC1} and C_{DAC2} connect to the digital outputs V_1 and $V_2(1-z^{-1})$ from the previous $(N-1)$th cycle, while their top plates sample the output of the third integrator. Subsequently, by connecting all bottom plates to the common-mode V_{CM}, the summing node of the capacitor network settles to $V_{\mathrm{Int3}} - (V_1 - V_2(1-z^{-1}))z^{-1}V_{\mathrm{Ref}}$. Therefore, a negative FB path with a nominal unity-gain is generated around the first quantizer, stabilizing the modulator with the 0.75 T_S ELD [9]. Since this ELD compensation method cannot help to reduce the swing of the last integrator, a scaling factor 1/4 is applied to the third integrator, thus significantly decreasing its swing as well as enhancing its FB factor. Note that the NC branch may also saturate the last integrator owing to the large amplitude of the 1.5-bit QN. To address this issue, the same scaling factor 1/4 is likewise applied to NC branch by extracting a scaling-down (1/4) residue from 1.5-bit SAR as the NC input (which is shown later). To maintain the original NTF, the references of the 1.5-bit quantizer in the first stage are correspondingly scaled down by a factor of 4 [26]. Two identical comparators are employed in parallel for the 1.5-bit quantization. Each comparator slice [13] comprises a preamplifier, a strong-arm regeneration latch, as well as a set-reset (SR)-latch. After the decision, the digital codes V_1 <1:0> are fed back to C_{DAC1}. Eventually, the residue E_{q1} of the current cycle would be produced on the summing node. By setting the total values of C_{DAC1} and C_{DAC2} as C_{res} and $2C_{\mathrm{res}}$, respectively, the residue is correctly scaled as $E_{q1}/4$, which will be subsequently alternately sampled by two identical capacitors C_{res} [9]. Afterward, as illustrated in Fig. 12, the residue charge is injected back

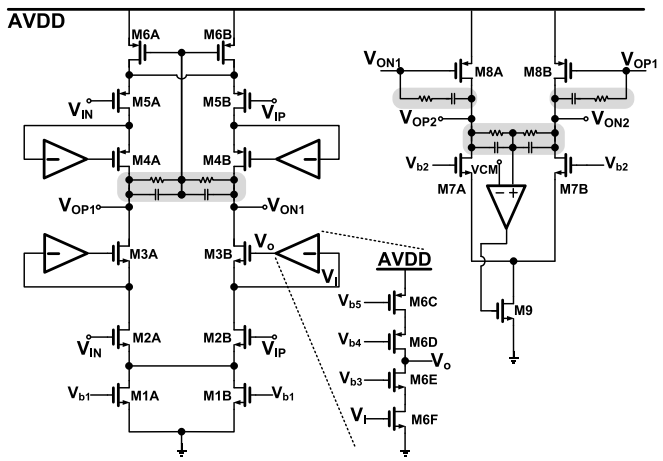

Fig. 13. Two-stage op-amp with Miller compensation used for the third integrator and NC buffer.

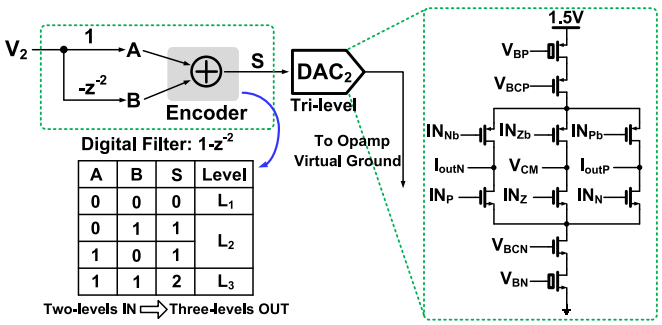

Fig. 14. One example showing the implementation of the 4-bit tri-level DAC.

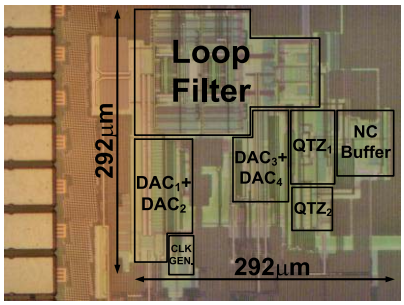

Fig. 15. Prototype chip micrograph.

to the third integrator through a unity-gain SC buffer in a closed-loop operation. Note that the input of the SC buffer is merely the scaling-down QN $E_{q1}/4$, whose swing is much smaller than a full-scale signal. It would lead to less power consumption when compared with the SC buffer processing a full-scale signal. The value of C_{res} is properly selected as 80 fF, compromising with good immunity to the parasitic capacitance existing in the virtual ground of the buffer op-amp and the conversion speed of the SC array in the 1.5-bit SAR. Therefore, a complete first-order NC path consists of the SC buffer and the summer formed by the third integrator.

D. Op-Amps

To achieve a better settling behavior, a Miller compensation is applied in the two-stage op-amp used for the third integrator and the NC buffer, rather than an FF compensation typically used in CT integrators. It is because the FF compensation introduces a zero at high frequency in the left half-plane and thereby worsens the settling [13]. As depicted in Fig. 13, the two-stage op-amp architecture is composed of a complementary input, cascade gainboosting, telescopic topology [27] for the first stage to double g_m, and the open-loop gain with less noise-contributing transistors, followed by a general differential architecture for the second stage. For the first stage, the common-mode FB (CMFB) is self-biased by using a parallel resistor–capacitor connection. In contrast, an active CMFB is used for the second stage to better control the output common-mode level. In order to achieve the desired NC gain error, the op-amp working as the third integrator has a dc gain of 72 dB and 4.8-GHz unity gain BW (UGBW), while the op-amp serving as the NC buffer achieves a dc gain of 72 dB and 6.4-GHz UGBW. Due to the relaxed settling requirements, the first and second integrators employ similar two-stage op-amp topology as shown in Fig. 13 but with a FF compensation for a better power efficiency [13]. Since their gain requirements are not as critical as the op-amps incorporated in the NC path, a simple common source topology is used for the gain-boosting branch. The FF path reuses the current from the second stage without consuming extra power. In addition, the input path is ac-coupled to the second stage to further improve the output linearity performance.

E. Tri-Level DAC

The 1.5-bit DAC has intrinsically three levels, while the 4-bit DAC combines the preceding filter, as shown in Fig. 11; both can be implemented using a tri-level DAC topology. Fig. 14 illustrates one example for the implementation of the 4-bit tri-level DAC_2 combining the preceding filter $(1-z^{-2})/2$. As shown, every single-bit signal of the thermometer-coded output V_2 in Fig. 11 running through the digital filter can be implemented as going through a tri-level encoder to generate three-level outputs in Fig. 14, thus matching the subsequent tri-level DAC.

Each DAC slice employs a complementary current-steering topology with cascode current sources. A 1.5-V power supply is used to provide adequate voltage headroom and obtain the required thermal noise. The tail transistors of the outermost DACs are properly sized to obtain the desired 0.2% matching accuracy. Due to the suppression of the preceding integrators, the target matching accuracy for inner DACs is 0.4% without affecting the target SNR. Combined with the suppression of thermal noise at this point, each slice size of the inner DACs is scaled down by a factor of 4 or more.

V. Experimental Results

A prototype of the proposed CT SMASH DSM was fabricated in a 28-nm CMOS process. The chip micrograph is shown in Fig. 15. The active core area is 0.085 mm^2.

Running at a sampling frequency of 1.2 GHz, the digital outputs of both stages are combined off-chip through a simple digital cancellation logic (as shown in Fig. 11) to generate

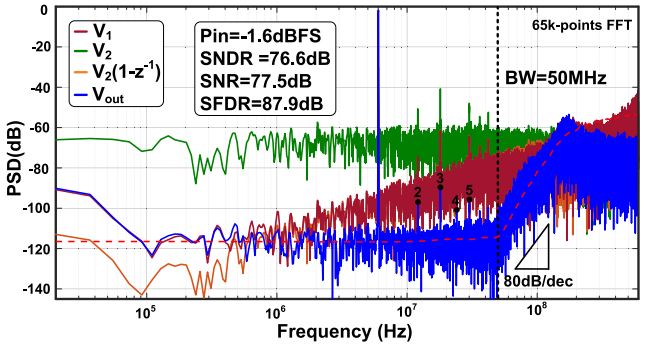

Fig. 16. Measured FFT spectrum of the digital outputs V_1, V_2, $V_2(1-z^{-1})$ and the final output V_{out} of the prototype DSM.

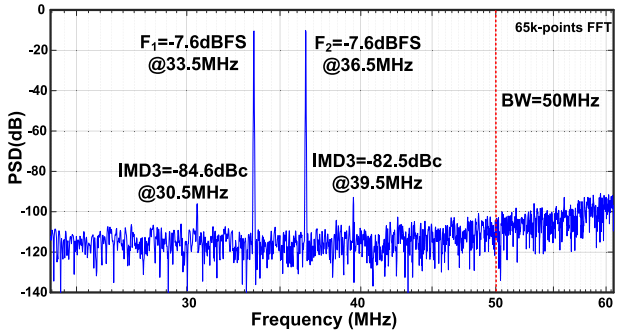

Fig. 17. Measured FFT spectrum of the IMD_3.

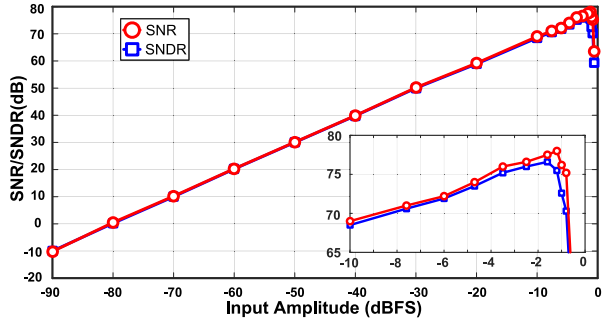

Fig. 18. Measured SNR/SNDR versus input signal power.

the final output. For the digital cancellation logic, the estimated logic gate count is 64, resulting in less than 100-μW digital power and 70 μm^2 area consumption. Note that the estimated area consumption of the digital cancellation logic is completely negligible to the active core area.

Fig. 16 shows the measured 65k-points FFT output spectrum for two digital outputs V_1 and V_2 as well as for $V_2(1-z^{-1})$ with a -1.6-dB FS input at 6 MHz. Both the spectra of V_1 and $V_2(1-z^{-1})$ almost overlap in the band of interest, thus implying that the desired cancellation of the QN E_{q1} would be accomplished through their subtraction. By subtracting V_1 and $V_2(1-z^{-1})$, it results in the final output V_{out}. Note that the theoretical noise plot shown in the red dotted line is also included in Fig. 16 to prove that the measured spectrum basically matches the theoretical result. As observed, the OOB spectrum of the final output V_{out} exhibits an 80-dB/decade slope of the shaped noise, thus indicating the desired fourth-order noise-shaping is obtained in this article. The

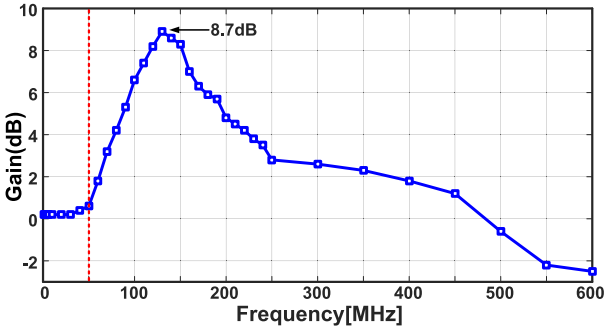

Fig. 19. Measured STF of the prototype DSM.

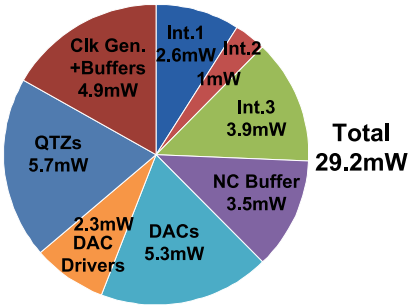

Fig. 20. Power breakdown of the prototype modulator.

measured SNDR/SNR/spurious-free dynamic range (SFDR) is 76.6 dB/77.5 dB/87.9 dB over a 50-MHz signal BW, respectively. By comparing the achieved SNDR of the output V_1 of the first stage, noise and distortion cancellation of 31 dB was obtained through the digital cancellation logic. The in-band SNDR performance is mostly limited by the thermal noise, which is in line with the theoretical estimation but $\sim$2 dB worse than the final post-layout simulation result.

As shown in Fig. 17, with two -7.6-dB FS inputs at 33.5 MHz/36.5 MHz, the measured IMD_3 is -84.6 dBc/-82.5 dBc, respectively. Fig. 18 shows the SNR/SNDR over input signal power, where the dynamic range (DR) is measured to be 80 dB. In addition, the MSA is achieved to be around -1-dB FS, which clearly verifies the effective multibit quantization within the loop filter. Fig. 19 shows the measured STF with a -35-dB FS input signal. The maximum STF peaking is 8.7 dB at around 130 MHz.

Fig. 20 provides a power breakdown. With 1.5-V supply for the DACs and 1.2 V for other blocks, the total power consumption is 29.2 mW. To achieve the desired NC gain error, the power consumed by the third integrator and NC buffer is larger than other op-amp blocks. In addition, the quantizers dissipate 19.5% of the total power to expedite the whole ELD loop and the residue extraction. Due to the use of the SC buffer and the required clock jitter performance, the clock part and DAC drivers contribute 24.7% of the total power.

Table I summarizes the performance of the prototype and makes a comparison to other SoA CT wideband DSMs. The prototype achieves a competitive Schreier figure-of-merit (FoM) of 168.9 dB. Using the proposed techniques, high linearity is achieved without employing any DAC linearization technique. In contrast, for other works [6], [9], [11], [14] with using multibit quantization, they either employ on-chip or

TABLE I

PERFORMANCE SUMMARY AND BENCHMARK WITH STATE OF THE ART

	This Work	ISSCC'18 He [14]	ISSCC'17 Huang [11]	JSSC'16 Wu [9]	JSSC'15 Yoon [6]	JSSC'16 Loeda [12]
Architecture	**SMASH 4th-order 1.5bit/4bit**	Single-loop 4th-order 4bit	Single-loop 4th-order 7bit	Single-loop 6th-order 4bit	SMASH 4th-order 4bit/4bit	Single-loop 4th-order 1bit
Process (nm)	**28**	28	16	65	28	40
Supply (V)	**1.2/1.5**	1.16/1.5	1/1.35/1.5	1.2/1.8	1.2/1.5	N/A
BW(MHz)	**50**	50	125	45	50	40
F_S (GHz)	**1.2**	2	2.15	0.9	1.8	2.4
SNDR (dB)	**76.6**	79.8	71.9	75.3	74.6	66.9
SFDR (dB)	**87.9**	95.2	N/A	83	89.3	N/A
THD (dBc)	**-83.9**	-94.1	-80	-78.1*	-79.9*	N/A
Power (mW)	**29.3****	64.3	54	24.7	78	5.25
Area (mm^2)	**0.085**	0.25	0.217	0.16	0.34	0.02
DAC Cal.	**w/o**	w/ on-chip	w/ on-chip	w/ off-chip	w/ on-chip	w/o
FoMw (fJ/step)	**53.1**	80.5	67.2	57.7	177.7	36.3
FoMs (dB)	**168.9**	168.7	165.5	167.9	162.7	165.7

$$FoM_W = \frac{Power}{2 \cdot BW \cdot 2^{[(SNDR-1.76)/6.02]}} \quad FoM_S = SNDR + 10 \cdot \lg\left(\frac{BW}{Power}\right)$$

*THD calculated based on the difference between SNDR and SNR reported.

** Include the estimated power of the digital cancellation logic.

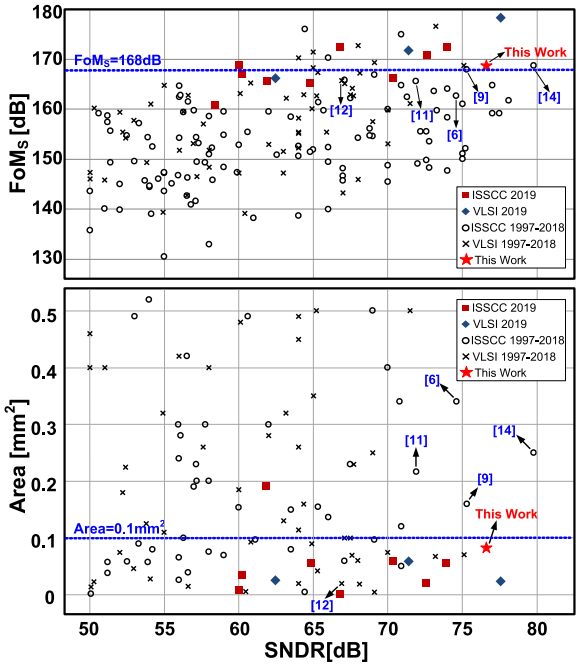

Fig. 21. Comparison with other ADCs published in ISSCC and VLSI.

off-chip DAC calibrations. As obviously observed in Table I, when compared with those works using on-chip DAC calibrations, the power and, especially, the area consumed by the proposed prototype are much smaller. As for the single-bit DSM in [12], even though the DAC calibration is obviously avoided as well, the achieved resolution is much lower than the presented and its MSA is also much lower. The latter does not only require significantly smaller input-referred noise for the same SNR, but it would also impose stricter noise requirements on the preceding circuitry of a transceiver.

Fig. 21 shows a comparison of the presented design with previously published ADCs with a signal BW $\geq$20 MHz and SNDR $\geq$ 50 dB published in ISSCC and VLSI 1997–2019 [28]. The upper one depicts the Schreier FoM versus the SNDR among all ADC works. This article achieves an SoA Schreier FoM while avoiding an explicit DAC linearization within the area where SNDR $\geq$ 75 dB. In contrast, for other works [6], [9], [14] with similar Schreier FoM and SNDR, all do employ DAC calibrations. From the perspective of the area consumption, the second comparison plot shows that this article achieves an attractively small area in the range where SNDR $\geq$ 75 dB.

VI. CONCLUSION

This article presents a dual-stage CT SMASH DSM using 1.5-bit/4-bit quantizers, respectively. First, it renders a fourth-order 1.5-bit first stage effectively into an overall fourth-order multibit DSM, achieving large MSA and OBG. Second, a zeroth-order topology is selected for the second loop to achieve an accurate unity-gain STF, resulting in less 1.5-bit noise leakage. Third, an SC extraction is applied for the QN extraction, which is robust over process and temperature variations. Fourth, combining the applied NC technique in the SMASH and an FIR LPF, the sensitivity to the multibit DAC non-linearity is mitigated significantly. Eventually, this article effectively operates as an overall fourth-order CT DSM with multibit quantization but escaping any DAC linearization. Fabricated in 28-nm CMOS with 1.2-V/1.5-V supplies, the prototype clocked at 1.2-GHz sampling frequency measures an SNDR/SFDR/DR of 76.6 dB/87.9 dB/80 dB over a 50-MHz

signal BW, respectively, with free DAC linearization. It consumes 29.2-mW power, yielding a Schreier FoM of 168.9 dB.

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REFERENCES

[1] A. Edward *et al.*, "A 43-mW MASH 2-2 CT ΣΔ modulator attaining 74.4 dB/75.8 dB/76.8 dB SNDR/SNR/DR and 50 MHz of BW in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 448–459, Feb. 2017.

[2] Y.-S. Shu, J.-Y. Tsai, P. Chen, T.-Y. Lo, and P.-C. Chiu, "A 28 fJ/conv-step CT ΔΣ modulator with 78 dB DR and 18 MHz BW in 28 nm CMOS using a highly digital multibit quantizer," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 268–269.

[3] J. G. Kauffman, P. Witte, J. Becker, and M. Ortmanns, "A 8.5 mW continuous-time ΔΣ modulator with 25 MHz bandwidth using digital background DAC linearization to achieve 63.5 dB SNDR and 81 dB SFDR," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2869–2881, Dec. 2011.

[4] J. G. Kauffman, P. Witte, M. Lehmann, J. Becker, Y. Manoli, and M. Ortmanns, "A 72 dB DR, CT ΔΣ modulator using digitally estimated, auxiliary DAC linearization achieving 88 fJ/conv-step in a 25 MHz BW," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 392–404, Feb. 2014.

[5] S. Ho, C.-L. Lo, J. Ru, and J. Zhao, "A 23 mW, 73 dB dynamic range, 80 MHz BW continuous-time Delta-Sigma modulator in 20 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 908–919, Apr. 2015.

[6] D.-Y. Yoon, S. Ho, and H.-S. Lee, "A continuous-time sturdy-MASH ΔΣ modulator in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2880–2890, Dec. 2015.

[7] Y. Zhang, C.-H. Chen, T. He, and G. C. Temes, "A continuous-time Delta-Sigma modulator for biomedical ultrasound beamformer using digital ELD compensation and FIR feedback," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 7, pp. 1689–1698, Jul. 2015.

[8] Y. Dong *et al.*, "A 930 mW 69 dB-DR 465 MHz-BW CT 1-2 MASH ADC in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2917–2927, Dec. 2016.

[9] B. Wu, S. Zhu, B. We, and Y. Chiu, "A 24.7 mW 65 nm CMOS SAR-assisted CT ΔΣ modulator with second-order noise coupling achieving 45 MHz bandwidth and 75.3 dB SNDR," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2893–2905, Dec. 2016.

[10] A. Jain and S. Pavan, "Continuous-time delta-sigma modulators with time-interleaved FIR feedback," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 2, pp. 434–443, Feb. 2018.

[11] S.-J. Huang, N. Egan, D. Kesharwani, F. Opteynde, and M. Ashburn, "A 125 MHz-BW 71.9 dB-SNDR VCO-based CT ΔΣ ADC with segmented phase-domain ELD compensation in 16 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 470–471.

[12] S. Loeda, J. Harrison, F. Pourchet, and A. Adams, "A 10/20/30/40 MHz feedforward FIR DAC continuous-time ΔΣ ADC with robust blocker performance for radio receivers," *IEEE J. Solid-State Circuits*, vol. 51, no. 4, pp. 860–870, Apr. 2016.

[13] C. Briseno-Vidrios, A. Edward, A. Shafik, S. Palermo, and J. Silva-Martinez, "A 75-MHz continuous-time Sigma–Delta modulator employing a broadband low-power highly efficient common-gate summing stage," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 657–668, Mar. 2017.

[14] T. He, M. Ashburn, S. Ho, Y. Zhang, and G. Temes, "A 50 MHz-BW continuous-time ΔΣ ADC with dynamic error correction achieving 79.8 dB SNDR and 95.2 dB SFDR," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 230–232.

[15] S. Dey, K. Reddy, K. Mayaram, and T. S. Fiez, "A 50 MHz BW 76.1 dB DR two-stage continuous-time Delta–Sigma modulator with VCO quantizer nonlinearity cancellation," *IEEE J. Solid-State Circuits*, vol. 53, no. 3, pp. 799–813, Mar. 2018.

[16] L. Qi, A. Jain, D. Jiang, S.-W. Sin, R. P. Martins, and M. Ortmanns, "A 76.6 dB-SNDR 50 MHz-BW 29.2 mW noise-coupling-assisted CT sturdy MASH ΔΣ modulator with 1.5 b/4b Quantizers in 28 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 336–338.

[17] L. J. Breems *et al.*, "A 2.2 GHz continuous-time ΔΣ ADC with −102 dBc THD and 25 MHz bandwidth," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2906–2916, Dec. 2016.

[18] S. Pavan, R. Schreier, and G. C. Temes, *Understanding Delta–Sigma Data Converters*, 2nd ed. Hoboken, NJ, USA: Wiley, 2017, pp. 85–90.

[19] L. J. Breems, R. Rutten, and G. Wetzker, "A cascaded continuous-time ΣΔ modulator with 67-dB dynamic range in 10-MHz bandwidth," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2152–2160, Dec. 2004.

[20] Y.-S. Shu, J. Kamiishi, K. Tomioka, K. Hamashita, and B.-S. Song, "LMS-based noise leakage calibration of continuous time ΔΣ modulator," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 368–379, Feb. 2010.

[21] Q. Liu, A. Edward, D. Zhou, and J. Silva-Martinez, "A continuous-time MASH 1-1-1 Delta–Sigma modulator with FIR DAC and encoder-embedded loop-unrolling quantizer in 40-nm CMOS," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 4, pp. 756–767, Apr. 2018.

[22] N. Maghari, S. Kwon, and U.-K. Moon, "74 dB SNDR multi-loop sturdy-MASH Delta-Sigma modulator using 35 dB open-loop opamp gain," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2212–2221, Aug. 2009.

[23] K. Lee, M. R. Miller, and G. C. Temes, "An 8.1 mW, 82 dB Delta-Sigma ADC with 1.9 MHz BW and −98 dB THD," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2202–2211, Aug. 2009.

[24] A. Sukumaran and S. Pavan, "Low power design techniques for single-bit audio continuous-time delta sigma ADCs using FIR feedback," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2515–2525, Nov. 2014.

[25] S. Pavan, "Systematic design centering of continuous time oversampling converters," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 57, no. 3, pp. 158–162, Mar. 2010.

[26] L. Qi, S.-W. Sin, S.-P. U, F. Maloberti, and R. P. Martins, "A 4.2-mW 77.1-dB SNDR 5-MHz BW DT 2-1 mash ΔΣ modulator with multirate opamp sharing," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 10, pp. 2641–2654, Oct. 2017.

[27] B. Wang, S.-W. Sin, S.-P. U, F. Maloberti, and R. P. Martins, "A 550-uW 20-kHz BW 100.8-dB SNDR linear-exponential multi-bit ΔΣ ADC with 256 clock cycles in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 4, pp. 1161–1172, Apr. 2019.

[28] B. Murmann, *ADC Performance Survey 1997-2019*. Accessed: Sep. 6. [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html

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