A 14-Bit Split-Pipeline ADC With Self-Adjusted Opamp-Sharing Duty-Cycle and Bias Current

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***Abstract*—Pipeline analog-to-digital converters (ADCs), which dominated high-speed and high-resolution applications, suffered from weak improvement in power efficiency. To address such a problem, this brief presents a 14-bit split-pipeline opamp-sharing ADC, with background calibration that optimizes duty-cycle ratio and amplifier power consumption in the shared opamp. Based on the interstage gain (that includes settling) error estimated by the split ADC calibration engine, the clock duty-cycle ratio and the bias current are adjusted to achieve better dynamic settling and resolution trade-offs. Operating at 100 MS/s with a 9-MHz input signal, the ADC achieves 46.5 dB of signal-to-noise-and-distortion ratio (SNDR) and 59.6 dB of spurious-free dynamic range (SFDR) before calibration, and after calibration, it improves to 71.7 dB of SNDR and 84.4 dB of SFDR, respectively. The ADC maintains an SNDR over 68.5 dB within the full Nyquist bandwidth consuming 32 mW of power, which yields a Walden figure-of-merit (FoM) of 147.2 fJ/conversion-step and a Schreier FoM of 160.4 dB.**

***Index Terms*—Analog-to-digital conversion, digital background calibration, pipelined ADC, split ADC, opamp-sharing technique.**

I. Introduction

THE PIPELINE ADC is the primary choice for the streaming, entertainment and communications application areas for its robust performance and high linearity. Since with process scaling down, the power efficiency of the amplifier-based pipeline ADC improves slowly, this implies that the ADC gradually becomes one of the main sources of power consumption in the system. In traditional amplifier-based Multiplying DAC (MDAC) circuits, the bias current and its settling time in each opamp are fixed. A higher design margin of the amplifier is required to meet all the process corners and working temperature conditions, thus leading to higher power consumption. Because the ADC will not always be fabricated in a slow process corner, neither will it always work in extreme temperature conditions, such extra power consumption to cover the extreme working conditions is a waste in normal operation.

The opamp-sharing technique is one of the solutions that can reduce the overall power consumption of pipelined ADC. Former works include opamp-sharing between adjacent stages [1], [2], reusing the current in one amplifier allowing it to work in two stages [1], or using a non-50% duty-cycle ratio to increase amplifier power efficiency [2], etc. However, these opamp-sharing schemes make the MDAC residue amplifiers more sensitive to various dynamic effects [3], and they also do not conform to the optimized pipeline scaling strategy [4].

Another method for higher power efficiency is to dynamically adjust the bias current of the amplifier [5]. In the former work, foreground calibration is accomplished by extracting the inter-stage gain parameter of the MDAC (that also includes the settling errors). By adopting the minimum bias current that maintains the required MDAC's inter-stage gain, the system finally obtains a higher power efficiency. However, this method is a foreground calibration thus cannot track the changing temperature and supply conditions; also, since the bias current is determined during the start-up, this technique cannot be utilized in an opamp-shared architecture since the opamps are working in a ping-pong manner between different stages that can have different settling requirements.

In this brief, we propose the background control of amplifier's sharing duty-cycle ratio and its bias current. Based on the observation of parameters estimated by a split-ADC calibration engine, the ADC records the gain and settling error's behavior to optimize the cost function and gets the best dynamic control of the duty-cycle ratio and the bias currents. This helps to alleviate the problems in [4] and is naturally suitable for the power scaling strategy of pipeline ADCs.

II. Errors in a Split-Pipeline ADC and the Proposed Calibration Scheme

A. The Calibration Mechanism in a Split-Pipeline ADC

Ones of the primary error sources in a pipeline ADC are the inter-stage gain and the settling errors, which can be extracted by background calibration methods like reference-ADC-based Least Mean Square (LMS) [6], Pseudo-random Number (PN) injection with Dynamic Element Matching (DEM) [7] or split ADC [8]. Split ADC is one of the efficient ways to extract and calibrate the errors above, having advantages that include (a) no extra calibration channel is necessary, and (b) no signal injection is required that may occupy the limited dynamic range of the amplifiers in MDACs.

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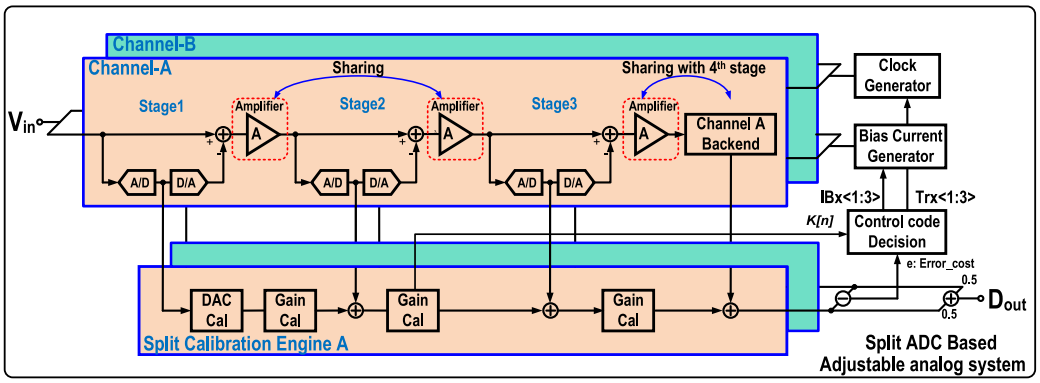

Fig. 1. Block diagram of the overall proposed split-pipeline ADC with opamp-sharing and calibration.

Fig. 1 shows the block diagram of a possible split-pipeline ADC that will be utilized in this brief. Two halves of the almost-identical pipeline ADC sub-channel, channel A and B, work simultaneously to convert the same analog input voltage V_{in} at the same sampling instance. As required by the generic split-ADC operation to avoid false convergence caused by zero error cost function [9], the 1st & 2nd stages in channel A comprise a 9-level MDAC while in channel B it is an 8-level, and the residue transfer function is horizontally offset from the other by approximately 1/8 V_{REF}. To consume less power, we use an opamp-sharing technique, e.g., sharing opamps in stages 1 and 2 within the same channel A. The pipeline ADC is an S/H-less type, and the timing-mismatch errors between the 1st stage flash and the MDAC sampling are tolerated by the traditional error correction tolerance scheme [10]. A short reset phase during the non-overlapping time is implemented to clear the memory effect of the opamp-sharing ADC [1].

The non-idealities in the analog components, like the gain errors (by finite opamp gain and capacitor mismatches) and settling errors, cause the deviations of the overall MDAC's inter-stage gain transfer functions in the sub-channels. The split calibration engine extracts the difference of such deviations between channels as the error cost function to drive and adjust the corresponding analog parameters. As proposed in this brief, the engine drives the 3b data Trx<1:3> which represents the duty-cycle ratio in the opamp-sharing clock distribution, as well as another 3b data IBx<1:3> for the opamp bias current adjustment. The goal is to achieve the convergence on the minimization of the error cost function that is linked to the ADC performance.

B. Adjustable Duty-Cycle Control and Bias Current of the Opamp-Sharing Pipeline ADC

We utilize opamp-sharing in the proposed split-pipeline sub-channel. As Fig. 1 shows, opamps in stage 1 and 2 are shared. Since the same opamp bias current is used in both stages, the settling dynamic will be slower in stage 1 when compared with stage 2 (Fig. 2). The large capacitive load in stage 1 causes large settling errors, while in stage 2 the opamp would be too fast due to the smaller capacitive loading. This creates a waste in the opamp current usage in stage 2, while in stage 1 the settling errors are dominant and become the bottleneck of the linearity of the whole pipeline ADC. To worsen the overall operation, the settling of the opamp is determined by its transconductance g_m and its capacitive load C_L, and both have process variations, with the corners move independently. To counteract the corners, a large margin of opamp bias current is necessary, which penalizes the power consumption of the ADC.

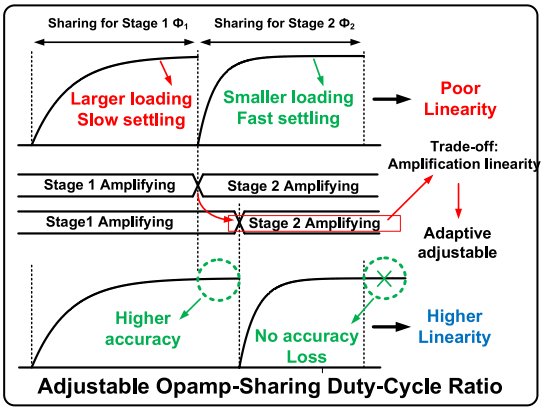

Fig. 2. The proposed self-adjustable opamp-sharing duty-cycle ratio.

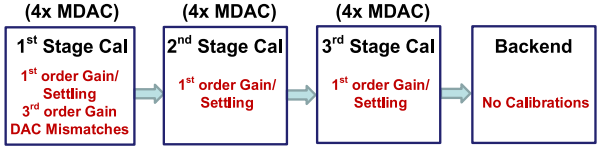

Fig. 3. The overall calibration setup of the ADC.

To alleviate the settling errors in the MDAC with a minimum power consumption of the opamp, we propose to auto-adjust the clock-period-ratio for stage 1 and stage 2 settling time by the cost function. That is, the duty-ratio between Φ1 & Φ2 is self-adjusted by the calibration algorithm, as Fig. 2 illustrates. The settling error in stage 1 causes nonlinearity in the overall ADC transfer function, which is extracted through the split ADC's cost function, and eventually, the calibration engine adjusts the duty ratio of the clock phases (through Trx<1:3>) to allocate additional settling time in phase 1. In this way, for the same power budget in the shared opamp, we allocate an extra settling time in the 1st stage while we need less in 2nd stage, achieving a well-balanced situation in terms of resolution and power trade-off.

The bias current of the opamp will also affect the settling errors. We also use the cost function to optimize the opamp bias current (through IBx<1:3>), while searching for the minimum power consumption and maintaining the linearity performance. This will contribute to the overall reduction of the ADC's power consumption over different Process, Voltage and Temperature (PVT) corners.

III. The Calibration Algorithm

The split-pipeline ADC proposed in this brief calibrates the inter-stage gains (that include settling errors), 3rd order

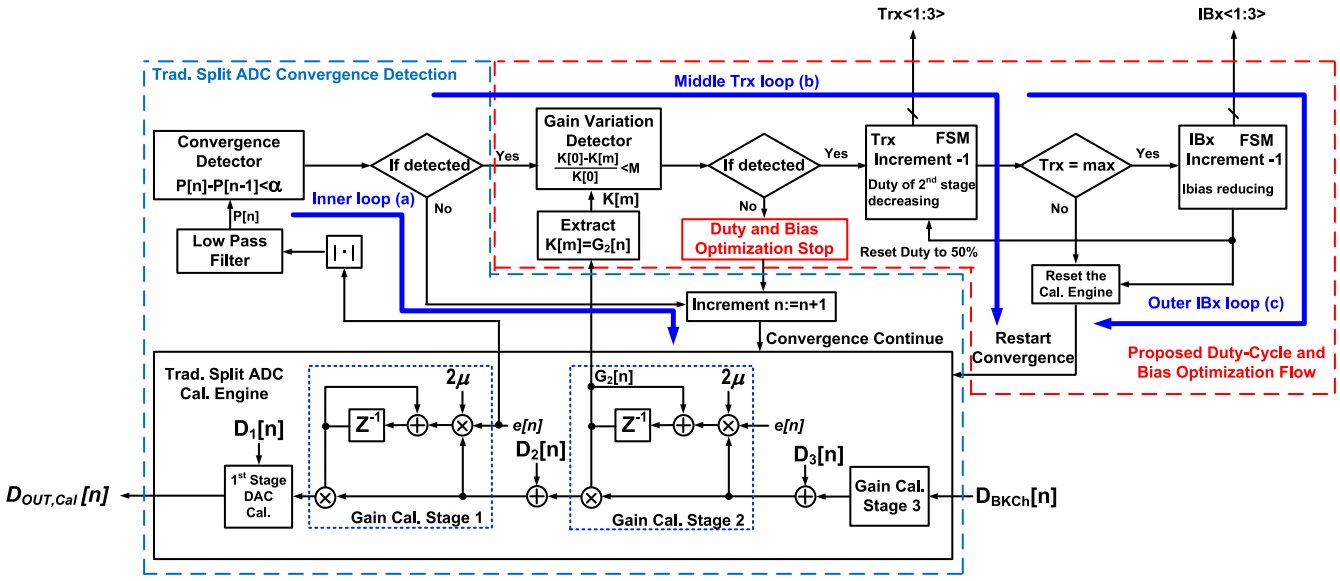

Fig. 4. The flow chart of the calibration algorithm.

nonlinear gain errors and Digital-to-Analog Converter (DAC) mismatch errors with traditional split-ADC calibration algorithm [8], and Fig. 3 illustrate the corresponding non-idealities that will be calibrated on each stage. In the 1st stage, linear gain/settling errors, 3rd order nonlinear gain error, and DAC mismatches are all calibrated. For the 2nd stage, the accuracy requirement is already relaxed to 12b, and we calibrate only linear gain/settling errors. The same calibration scheme happens in the 3rd stage. After that, no calibration is necessary for the backend.

Fig. 4 illustrates the overall conceptual calibration flow of the proposed ADC. It contains 3 loops: (a) the traditional split- ADC calibration inner loop; (b) the proposed duty-cycle optimization middle loop; and (c) the proposed bias current optimization outer loop. For simplicity, the 3rd order nonlinear gain calibration is not shown in the loop (a).

The ADC will be initially set with the largest bias current and 50% duty-cycle ratio. This makes the 2nd stage MDAC fast enough so that its settling errors can be neglected in the initial calibration phase. The loop (a) starts to calibrate the non-idealities listed in Fig. 3. Using the difference of the output codes from channel A and B as the cost function "J", we adopt the LMS algorithm to estimate the gain error. Neglecting the errors after the 1st stage, the error cost function will become:

$$J = |e|^2 = \Big[D_{1A} - D_{1B} + \sum \varepsilon_{DACiA} Con(D_{1A}) - \sum \varepsilon_{DACiB} Con(D_{1B}) + G_{1A} D_{BKChA} - G_{1B} D_{BKChB}\Big]^2 \quad (1)$$

where D_{1X} (X refers to channel A or B) is the digital code from the 1st stage, ε_{DACiX} is the coefficient corresponding to the mismatch error from the i^{th} capacitor in the MDAC, Con(D_{1X}) is the control code of the 1st MDAC capacitor array, G_{1X} is a coefficient correspondi ng to the gain of the 1st stage and D_{BKChX} is the output code from the backend ADC. The gradients of the gain and DAC mismatch errors can be expressed as:

$$\nabla G_{1X} = \frac{\partial e}{\partial G_{1X}} = D_{BKChX} \quad (2)$$

$$\nabla \varepsilon_{DACiA} = \frac{\partial e}{\partial \varepsilon_{DACiA}} = Con(D_{1A}) \quad (3)$$

Then, the LMS update formula are then derived as:

$$G_{1X}[n+1] = G_{1X}[n] + 2\mu e[n] D_{BKChX}[n] \quad (4)$$

$$\varepsilon_{DACiA}[n+1] = \varepsilon_{DACiA}[n] + 2\mu e[n] Con(D_{1A}) \quad (5)$$

After we achieve calibration convergence, the gain error's convergence value of the 2nd stage K[m] will be attained. This is considered as a fully settled gain value with finite amplifier gain error only (because of maximum bias current and 50% duty ratio). Then the loop (b) will adjust the duty-cycle through Trx<1:3> to allocate more time to the 1st stage settling, and the convergence of loop (a) will be restarted. The output signal settling of i^{th} stage MDAC is

$$V_{out} = G(V_{in} - V_{DAC}(D_{iX}))(1 - e^{-\frac{t}{\tau}}) \quad (6)$$

where V_{in} is the analog input of the MDAC, V_{DAC} is the DAC reference voltage, D_{iX} is the output code of the i^{th} stage in the pipeline ADC, G is the gain parameter which only relates to the finite amplifier gain, and t is the time constant of the settling.

With less time allocated in the 2nd stage, its gain will gradually decrease as demonstrated in (6) when the time is smaller than needed to have a full settling. Note that a portion of the settling error can be calibrated as a gain error during this process. The duty-cycle adjustment will stop when the gain of the 2nd stage K[m] decreases by M=5% compared to its initial value K[0] (obtained under maximum bias and 50% duty condition). This is detected by the "Gain Variation Detector" as shown in Fig. 4. If it doesn't reach this value after the duty of 2nd stage settling time reaches the minimum, less bias current will be set by the outer loop (c), and the calibration restarts a new cycle of duty-cycle adjustment. This procedure will be repeated until the ratio of gain variation in 2nd stage crosses the threshold M=5%. The bias current and the duty-cycle ratio will then be frozen, and the split ADC reaches its target working state with minimized power consumption.

IV. Circuit Implementation

A. Design of Clock Generator and Bias Current Generator

Fig. 5 shows the circuit diagram for the clock generator with the adjustable duty-cycle functionality. A standard

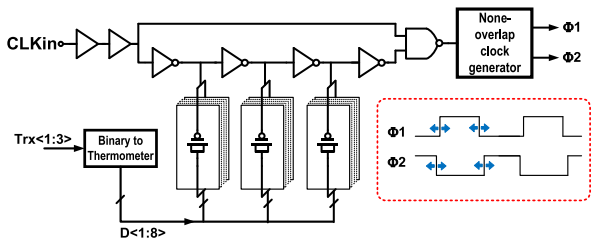

Fig. 5. Clock generator with adjustable duty-ratio.

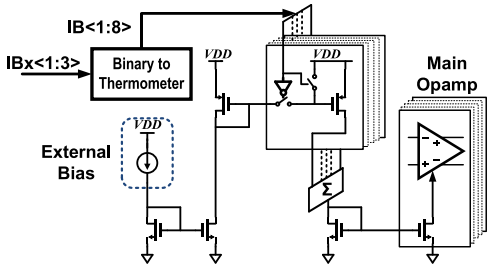

Fig. 6. Adjustable bias current generator.

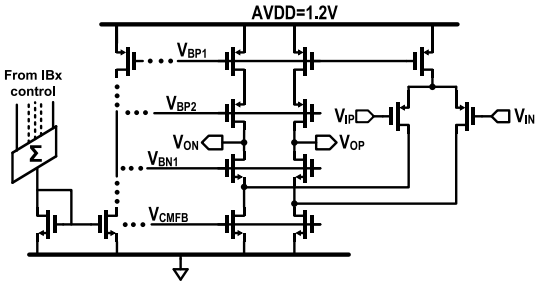

Fig. 7. The circuit schematic of the 1st opamp (shared by 1st and 2nd stage).

non-overlapping clock generator is utilized. The delay difference between the two paths before the NAND determines the pulse widths of Φ1 and Φ2. This delay is adjustable by an array of thermometer-based MOS capacitors controlled by Trx<1:3> from the calibration engine. The data modifies the biasing conditions of the MOS capacitors, and as a result, their capacitance, as well as the delay, can be adjusted.

Fig. 6 depicts the bias network of the amplifiers in the proposed pipeline ADC is shown in Fig. 6. We divide the bias current into eight thermometer-based small current sources. The total bias current is tunable by the data IBx<1:3> of the calibration engine.

B. The Circuit Schematic of the Opamp

The opamp (Fig. 7) used in this brief is a standard single-stage folded-cascode opamp with DC gain of 38dB in the 1st and 2nd MDAC. The opamp used PMOS input pair with NMOS cascode transistors that allow better phase margin. The bias current of the opamp is controlled by the IBx<1:3> from the 3rd loop of the calibration.

C. Identical Split ADC Front-End for Minimum Sampling Mismatch

The split ADC needs to sample the same analog input signal in two channels at the same sampling instance [11]. While as discussed before, for split ADC operation, a constant offset is necessary for differentiating the transfer function of

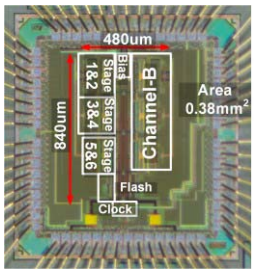

Fig. 8. Chip micrograph of prototype ADC.

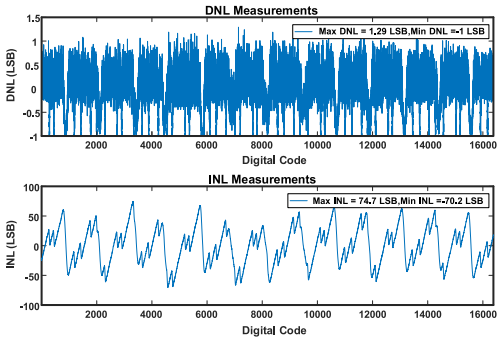

Fig. 9. Measured DNL/INL before calibration.

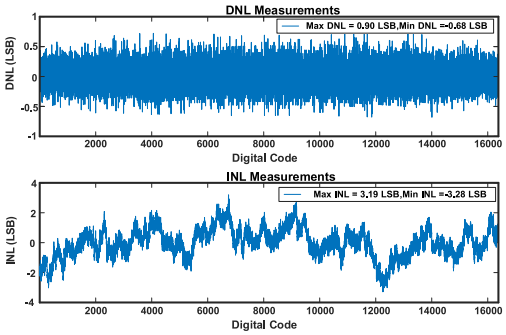

Fig. 10. Measured DNL/INL after calibration.

two channels. It will be problematic if the offset is injected in the sampling front-ends, as this will create a difference between the two sampling networks in the two channels, sampling mismatches (including gain and timing mismatches) will occur. In this brief, two identical sampling networks are implemented in sampling phase. A constant offset is implemented in hold phase by injecting an offset control code in MDAC which will minimize the sampling error between the two channels.

V. Measurement Results

Fig. 8 shows the chip micrograph of the 14-bit 100 MS/s split-pipeline ADC prototype implemented in 65 nm digital CMOS, with an active area of 0.38mm^2. The ADC has a full-scale input range of 1.2 V_{pp} differential and a total input capacitance of 5.2pF. Fig. 9 shows the measured Differential/Integral Nonlinearity (DNL/INL) before the calibration which is 1.29/74.7 LSB. With the background calibration activated, the DNL/INL is reduced to 0.9/3.28 LSB @ 14b level (Fig. 10). The calibration convergence is obtained within 1.4×10^5 samples. Fig. 11 presents the FFT spectrum (decimated by 5x to reduce the impact from the PCB buffer

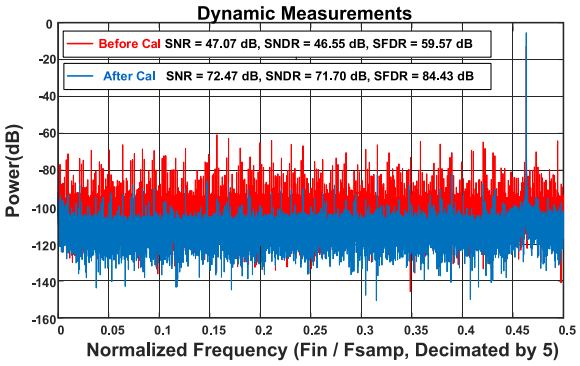

Fig. 11. Measured FFT spectrum before and after calibration.

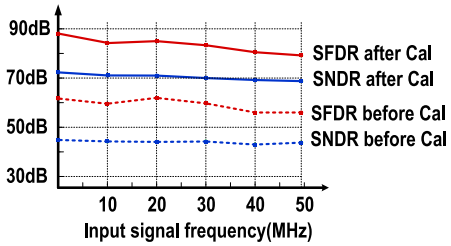

Fig. 12. Measured SNDR/SFDR vs. f_{in}, before and after calibration.

TABLE I
PERFORMANCE SUMMARY AND BENCHMARK WITH THE STATE-OF-THE-ART

	JSSC'15 [8]	ISSCC'15 [12]	ISSCC'15 [13]	ISSCC'17 [14]	This Work
Technology	40nm	180nm	65nm	65nm	65nm
Structure Feature	Split ADC w/opamp	Switched-Current Pipeline ADC	Pipeline ADC	Split ADC Pipelined SAR	Adjustable Split ADC
Signal Vppd (V)	2.0	1.25	1.5	1.0	1.2
Supply Voltage (V)	1.1	3.3/1.8	1.2	1.0	1.2
Fs (MHz)	200	500	250	75	100
SNDR@Nyq. (dB)	64.8	64.0	65.7	70.8	68.5
Power (mW)	53	550	49.7	24.9	32
Area (mm^2)	0.81	2.5	0.59	0.34	0.38
[1]Walden FoM (fJ)	191.4	849.3	126.2	117.2	147.2
[2]Schreier FoM (dB)	157.5	150.6	159.7	162.6 [3]	160.4

[1] Walden FoM = Power / [(2^ENOB@Nyq)*fs] (According to definition from B. Murmann below)
[2] Schreier FoM = SNDR@Nyq + 10*log10(BW/Power) (According to definition from B. Murmann below)
[3] Correct data from: B. Murmann, "ADC Performance Survey 1997-2017," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

switching noise, which is sensitive even for 100MS/s at this resolution) of the output (f_{in} = 9 MHz), with the SNDR and SFDR improved from 46.6dB/59.6dB to 71.7dB/84.4dB, respectively. This shows that the calibrated ADC performance is limited mainly by noise. All these results demonstrate the effectiveness of the proposed background calibration. Fig. 12 confirms the robust dynamic performance of the ADC with the SNDR maintained above 68.5dB for full Nyquist bandwidth.

The total power consumption is 32mW at a single 1.2 V supply. The self-adjusted optimization of the opamp's bias currents reduces the ADC power by as much as 30% after reaching convergence. The calculated Walden FoM at Nyquist input is 147.2 fJ while the Schreier FoM is 160.4dB. Table I summarizes the performance and presents a benchmark with recent state-of-the-art opamp-based pipelined ADCs [8], [12]–[14]. This brief achieves excellent power efficiency among the opamp-based pipeline ADC designs, even in a less advanced technology node.

VI. CONCLUSION

This brief presents a background calibration technique based on the optimization of the self-adjustable analog parameters in an opamp-sharing split-pipeline ADC architecture. The ADC gain and settling errors are corrected in the digital domain, and the working states, including the clock duty-cycle ratio and the amplifier bias current, are adjusted according to the calibration convergence values leading to optimized power efficiency. The final measurement result of shows a 25dB improvement in the SNDR with 30% of power saving after the calibration engine is active. This ADC achieves state-of-the-art performance, with an SNDR of 71.7dB obtained in a 100MS/s ADC prototype in 65nm CMOS. The total dissipating power is 32mW. This leads to a Walden FoM of 147.2fJ/conv-step and a Schreier FoM of 160.4dB.

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