A 0.137 mm^2 9 GHz Hybrid Class-B/C QVCO With Output Buffering in 65 nm CMOS

Md. Tawfiq Amin, *Student Member, IEEE*, Pui-In Mak, *Senior Member, IEEE*, and Rui P. Martins, *Fellow, IEEE*

***Abstract*—A compact realization of hybrid class-B/C quadrature voltage-controlled oscillator (QVCO) with output buffering is proposed. It employs a four-phase amplitude detector feedback loop to shift the operation mode from hybrid class-B/class-C to class-C after power up. The power-efficient class-C core allows quadrature-locking via passive capacitive coupling, whereas the auxiliary class-B core ensures a robust startup. For higher output drivability, PMOS-based source followers are stacked atop the QVCO for reusing its bias current and avoiding any AC-coupling networks. The buffered QVCO can directly drive up the 50-Ω port of testers, or to withstand a large capacitive load in on-chip signal distribution. The fabricated 9 GHz QVCO in 65 nm CMOS draws 10.5 mW and exhibits −99.37-dBc/Hz phase noise at 1 MHz offset. The active area is just 0.137 mm^2 by using two compact spiral inductors with patterned ground shields.**

***Index Terms*—Buffer, CMOS, class-B, class-C, phase noise, quadrature voltage-controlled oscillator (QVCO).**

I. Introduction

QUADRATURE voltage-controlled oscillator (QVCO) is a primary choice of high-speed four-phase local oscillator (LO) generation in wireline (e.g., clock and data recovery) and wireless (e.g., phased-array receivers) communication systems [1], [2]. To lower the power, the negative transconductor can be operated at the class-C mode [3], but at the risk of long startup time or non-oscillation against process variations. To surmount this, different approaches on class-C VCOs [4]–[6] or a hybrid class-B/C VCO [7] have been studied. For the latter, the class-C core secures steady-state oscillation with low phase noise, while the auxiliary class-B core [7] aids the startup. Yet, the current ratio between the class-B and class-C cores still pose a tight tradeoff among the startup time, phase noise and power.

This work is a compact hybrid class-B/C QVCO suitable for on-chip LO distribution such as multi-channel transceivers that have local buffers to recover the signal swing before driving the I/Q mixers of each channel. The main function of the merged buffer is to overcome the parasitics of the layout routing and drive up the local buffers similar to [8], but it is a class-B VCO-buffer without the quadrature locking issue. The design details of this work are presented next.

Manuscript received May 26, 2014; revised July 20, 2014; accepted July 22, 2014. Date of publication August 06, 2014; date of current version October 02, 2014. This work was supported by the University of Macau MYRG114(Y1-L4)-FST13-MPI and the Macao Science and Technology Development Fund (FDCT).

M. T. Amin and P.-I. Mak are with the State-Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macao, China (e-mail: pimak@umac.mo).

R. P. Martins is with the State-Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macao, China and also with the Instituto Superior Técnico (IST)/U of Lisbon, Lisbon, Portugal (e-mail: rmartins@umac.mo).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LMWC.2014.2344449

II. Proposed Hybrid Class-B/C QVCO

The proposed hybrid class-B/C QVCO is depicted in Fig. 1. With a coupling capacitor $C_{\rm C}$ (1 pF) between the class-C cores of two VCOs ($\rm VCO_1$ and $\rm VCO_2$), they can be quadrature-locked under their 2nd harmonics generated at their common-source nodes $V_{\rm S1,C}$ and $V_{\rm S2,C}$. Considering $\rm VCO_1$, the negative transconductor is a parallel structure of class-B ($M_{\rm B1,2}$: $20/0.06$ μm) and class-C ($M_{\rm C1,2}$: $160/0.06$ μm) NMOS transistors. For lower power and phase noise, 80% of the bias current ($I_{\rm bias,C}$) is assigned to the class-C core, while $V_{\rm bias}$ can be set below the threshold voltage of $M_{\rm C1,2}$. To ensure a reliable startup, 20% of the bias current ($I_{\rm bias,B}$) is reserved for the class-B core that is biased at a higher dc level copying from $V_{\rm IP}$ and $V_{\rm IN}$. The two bias current sources $M_{\rm bias,C}$ ($88/1.0$ μm) and $M_{\rm bias,B}$ ($12/1.0$ μm) are optimized to closely fit the size ratio of $M_{\rm C1,2}$ to $M_{\rm B1,2}$, and with a long channel length to reduce their $1/f$ noise. The former uses a static gate bias, whereas the latter uses a dynamic one ($V_{\rm PD}$) to accelerate the quadrature-locking time. $V_{\rm PD}$ is offered by an amplitude detector that monitors the four-phase QVCO outputs ($V_{\rm IP}, V_{\rm IN}, V_{\rm QP}, V_{\rm QN}$) simultaneously, and negatively feedback the amplitude information to $M_{\rm bias,B}$ to assist the startup. When carrying the full swing of current, the lack of source feedback pushes $M_{\rm C1,2}$ slightly out of the saturation region at the maximum level. Thus, the bias current should be optimized to ensure class-C operation for the full output swing. When two VCOs are quadrature-locked, they will operate in a tail-current shaping mode that raises their output amplitude and lowers their phase noise [9]. In fact, the benefits of class-C QVCO is not as high as that of class-C VCOs [4]–[6] when there is no big capacitance in parallel with the current sources $M_{\rm bias,C}$. In overall, 25% reduction of bias current is expected from simulations when compared with a typical class-B QVCO with identical performances.

To further save power when delivering the high-frequency outputs to the load, the bias current can be further reused by stacking the QVCO with its output buffers, which can be a simple PMOS-based source follower. With it, the QVCO can be biased in the current-limiting region, while avoiding $M_{\rm B1,2}$ and $M_{\rm C1,2}$ from overdriving by the peak output swing. Also the PMOS-based buffer matches its input common-mode level with the QVCO's output one. Thus, no AC-coupling is entailed that otherwise degrades the LC tank's Q factor, and penalizes the die area and parasitics. The noise coupling between the QVCO

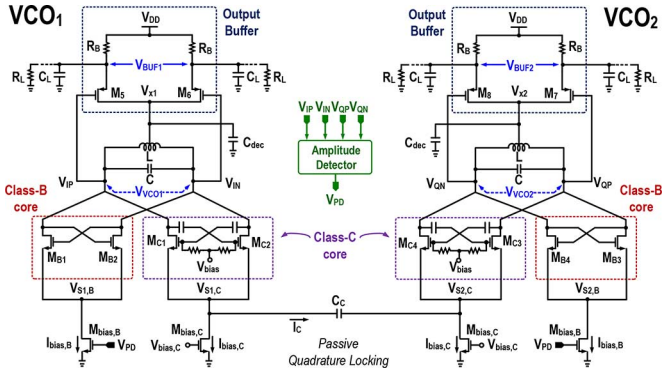

Fig. 1. Proposed hybrid Class-B/C QVCO (bottom) current-reused with its buffers (top) for better output drivability at small power.

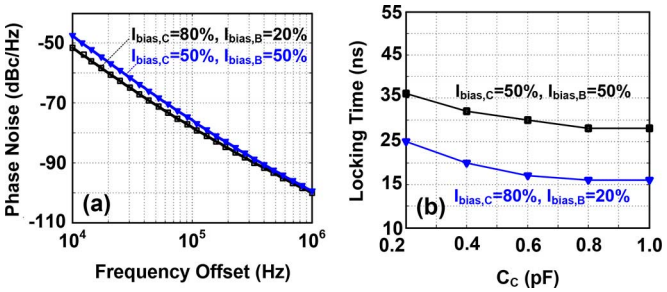

Fig. 2. Simulated (a) phase noise for different set of bias current drained by the class-B/C cores, and (b) locking time with respect to the size of $C_{\rm C}$. The carrier frequency is 9.34 GHz.

and buffers can be managed by adding a decoupling capacitor ($C_{\rm dec}$ = 3 pF) between $V_{\rm x1,2}$ to ground. To save area, the *LC* tank adopts two small differential spiral inductor (0.5 nH) for the oscillation frequency (ω_0) at ∼9 GHz.

A. Hybrid Class-B/C QVCO Using Capacitive Coupling

The 2nd harmonics are produced at the common-source nodes of both $\rm VCO_1$ and $\rm VCO_2$ due to the mixing property of cross-coupled NMOS switches. Thus, all $V_{\rm S1,B}$, $V_{\rm S2,B}$, $V_{\rm S1,C}$ and $V_{\rm S2,C}$ oscillate at $2\omega_0$. Since most currents are drained by the two class-C cores, the capacitive coupling should be placed on them to maximize the coupling strength for minimum phase error. The optimal ratio of current drained by the class-B and class-C cores should account the quadrature accuracy, power and phase noise. We plot the phase noise under two sets of bias current in Fig. 2(a). For 80%-$I_{\rm bias,C}$ and 20%-$I_{\rm bias,B}$, the phase noise at 100-kHz to 10 MHz offset is ∼2 dB better when comparing with that under 50%-$I_{\rm bias,C}$ and 50%-$I_{\rm bias,B}$. When sizing $C_{\rm C}$, it must ensure the quadrature accuracy with the lowest possible locking time. $C_{\rm C}$ is swept from 0.2 to 1 pF as shown in Fig. 2(b) to assess the locking time behavior. For the employed 80%-$I_{\rm bias,C}$ 20%-$I_{\rm bias,B}$ current ratio, the QVCO locks at 16 ns at $C_{\rm C}$ = 0.8 pF. At the same size of $C_{\rm C}$, the locking time takes 28 ns for the 50%-$I_{\rm bias,C}$ 50%-$I_{\rm bias,B}$ design. Thus, shorter locking time and lower phase noise can be concurrently achieved under the used current ratio.

B. Amplitude-Detector Feedback Loop

The 4-phase amplitude detector [Fig. 3(a)] is to monitor the oscillation amplitude via the transistors $M_{\rm d1\text{-}4}$. The capacitor $C_{\rm d}$ can be simply the parasitic to maximize the speed of the loop. Specifically, during the startup, the common-source node

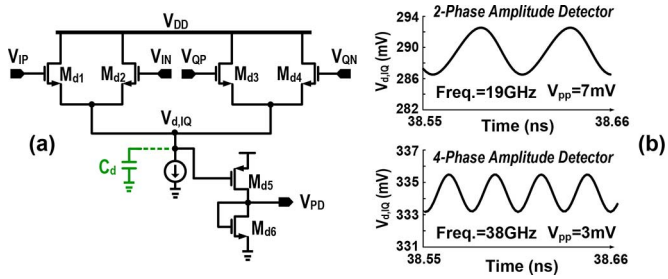

Fig. 3. (a) Schematic of the proposed four-phase amplitude detector. (b) Simulated outputs for two-phase operation with a VCO (upper) and proposed four-phase operation for a QVCO (lower).

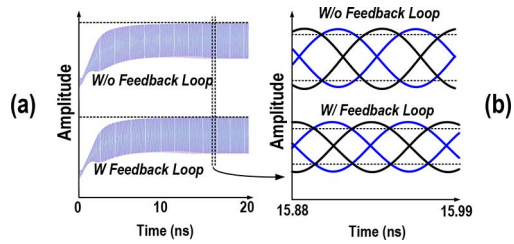

Fig. 4. (a) Simulated transient waveform of the QVCO with and without the feedback loop to enhance the amplitude and phase balancing during the startup. (b) Zoom view of (a) at ∼16 ns.

of $M_{\rm d1\text{-}4}$ responds to the peak amplitude of $V_{\rm IP}$, $V_{\rm IN}$, $V_{\rm QP}$ and $V_{\rm QN}$, and integrates them into $C_{\rm d}$ to smooth $V_{\rm d,IQ}$. Thus, any amplitude and phase imbalances between $V_{\rm IP}$, $V_{\rm IN}$, $V_{\rm QP}$ and $V_{\rm QN}$ will generate an irregular waveform at $2\omega_0$ superpositioned on $V_{\rm d,IQ}$, triggering the feedback loop. To save power and attain a high sensitivity, $M_{\rm d1\text{-}4}$ can be biased in the subthreshold region. In Monte-Carlo simulations, only small variations of QVCO's output swing and phase noise were found, given that they are dominated by the class-C core in the steady state. $V_{\rm d,IQ}$ is inverted and amplified by $M_{\rm d5,6}$ before driving to the tail current source of the class-B core ($M_{\rm bias,B}$), which injects the cancelling signal back to the QVCO. $M_{\rm d5,6}$ not only gives extra design flexibility but also handily makes the loop a negative feedback.

A large $C_{\rm d}$ could reduce the ripple at $V_{\rm d,IQ}$, but with a slow response time. Since the 4-phase amplitude detector can push the ripple frequency to $4\omega_0$, its amplitude is heavily suppressed due to the limited bandwidth at $V_{\rm d,IQ}$. Thus, the tradeoff between the size of $C_{\rm d}$ and to the startup time is more alleviated in QVCO (4 phases) than VCO (2 phases) as shows in Fig. 3(b), where the 4-phase operation shows 57% less ripple.

The class-B core is to ensure a reliable and fast startup for the QVCO. Once the QVCO enters into the steady state, the class-C core will dominate the operation. Thus, the phase noise will be further desensitized from the residual ripple at $V_{\rm d,I/Q}$ that only drives the non-dominant class-B core. The simulated transient waveforms are shown in Fig. 4(a) and (b), showing the startup states under conventional two-phase and proposed four-phase amplitude detectors. For the latter, the QVCO locks at 16 ns with balanced oscillation amplitude and phase. For the former, unbalanced amplitude and phase are still observed at 16 ns (it eventually takes ∼20 ns to lock properly).

C. Inherent Output Buffering for Better Drivability

Output buffering should deliver adequate output swing to the load, while offering adequate isolation between the load and

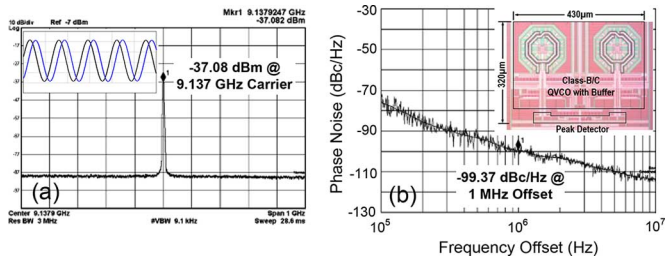

Fig. 5. Measured (a) output spectrum and quadrature-output waveforms, and (b) its phase noise and chip photo.

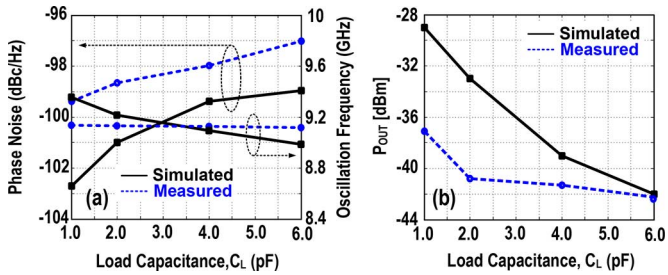

Fig. 6. Simulated and measured performances versus C_L variations: (a) phase noise and oscillation frequency. (b) Output power. Note that the output power is low due to the 50-Ω load in tests.

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART

.	[10]	[11]	This Work
Technology	0.18 μm CMOS	0.13 μm CMOS	65 nm CMOS
Topology	Class-B QVCO	Class-B QVCO	**Class-B/C QVCO**
Freq., f_{osc} (GHz)	8	10	9.14
Power, P_{diss} (mW)	14.9	14.4	10.5
Phase Noise, L(Δf) (dBc/Hz)	-94.7 @ 1 MHz	-95.0 @ 1 MHz	-99.37 @ 1 MHz
Active Area (mm^2)	6.4	0.162	**0.137**
FoM [1]	161.5 (VCO only)	163.4 (VCO only)	**168.3 (VCO+Buffer)**
FoM_A [2]	152.9 (VCO only)	171.3 (VCO only)	**177.0 (VCO+Buffer)**

QVCO core. The size of $M_{5\text{-}8}$ was chosen as $140/0.24$ μm to achieve $g_{m5\text{-}8} = 12$ mS, and R_B was set as 120 Ω.

D. Area of Inductor and Performance Tradeoffs

For a 0.5 nH inductor (L) with a patterned ground shield in 65 nm CMOS, the simulated quality factor is ∼13 with the simulated phase noise is −104 dBc/Hz at 1 MHz offset, while the area is 155×150 μm^2. If L is upsized to 1 nH, the quality factor is ∼18 and phase noise is −110 dBc/Hz at 1 MHz offset. Yet, the area including the layout boundary for isolation has to be doubled (215×210 μm^2). Thus, the chosen L is 0.5 nH. $L = 1$ nH is a power-efficient option if targeting lower phase noise.

III. MEASUREMENT RESULTS

The QVCO fabricated in 65 nm CMOS occupies 0.137 mm^2. There is no startup problem for all test chips and after many times of power-ON/OFF. The QVCO under test directly drives up the 50-Ω port of the equipment. The output spectrum along with the quadrature waveforms are shown in Fig. 5(a). The steady-state amplitude and phase errors are ∼0.3 dB and ∼5°, respectively. Fig. 5(b) shows the chip photo and phase noise which is −99.37 dBc/Hz at 1 MHz offset, and −113.5 dBc/Hz at 10 MHz offset. The QVCO is tested over a wide range of C_L from 1 to 6 pF [Fig. 6(a) and (b)]. Note that the output power is low due to the 50-Ω load in tests, but it is not required in on-chip LO distribution. The phase noise variation is limited to ∼2 dB, with a trend similar to the simulated values. The bondwire and PCB parasitics should account for other discrepancy. No frequency tuning is adopted for this prototype, but it can be added with additional varactors in parallel with the *LC* tank. The QVCO draws 10.5 mW at 1.4 V (9.66 mW in simulations). A comparison with the prior art is given in Table I [10], [11].

IV. CONCLUSION

This letter reported a compact QVCO using a hybrid class-B/C negative transconductor to enhance the power efficiency. The optimized current ratio (20% for class-B, 80% for class-C) allows passive quadrature-locking of the two VCOs via adding a coupling capacitor between the primary class-C cores, resulting in low phase. The auxiliary class-B core is monitored by a four-phase amplitude-detector feedback loop to accelerate the quadrature-locking during the startup, while inducing only a small ripple in the steady state. The QVCO also features a current-reuse output buffer stacked atop of it to enhance the output drivability. The 65 nm CMOS prototype directly driving the 50 Ω testers shows 9.14 GHz oscillation frequency, 10.5 mW of power and −99.37 dBc/Hz phase noise at 1 MHz offset.

REFERENCES

[1] I.-S. Shen, T.-C. Huang, and C. F. Jou, "A low phase noise quadrature VCO using symmetrical tail current-shaping technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 7, pp. 399–401, Jul. 2010.
[2] S. L. Jang, S. S. Huang, C. F. Lee, and M. H. Juang, "CMOS quadrature VCO implemented with two first-harmonic injection-locked oscillators," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 10, pp. 695–697, Oct. 2008.
[3] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs with a general result on phase noise," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.
[4] K. Okada, Y. Nomiyama, R. Murakami, and A. Matsuzawa, "A 0.114-mW dual-conduction class-C CMOS VCO with 0.2-V power supply," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2009, pp. 228–229.
[5] W. Deng, K. Okada, and A. Matsuzawa, "Class-C VCO with amplitude feedback loop for robust start-up and enhanced oscillation swing," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 429–440, Feb. 2013.
[6] J. Chen, F. Jonsson, M. Carlsson, C. Hedenas, and L. R. Zheng, "A low power, start-up ensured and constant amplitude class-C VCO in 0.18 μm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 8, pp. 427–429, Aug. 2011.
[7] L. Fanori, A. Liscidini, and P. Andreani, "A 6.7-to-9.2 GHz 55 nm CMOS hybrid class-B/class-C cellular TX VCO," in *Proc. IEEE ISSCC*, Feb. 2012, pp. 354–355.
[8] M. T. Amin, P.-I. Mak, and R. P. Martins, "A 3.6 mW 6 GHz current-reuse VCO-buffer with improved load drivability in 65 nm CMOS," *Int. J. Circuit Theory Appl.*, to be published.
[9] B. Soltanian and P. Kinget, "A low phase noise quadrature LC VCO using capacitive common-source coupling," in *Proc. IEEE ESSCIRC*, Sep. 2006, pp. 436–439.
[10] Y. J. The, Y. Zheng, and W. G. Yeoh, "A 0.18 μm CMOS 8 GHz quadrature VCO for UWB application," in *Proc. IEEE Int. Conf. Ultra-Wideband*, Sep. 2007, pp. 636–639.
[11] S. Li, I. Kipnis, and M. Ismail, "A 10 GHz CMOS quadrature LC-VCO for multicore optical applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1626–1634, Oct. 2003.