A Sine-LO Square-Law Harmonic-Rejection Mixer—Theory, Implementation, and Application

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***Abstract*—A square-law harmonic-rejection mixer (SL-HRM) driven by a sine local oscillator (LO) is proposed for *wideband* and *tunable* rejection of all LO harmonics. The key performances including the gain, noise figure (NF), input-referred third-order intercept point (IIP3), and harmonic rejection ratio (HRR) with respect to the amplitude and purity of the sine-LO are analyzed. In the circuit level, the SL-HRM incorporates a voltage-boosted technique to surmount the gain and NF penalties of square-law mixing, while guaranteeing the device reliability via introducing a supply startup circuit and a node-voltage protection circuit. The entailed high-purity sine-LO is achieved via a digital-intensive square-to-sine LO generator plus a passive-RC low-pass filter. Fabricated in 65-nm CMOS, the VHF-/UHF-band SL-HRM has a tunable gain of 1–13 dB, associated with an NF of 27–15 dB, under an LO amplitude of 50–200 mV_{pp}. The IIP3 is stable within from $+6.5$ to $+7.6$ dBm, as expected. The tunable HRR_3 and HRR_5 are 13–40 dB and 17–45 dB, respectively. The mixer core consumes 7.5 mW at 2.5 V, while the LO generator draws 3–6 mW at 1.2 V. The total active area is just 0.042 mm^2.**

***Index Terms*—Active mixer, CMOS, gain, harmonic rejection, input-referred third-order intercept point (IIP3), noise figure (NF), sine local oscillator (LO), square law, voltage boosted, wideband.**

I. Introduction

THE harmonic-mixing problem complicates the design of wideband multi-standard transceivers, such as the software-defined radios (SDRs) and cognitive radios (CRs) [1], [2]. In a wireless receiver, the sensitivity is mainly limited by its noise figure (NF). Thus, the forefront low-noise amplifier (LNA) and mixers should feature high gain and low noise. These requests promote the use of an active mixer driven by an adequately large local oscillator (LO) for *hard-switching* (HS) *mixing*. The induced harmonic-mixing problem was not so critical in the past, as a single-standard design can resort from a surface acoustic wave (SAW) filter to band-limit the RF input signal. Thus, most research efforts were focused on HS mixing. Yet, the harmonic mixing is getting much severe in wideband down-conversion because any high-power blockers located at the harmonic frequencies of the LO will become the co-channel interferers. Since the equivalent LO of HS is like a square wave, the power of the odd-order harmonics decays gradually. The inherent harmonic rejection ratio (HRR) is associated with the harmonic number, e.g., a blocker located at the third (fifth) harmonic of the LO experiences a 9.5-dB (14-dB) rejection.

To enhance the blocker resilience of wideband systems, a number of techniques have been reported to enhance the HRR. The three-path eight-phase harmonic-rejection mixer (HRM) (3P-8P HRM) can reject the critical third and fifth harmonics by signal cancellation [3], and has been widely utilized in TV band applications [4]–[6]. Although the added hardware complexity is reasonable, a higher HRR and rejecting more harmonics are essential for SDR or CR that covers a decade-wide or more spectrums. Increasing further the numbers of path and phase significantly raises the design complexity in this kind of HRM.

This paper proposes a square-law harmonic-rejection mixer (SL-HRM) incorporating a sine-LO for *wideband* and *tunable* rejection of all LO harmonics in a compact single-branch double-balanced mixer. The sine-LO is created through a digital-intensive square-to-sine LO generator plus a passive-RC low-pass filter (LPF); both induce low hardware overhead. The LO generator can interface directly with a voltage-controlled oscillator (VCO), or after a frequency divider that is widely required to extend the LO coverage and generate the I/Q outputs for quadrature down-conversion.

Though square-law (SL) mixing has been studied in the past, such as [7], wideband receivers were uncommon by that time. To our knowledge, there is no theoretical or experimental effort on analyzing the HRR with respect to sine-LO mixing and its consequences to other parameters, such as gain, linearity, and NF. This work addresses those aspects in details and provides the experimental proofs.

Following this Introduction, Section II reviews the state-of-the-art HRMs and highlights the uniqueness of the proposed SL-HRM. Section III analyzes the key performances of the SL-HRM with the emphasis put in the LO. Section IV presents the circuits design of a voltage-boosted SL-HRM, a supply startup circuit, a node-voltage protection circuit, and finally, a square-to-sine LO generator. The experimental results are summarized in Section V, and the potential applications and conclusions are drawn in Sections VI and VII, respectively.

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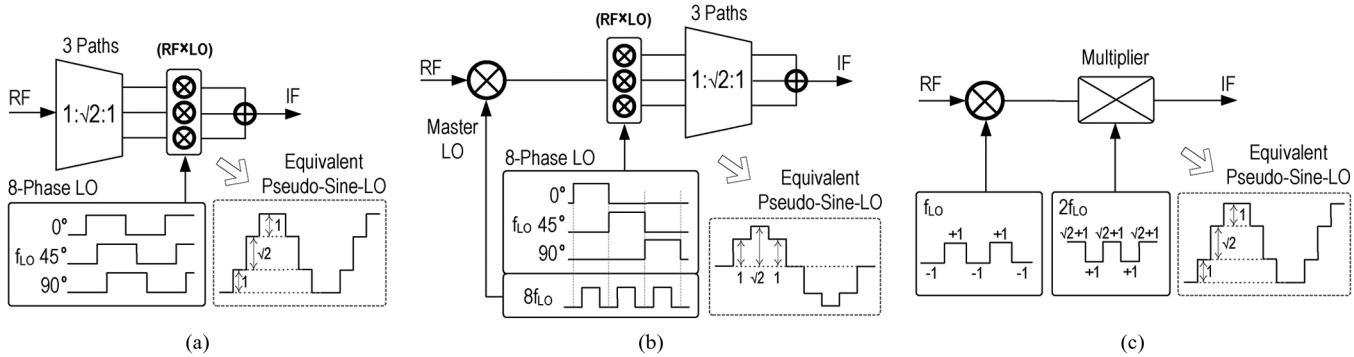

Fig. 1. Block schematics of the existing: (a) 3P-8P HRM, (b) rotational HRM, and (c) switched-load HRM.

II. Review of the State-of-the-Art HRMs and Basic Principles of the Proposed Solution

This section overviews the state-of-the-art HRM topologies and outlines the basic principle of the proposed SL-HRM.

A. 3P-8P HRM [3]

This is the initial version of multi-path poly-phase HRM [see Fig. 1(a)] intended to reject the most critical third and fifth harmonics. The equivalent pseudo-sine-LO is approximated through proper gain-weighting the three signal paths with $1:\sqrt{2}:1$, and summation of their IF outputs after phase shifts by an eight-phase LO (i.e., 45° resolution) at the LO frequency $(f_{\rm LO})$. This 3P-8P HRM, together with HS mixing, has high gain and low NF, but the $\rm HRR_{3,5}$ is limited to around 30–35 dB for 1° phase and 1% gain errors. It is possible with proper circuit techniques to extend the HRR [8] and the number of rejecting harmonics [9], but the hardware complexity is raised considerably as well. Thus, the HRR is a tradeoff with the circuit complexity, impacting the operating frequency, die area, and power [8], [9].

B. Rotational HRM [9]

This rotational HRM [see Fig. 1(b)] employs a high-frequency one-phase master LO rotating to a set of HS mixers via a low-frequency eight-phase LO. Thus, the effective mixing waveform is only determined by the master LO, minimizing the phase error. The gain weighting $(1:\sqrt{2}:1)$ is delayed to the baseband, which facilitates device matching. Comparing with the 3P-8P HRM, this topology is more robust, but the design tradeoff is similar to that of 3P-8P HRM when targeting a higher HRR and on more harmonics.

C. Switched-Load HRM [10]

Unlike the previous two HRMs that are based on vector summation, this switched-load HRM [see Fig. 1(c)] employs vector multiplication to approximate a pseudo-sine-LO. A single HS mixer is driven by a one-phase LO like a conventional mixer, but its load is switched by a $2f_{\rm LO}$ functioning like a multiplier. The amplitude of the $2f_{\rm LO}$ LO is equivalent as 1 and $\sqrt{2}+1$. This topology has the benefit of circuit simplicity, but the rejecting harmonic is still limited to the fifth. The HRR would also likely be limited by both the gain and phase mismatches.

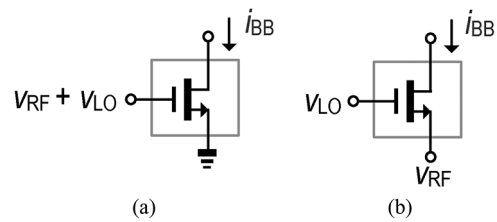

Fig. 2. Basic principles of SL mixing in a single transistor. (a) Work [11]. (b) Basis of this work.

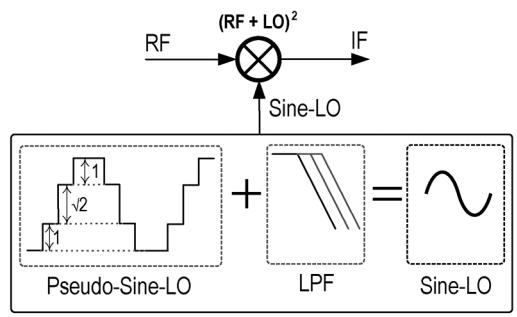

Fig. 3. Proposed sine-LO SL-HRM.

D. Basic Principle of the Proposed Sine-LO SL-HRM

The SL-HRM uses a fundamentally different principle. If two small signals RF $(v_{\rm RF})$ and LO $(v_{\rm LO})$ are applied to one MOSFET, as shown in Fig. 2(a) [11] and (b) (basis of this work), the squaring function of the voltage-to-current (*V–I*) conversion can realize downconversion, as squaring the sum or difference of two signals can generate a product term $v_{\rm RF}\times v_{\rm LO}$. Thus, to be described later, with the same topology as a typical active mixer, the use of a high-purity sine-LO can lead to more HRR, and the rejection is on *all* unwanted LO harmonics. Comparing the two options in Fig. 2(a) and (b), the latter is preferred as it can avoid the area-hungry LC combiner [11] for passively pre-summing $v_{\rm RF}$ and $v_{\rm LO}$.

The block schematic of the proposed SL-HRM is depicted in Fig. 3. As mentioned, the RF and sine-LO signals are summed and squared to generate the IF output under SL mixing. A sine-LO is generated through passive interpolating a set of multi-phase square-wave LOs, and then low-pass filtering to minimize the harmonic contents. The LO path is easier to be

TABLE I
COMPARISON OF STATE-OF-THE-ART HRMS WITH THE PROPOSED SINE-LO SL-HRM

	3P-8P HRM [3]	Rotational HRM [9]	Switched Load HRM [10]	Sinel-LO SL-HRM (This Work)
Mixer Architecture	Multi-Signal Path + RF Gain Weighting	Multi-Signal Path + Baseband Gain Weighting	Single-Signal Path + Gain Weighting Load	Single-Signal Path
LO	Poly-Phase LO	Single-Phase Master LO + Poly-Phase Secondary LO	Two Single-Phase LOs	Sine-LO
Mixing Type	Hard Switching	Hard Switching	Hard Switching	Square Law
Rejected Harmonics	N – 3	N – 3	N – 3	All

N: The number of LO phase.

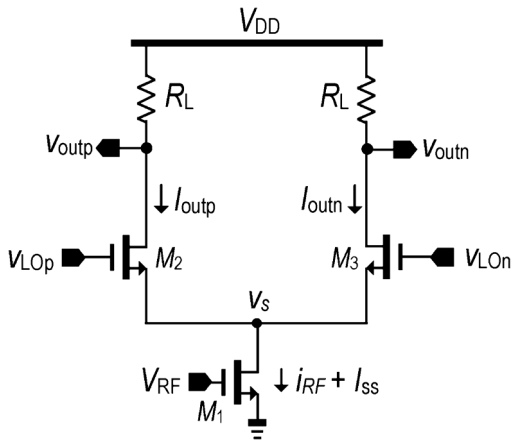

Fig. 4. Single-balanced active mixer under SL mixing (simplified).

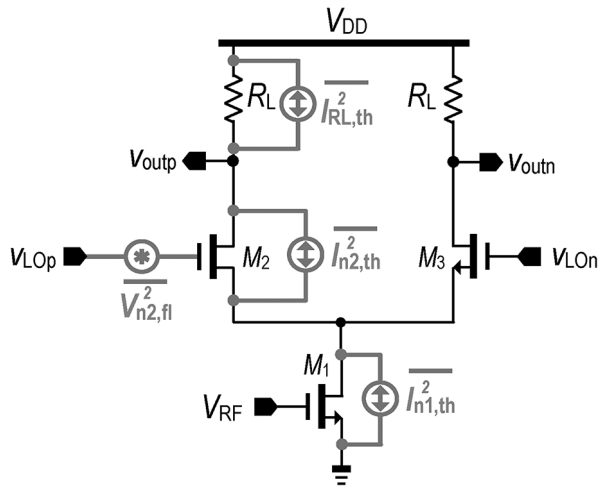

Fig. 5. Simplified noise model of active mixer under SL mixing.

optimized as it is independent from the signal path. A comparison of this solution to those in Fig. 1(a)–(c) is summarized in Table I.

III. ACTIVE MIXER PERFORMANCES WITH A SINE-LO

This section analyzes the gain, NF, input-referred third-order intercept point (IIP3), and HRR of the proposed SL-HRM with respect to the LO.

A. Gain

We use a single-balanced active mixer (Fig. 4) to simplify the analysis. It can be decomposed into a transconductor (M_1), a mixing quad $(M_{2,3})$, and a load (R_L). The LO signals ($v_{\mathrm{LO}p}$ and $v_{\mathrm{LO}n}$) are assumed to be a sine-wave, M_2 and M_3 operate like a differential amplifier, with their common source node (v_s) modulated by v_{RF} as given by

$$v_s = -\frac{g_{1,\mathrm{RF}}}{2g_{1,mx}} v_{\mathrm{RF}} \tag{1}$$

where $g_{1,\mathrm{RF}}$ is the transconductance of M_1 and $g_{1,mx}$ is the trans-conductance of M_2 (M_3). By using Taylor series, the small-signal currents $i_{\mathrm{out}p}$ and $i_{\mathrm{out}n}$ can be approximated as

$$\begin{cases} i_{\mathrm{out}p} = g_{1,mx}(v_{\mathrm{LO}p} - v_s) + g_{2,mx}(v_{\mathrm{LO}p} - v_s)^2 \\ i_{\mathrm{out}n} = g_{1,mx}(v_{\mathrm{LO}p} - v_s) + g_{2,mx}(v_{\mathrm{LO}n} - v_s)^2 \end{cases} \tag{2}$$

where the higher order terms beyond two are omitted and $g_{2,mx}$ is the second-order transconductance coefficient of M_2. Assuming $v_{\mathrm{LO}p} = -v_{\mathrm{LO}n} = v_{\mathrm{LO}}$, (2) leads to a differential output current as given by

$$i_{\mathrm{out}p} - i_{\mathrm{out}n} = 2v_{\mathrm{LO}} g_{1,mx} - 4g_{2,mx} v_{\mathrm{LO}} v_s. \tag{3}$$

Note that the term $2v_{\mathrm{LO}} g_{1,mx}$ will be cancelled for a *double-balanced* active mixer, leaving the desired term $4g_{2,mx} v_{\mathrm{LO}} v_s$ that leads to the gain

$$A_v = \frac{g_{1,\mathrm{RF}}}{2g_{1,mx}} g_{2,mx} A_{\mathrm{LO}} (R_L // r_{o2}) \tag{4}$$

where r_{o2} is the output resistance of M_2 and A_{LO} is the LO amplitude. Equation (4) essentially shows that, under SL mixing, the gain of the mixer is linearly controllable by the LO amplitude.

B. NF

The noise contribution of the transconductor and mixing quad are analyzed based on the simplified noise model shown in Fig. 5. For the transconductor, its flicker noise is up-converted to the LO frequency and to its odd harmonics, being negligible in a direct down-conversion receiver. The flicker noise of the transconductor contributes only with a small portion to the overall NF (only when there is component mismatch among the mixing quad). For the mixing quad, its flicker noise $(2\overline{V_{n2,fl}^2})$ will be multiplied by a factor $[g_{1,mx}(R_L // r_{o2})]^2$ when appearing at the output. For the conventional HS mixing, increasing the mixing quad's device size (W and L) can min-

imize $\overline{V_{n2,fl}^2}$, but it will increase the power of the LO driving buffers. Differently here, under SL mixing, only a small $A_{\rm LO}$ is entailed, surpassing such a tradeoff while reducing the LO leakages to the RF and IF ports.

The thermal noise of the transconductor accompanies the RF signal being translated to the same IF. Due to SL mixing, the thermal noise at the LO odd harmonics is suppressed. The thermal noise induced by M_1 ($\overline{I_{n1,th}^2}$) will be multiplied by a noise aliasing factor $4n_aA_v^2/g_{1,\rm RF}^2$ when appearing at the output. Since the HRR of SL mixing is much improved when compared with its HS counterpart, the noise aliasing due to LO harmonics is also smaller. In other words, SL mixing also reduces noise aliasing due to better HRR of all harmonics. For the mixing quad, their thermal noise ($2\overline{I_{n2,th}^2}$) will be multiplied by a factor of $[(R_L//r_{o2})]^2$ when appearing at the differential output. The load contributes with noise to the output directly. Taking all those noise sources into account, the NF of SL mixing in a double-balanced SL-HRM can be calculated, using a test source with an impedance of R_s, shown in (5) at the bottom of this page, where the noises of R_s and the input resistor for impedance matching are not shown for simplicity; k is the Boltzmann constant; T is the absolute temperature; γ is a noise factor; $\overline{V_{n2,fl}^2}$ is the flicker noise of M_2; and n_a is a noise aliasing factor given by

$$n_a = 2\left[1+\sum_{n=3}^{+\infty}\left(\frac{1}{\rm HRR_n}\right)^2\right], \qquad n=3,5,7\ldots \tag{6}$$

where $\rm HRR_n$ stands for the nth-order HRR, and (5) shows the monotonic decreasing function of NF with the LO amplitude, consistent with the gain expression in (4). Observing the second term of (5) that is the thermal and flicker noises generated by the mixing quad, a small $A_{\rm LO}$ can penalize the NF. To be described in Section IV, the gain and NF penalties of SL mixing can be surmounted through proper circuit techniques.

C. IIP3

For deriving the IIP3, the output current with Taylor-series expansion is employed,

$$\begin{aligned} i_{\rm out} &= i_{{\rm out}p} - i_{{\rm out}n} \\ &= f(v_{\rm LO}, v_{\rm RF}) \\ &= \sum_{n=0}^{+\infty}\sum_{p=0}^{+\infty}(a_{n,p}\cdot v_{\rm LO}^n v_{\rm RF}^p) \end{aligned} \tag{7}$$

where the coefficient $a_{n,p}$ is

$$a_{n,p} = \frac{1}{n!p!}\frac{\partial^{n+p}f(0,0)}{\partial v_{\rm LO}^n \partial v_{\rm RF}^p}. \tag{8}$$

According to the IIP3 definition [12],

$$A_{\rm IIP3} = \sqrt{\frac{4}{3}\left|\frac{a_{1,1}}{a_{1,3}}\right|}. \tag{9}$$

Thus, the IIP3 is primarily related to the modulation between the transconductor and mixing quad, and should be adequately stable against the LO.

D. HRR

Assuming that the desired signal and blocker located at LO harmonics are single tones, the product $[v_{\rm LO}^n \cdot v_{\rm RF}]$ in (7) can be discussed. The nth power of $v_{\rm LO}$ downconverts the input RF signal $v_{\rm RF}$ of frequency $f_{\rm RF}$ to IF, resulting in expansion terms with frequencies ranging from $(f_{\rm LO}-f_{\rm RF})$ to $(nf_{\rm LO}-f_{\rm RF})$. With it, the nth-order HRR can be derived,

$$\rm HRR_n = \frac{H_1 + \sum_{i=3}^{+\infty}(2^{i-1}\cdot d_{1,i}\cdot H_i)}{H_n + \sum_{j=n+2}^{+\infty}(2^{j-1}\cdot d_{n,j}\cdot H_j)}, \qquad i,n=3,5\ldots \tag{10}$$

where

$$d_{n,j} = \frac{1}{2^{j-1}}\frac{j!}{\left(\frac{j+n}{2}\right)!\left(\frac{j-n}{2}\right)!} \tag{11}$$

$$H_n = \frac{a_{n,1}}{2^n}A_{\rm LO}^n A_{\rm RF}. \tag{12}$$

It can be proven that the higher order terms in the summations of (10) are negligible, yielding

$$\rm HRR_n \approx \frac{H_1}{H_n} = 2^{n-1}\cdot\frac{a_{1,1}}{a_{n,1}}\cdot\frac{1}{A_{\rm LO}^{n-1}}. \tag{13}$$

This indicates that $\rm HRR_n$ is inversely proportional to $(n-1)$th power of the LO amplitude, showing the *tunable* and *wideband* harmonic-rejection ability of SL mixing.

IV. Circuits Design and Implementation

A. Proposed Voltage-Boosted SL-HRM

In nanoscale CMOS such as the employed 65-nm node, dual-oxide transistors (thick and thin) and dual supplies (2.5-V I/O and 1.2-V core) are commonly available to facilitate the circuits

$$\rm NF \approx 10\log\left[\frac{1}{kTR_s}\left(\underbrace{2n_a\frac{4kT\gamma}{g_{1,\rm RF}}}_{\rm Transconductor} + \underbrace{\frac{16kT\gamma g_{1,mx}^3 + 4g_{1,mx}^4\cdot\overline{V_{n2,fl}^2}}{g_{1,\rm RF}^2 g_{2,mx}^2 A_{\rm LO}^2}}_{\rm Mixing\ Quad} + \underbrace{\frac{16kTg_{1,mx}^2}{g_{1,\rm RF}^2 g_{2,mx}^2 A_{\rm LO}^2 R_L}}_{\rm Load}\right)\right] \tag{5}$$

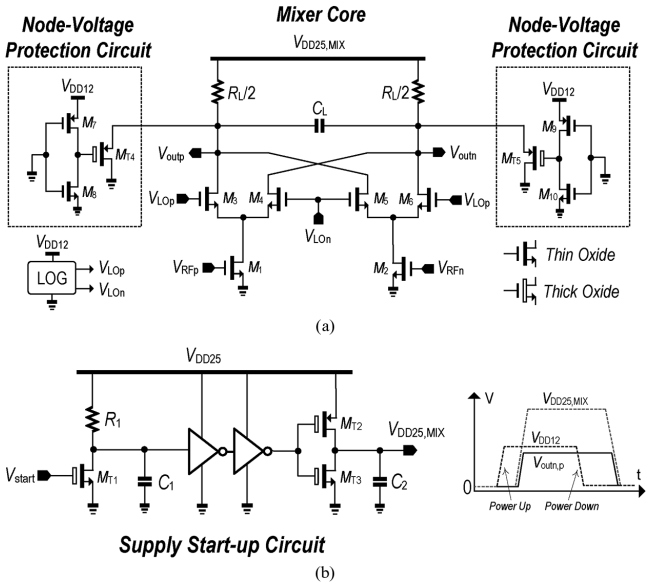

Fig. 6. Schematic of the proposed SL-HRM. (a) Mixer core and its node-voltage protection circuits. (b) Supply startup circuit.

design, enabling many mixed-voltage mixed-transistor circuit techniques [1], [13], [14]. For a double-balanced SL-HRM [see Fig. 6(a)] featuring an input transconductor (M_{1-2}), a mixing quad (M_{3-6}), and a load (R_L, C_L) in cascode, it is feasible to elevate the supply to 2.5 V such that more gain and lower NF can be achieved, without sacrificing the dynamic range. Of course, the circuit reliability must be taken into account to ensure all devices are not overstressed at all times. To achieve it, in the steady state, a proper bias assignment can let all terminal voltages ($V_{\rm GS}, V_{\rm GD}, V_{\rm DS}$ of each MOSFET) be within the reliability limits, e.g., 1.2 V for the thin-oxide MOSFETs. For the power-up/-down transients, a supply startup circuit [see Fig. 6(b)] similar to that in [1] is employed to manage the supply $(V_{DD25,\rm MIX})$ of the SL-HRM. When the gate-bias voltage of M_{1-2} is ready, and with the presence of $V_{{\rm LO}p,n}$, $V_{\rm start}$ enables the generation of $V_{DD25,\rm MIX}$ via kicking up an amplifier (M_{T1} and R_1). After buffering by two inverters, M_{T2} will allow a ramp up of $V_{DD25,\rm MIX}$. The capacitors (C_{1-2}) can set the ramp-up/-down time during the transient, and are served as the supply decoupling in the steady state.

It is also possible that, during the power down, V_{DD12} is removed before V_{DD25}, exposing $M_1 - M_6$ to $V_{DD25,\rm MIX}$. To address it, a compact node-voltage protection circuit (M_{T4-5} and M_{7-10}) is added to the mixer core. M_{7-10} sense the present of V_{DD12}, which indicates the bias of M_{1-2} and the presence of $V_{{\rm LO}p,n}$. If they are not ready, M_{7-10} will turn M_{T4-5} (thick-oxide) into the on state, shrinking current from $V_{{\rm out}p,n}$ to limit its dc level. In the nominal condition, such a circuit is disabled automatically since $V_{{\rm out}p,n}$ is settled at $\sim$1 V, whereas the gate voltage of M_{T4-5} is pushed to 1.2 V.

The effect of LO on the reliability needs to be considered as well. For a single-balanced mixer, the LO signal can appear at the output, which may exceed the allowable dc level and has the risk of overstress. However, for a double-balanced active mixer, the differential LO ensures there is no zero-current condition. Transient simulations can be used to track the terminal voltages

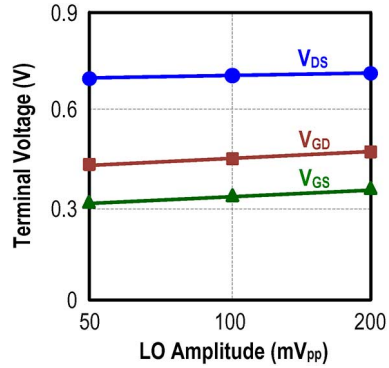

Fig. 7. Transient simulations of the terminal voltages with respect to the LO amplitude.

TABLE II
MAJOR DEVICE VALUES OF THE SL-HRM

Device	Size
$M_{1\text{-}2}$	20 µm / 0.06 µm
$M_{3\text{-}6}$	600 µm / 0.4 µm
R_L	2 kΩ
C_L	1 pF

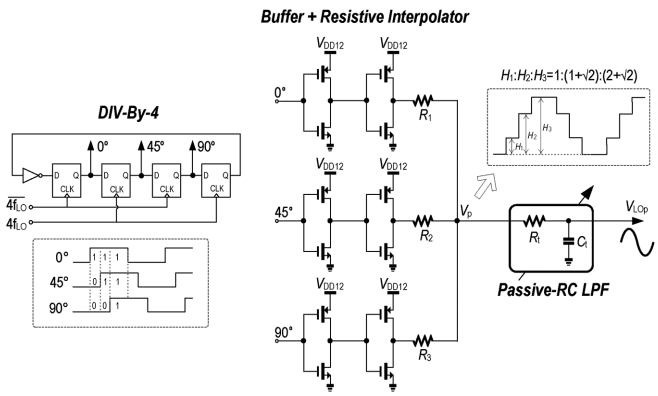

Fig. 8. Proposed square-to-sine LO generator.

of the mixing quad with respect to the LO amplitude, as plotted in Fig. 7. All terminal voltages are stable and are below 0.75 V. After all, it is safe to operate a voltage-boosted SL-HRM. The employed device sizes are presence in Table II.

B. A Digital-Intensive Square-to-Sine LO Generator

The proposed square-to-sine LO generator (Fig. 8) includes three parts, which are: 1) a div-by-4 synthesizes a set of polyphase square-wave LOs; 2) a resistive interpolator transforms such LOs into a pseudo-sine-LO; and 3) a passive-R_tC_t LPF furthers the purity of the sine-LO. Note that part of C_t is counted as the input gate capacitance of the mixing quad, saving the die area. The div-by-4 circuit can be directly driven by the VCO or a frequency divider. The LO generator operates at a 1.2-V supply (V_{DD12}) to save the dynamic power.

Passive interpolation [15] is power and area efficient, and can be well-matched in layout via upsizing the physical dimension of the resistors (e.g., poly-silicon). Here, a three-path resistive interpolation scheme is added after the inverter-based buffers. Similar to the typical $RC - CR$ polyphase filter [16] for I/Q

generation, the resistors in the LO path add minor phase noise as they drive only a capacitive load. The weighting ratio of $R_1 : R_2 : R_3$ is $\sqrt{2} : 1 : \sqrt{2}$. When the div-by-4 outputs a level of {1, 0, 0} for the phases {0°, 45°, 90°}, after combining through the resistors at V_p, the amplitude at V_p becomes $H_1 = V_{DD12}/(2+\sqrt{2})$. Likewise, for the divider output level {1, 1, 0} and {1, 1, 1}, the corresponding amplitudes at V_p are derived as $H_2 = V_{DD12}(1+\sqrt{2})/(2+\sqrt{2})$ and $H_3 = V_{DD12}$, respectively. The equivalent output is a pseudo-sine-LO suppressing the critical third and fifth harmonics. Other higher order harmonics are easily handled by the LPF, which offers a tunable bandwidth, and a first- to third-order attenuation mode to fit a wide range of RF and LO amplitudes. Unlike the existing HRMs that an LPF can only be put in front of the HRM in the signal path, the LPF here is more affordable in the LO path, leveraging the noise and linearity tradeoff.

It is worth discussing the performance of such an LO generator. If only a square-wave LO is passed through the LPF, the rejection of the third and fifth harmonics will be less effective, as expected. For instance, to generate a 200-MHz sine-LO, transient simulations were conducted under the following three cases: a) a square-wave LO directly filtered by an LPF; b) only the pseudo-sine-LO; and c) a pseudo-sine-LO filtered by an LPF. The results are shown in Fig. 9(a). The vertical axis is the normalized LO harmonic rejection $(A_{\rm LO}/A_{{\rm LO}n})$, where the amplitude of the nth LO harmonic is denoted as $A_{{\rm LO}n}$. Clearly, the rejection of the third is only 20 dB in Case a. For Case b, the rejection of the 7th LO harmonic is limited to 17 dB. Thus, it is essential to combine a pseudo-sine-LO with an LPF as in Case c, offering an over 40-dB rejection of all harmonics.

Considering the amplitude and purity of the sine-LO to the HRR of the SL-HSM, the HRR_n can be rewritten as

$$\mathrm{HRR}_n \approx \frac{H_1}{H_n + H_{{\rm LO}n}} \tag{14}$$

and

$$H_{{\rm LO}n} = \frac{a_{1,1}}{2} A_{{\rm LO}n} A_{\rm RF} \tag{15}$$

where $H_{{\rm LO}n}$ stands for the effect of LO harmonic on the ultimate HRR performance of the SL-HRM. Fig. 9(b) and (c) presents the simulated HRR_3 and HRR_5 versus $A_{\rm LO}/A_{{\rm LO}n}$ at 200 MHz, with an LO amplitude ranges from 50, 100, and 200 mV_{pp}. It shows that when $A_{\rm LO}/A_{{\rm LO}n}$ is high, HRR_3 and HRR_5 get better and rise to a limit governed by the HRM itself (i.e., closer to HS mixing). When $A_{\rm LO}/A_{{\rm LO}n}$ is low, HRR_3 and HRR_5 get worse and are limited by the purity of the LO. The simulated HRR_5 at LO amplitudes of 50 and 100 mV_{pp} are almost equal due to the dominance of LO harmonics, and the negligible effect of the SL-HRM itself, as predicted from (13) and (14). The results also show that a small LO favors the HRR more, as it can keep the SL-HRM under deep SL mixing.

V. Experimental Results

An SL-HRM prototype suitable for UHF-/VHF-band TV tuners or IEEE 802.22 CR was fabricated in a 65-nm CMOS process. The die micrograph is shown in Fig. 10. The active area is 0.042 mm^2 (LO generator: 140 × 190 $\mu\mathrm{m}^2$, startup circuit: 70 × 85 $\mu\mathrm{m}^2$, and mixer: 70 × 140 $\mu\mathrm{m}^2$). The mixer

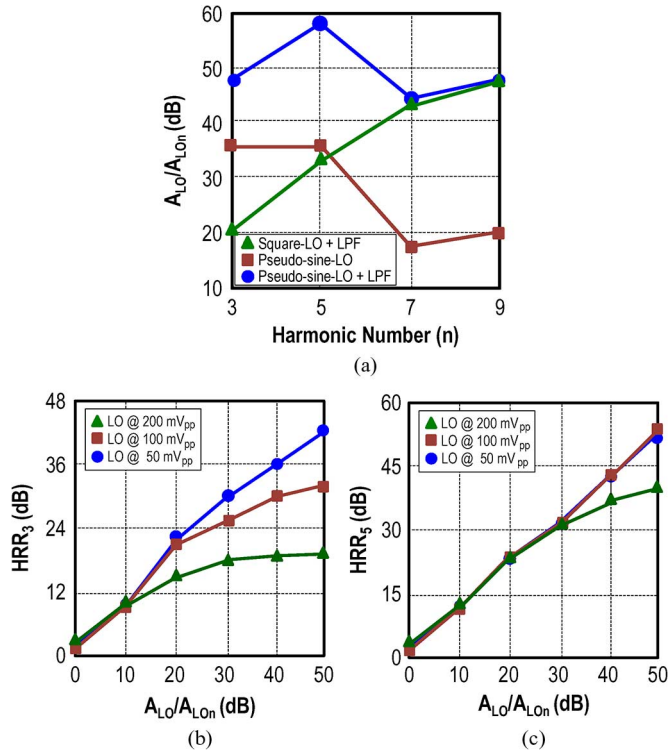

Fig. 9. Simulated: (a) normalized LO harmonic rejection $(A_{\rm LO}/A_{{\rm LO}n})$ versus the harmonic number under three different ways of sine-LO synthesis. (b) HRR_3 versus $A_{\rm LO}/A_{{\rm LO}n}$. (c) HRR_5 versus $A_{\rm LO}/A_{{\rm LO}n}$.

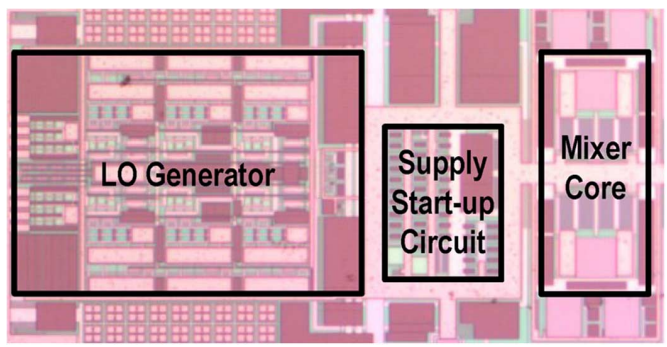

Fig. 10. Die micrograph.

consumes 7.5 mW at 2.5 V, and the LO generator dissipates 3–6 mW at 1.2 V. Due to the 2.5-V supply, a 6-dB higher gain is achieved when compared with a typical 1.2-V design, being more comparable with HS mixing. The supply startup and node-voltage protection circuits draw no static power in nominal operation. Their effectiveness was assessed through long-hour running of the chip and power-up/-down it many times under different supply sequences. No visible performance degradation or change of bias current was noted.

A. Key Performances of the SL-HRM Versus Input Frequency

The SL-HRM and LO generator were optimized to cover the 100–500-MHz range. The wideband results of conversion gain, NF, $P-1$ dB, IIP3, HRR_3, and HRR_5 were measured as shown in Fig. 11(a)–(e). Under each LO amplitude from 50 to 200 mV_{pp}, most data are wideband consistent. The HRR_3 and HRR_5 at small LO are higher in the low-frequency range

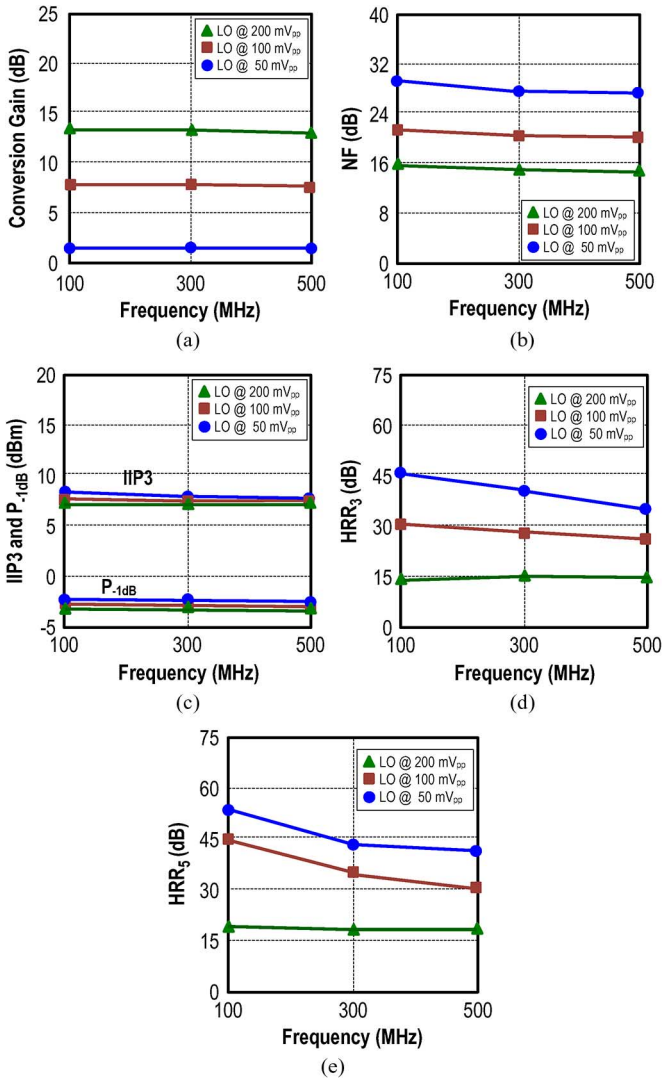

Fig. 11. Measured wideband results. (a) Conversion gain. (b) NF. (c) IIP3 and $P_{-1\,\mathrm{dB}}$. (d) HRR_3. (e) HRR_5. The results are obtained at a 4-MHz IF.

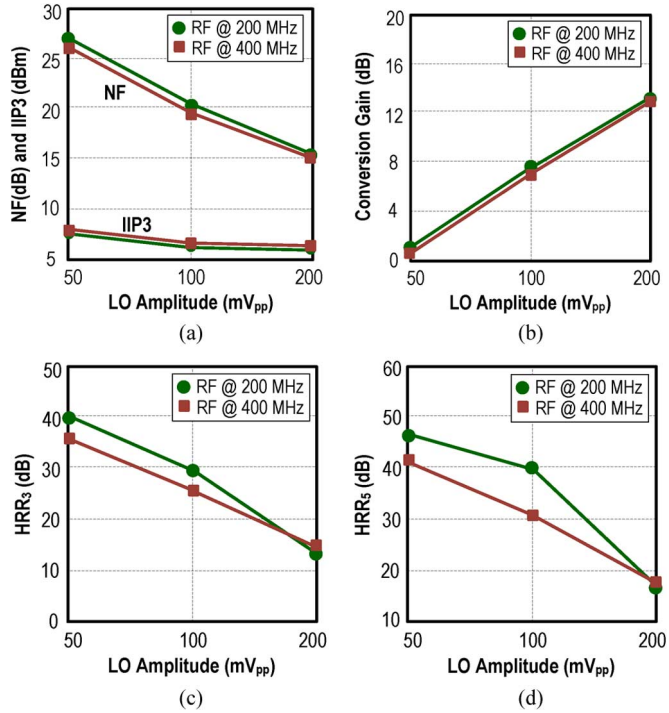

Fig. 12. Measured key results under different LO amplitudes. (a) NF and IIP3. (b) Conversion gain. (c) HRR_3. (d) HRR_5. The results were obtained at 200- and 400-MHz RF.

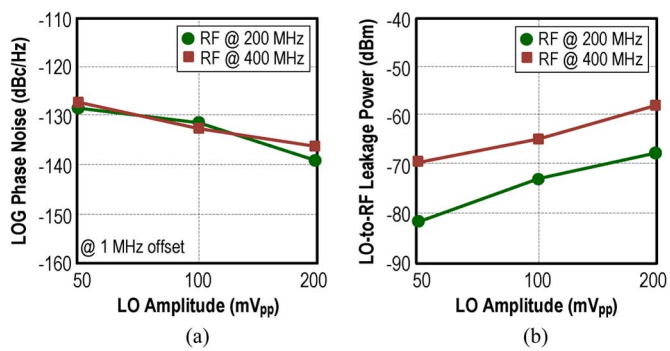

Fig. 13. Measured: (a) LO generator added phase noise and (b) LO-to-RF leakage power versus the LO amplitude. The results are obtained at RF of 200 and 400 MHz.

(<300 MHz) due to more filtering provided by the passive-RC LPF (i.e., higher purity of the LO).

B. Key Performances of the SL-HRM Versus LO Amplitude

The measured double-sideband (DSB) NF ranges from 15 dB ($\mathrm{LO} = 200\ \mathrm{mV}_{pp}$) to 27 dB ($\mathrm{LO} = 50\ \mathrm{mV}_{pp}$), as shown in Fig. 12(a). The IIP3 is obtained under a two-tone test at $f_{\mathrm{LO}} +$ 6 MHz and $f_{\mathrm{LO}} + 10$ MHz. By measuring the third-order intermodulation (IM3) term product downconverted to the 2-MHz IF, an IIP3 of from $+6.5$ to $+7.6$ dBm is stably achieved. The conversion gain [see Fig. 12(b)] increases from 1 to 13 dB with respect to the LO amplitudes from 50 to 200 mV_{pp}. This property offers a simple way to realize gain control.

The HRR_3 and HRR_5 were tested by inputting a signal of -20 dBm at $3f_{\mathrm{LO}} + 4$ MHz and $5f_{\mathrm{LO}} + 4$ MHz, respectively. The output baseband signal at 4 MHz was captured as the component downconverted by the corresponding LO harmonics. As shown in Fig. 12(c), with an LO amplitude of 50, 100, and 200 mV_{pp}, the achieved tunable HRR_3 is 13–40 dB at 200 MHz, and 15–37 dB at 400 MHz. For the HRR_5 shown in Fig. 12(d), it can be scalable from 17 to 45 dB at 200 MHz, and from 18 to 41 dB at 400 MHz. The higher order harmonic rejection over 200 MHz is also measured for the same range of LO amplitude, showing that the tunable HRR_7, HRR_9, and HRR_{11} are 24–35 dB, 30–39 dB, and 37–50 dB, respectively.

For an overall HRR of >60 dB in a receiver, the SL-HRM can be further incorporated with other filtering techniques, such as the harmonic-rejection LNA in [17] that offers over >20-dB HRR, or the tunable LC filter [18] that gives 26–36-dB HRR. Both are power-efficient solutions.

C. LO Phase Noise and LO-to-RF Leakage

Fig. 13(a) shows the measured LO phase noise added by the LO generator at 200 and 400 MHz. The LO source is from a high-quality signal generator. At a 1-MHz offset, the result

TABLE III
PERFORMANCE SUMMARY AND BENCHMARK WITH THE STATE-OF-THE-ART HRMS

	MWCL'09 [5]	JSSC'10 [19]	ISSCC'11 [9]	TCAS-I'13 [10]	RFIC'13 [20]	This Work
CMOS Process	90 nm	65 nm	110 nm	0.18 μm	45nm SOI	65 nm
RF Range (MHz)	48 to 860	200 to 900	100 to 300	48 to 862	500 to 1500	100 to 500
Die Area (mm^2)	N/A	0.4	0.12 [a]	0.05 [a]	0.352	0.042
Mixer Core Current (mA) @ V_{DD}	14.5 @ 1.2 V	14.5 @ 1.2 V	11 @ 2.7 V	3 @ 1.8 V	17 @ 1V	3 @ 2.5 V
LO gen. Current (mA) @ V_{DD} and RF	N/A	12.5 @ 1.2 V, 200 MHz RF 15.3 @ 1.2 V, 900 MHz RF	8 @ 1.3 V, 100 MHz RF	N/A	N/A	2.5 @ 1.2 V, 100 MHz RF 5 @ 1.2 V, 500 MHz RF
Gain (dB)	1 to 3	-0.5 to 2.5	15	4.5	8	1 to 13 [c]
NF (dB)	13.5	18 to 20	11	15.7	35	15 to 27 [c]
IIP3 (dBm)	10 to 13	10	12	8.2	-3	6.5 to 7.6
HRR_3/ HRR_5 (dB)	37 / -- @ <300 MHz RF	>25 / 25 @ <900 MHz RF	52 / 54 @ 200 MHz RF	38 / 34.5 @ <300 MHz RF	55 / 58 @ <1.5 GHz RF	13 to 40 [c] @ 200 MHz RF 17 to 45 [c] @ 200 MHz RF
HRR_7/ HRR_9 (dB)	No / No	No / No	55 [b] / -- @ 150 MHz RF	No / No	No / No	24 to 35 [c] @ 200 MHz RF 30 to 39 [c] @ 200 MHz RF

[a]: Estimated from figure [b]: At LO phase number $N = 12$ [c]: Tunable with LO amplitude

ranges from -137 to -127 dBc/Hz under an LO amplitude of 50–200 mV_{pp}, which should be better than that of a typical LC VCO, leading to an LO generator that would not be the phase-noise bottleneck.

The LO-to-RF leakage can result in a time-varying dc-offset at the IF port. As shown in Fig. 13(b), the measured leakage power is < -58 dBm, with a span of 12 dB consistent with the used LO range. The LO leakage at 400 MHz is $\sim$10 dB higher than that at 200 MHz, due to more pronounced parasitic coupling. In any case, the low LO leakage is another valuable property of SL mixing against its HS counterpart.

D. Performance Summary and Benchmark

The performance summary is given in Table III. Compared with the prior art [5], [9], [10], [19], [20], this work has the major benefits of: 1) small chip area and power; 2) rejection of ALL harmonics without complicated circuitry; and 3) tunable HRR via adjusting the LO amplitude.

VI. POTENTIAL APPLICATIONS

As demonstrated, a sine-LO SL-HRM offers a tunable HRR, which can be used to adapt the receiver performances under different air environments. In fact, the spectrum condition is not always pessimistic requesting for the best sensitivity. The sought channel can possess a reasonably high signal-to-noise ratio (SNR), as shown in the power spectrum density (PSD) plot in Fig. 14(a). Consequently, the gain and NF of the receiver become less demanding, allowing the use of a smaller sine-LO to improve the blocker tolerability, as shown in Fig. 14(b).

We use the transient simulation (Fig. 15) to show a potential adaptive operation scenario: when there is no blocker (first time zone), a large sine-LO ($A_{\rm LO} = 200$ mV_{pp}) is used to optimize the sensitivity. However, when there is a -20-dBm blocker located at the third harmonic of the LO, the wanted signal will be jammed (second time zone). To alleviate it, $A_{\rm LO}$ can be downsized to 100 mV_{pp} to recover the signal (third time zone).

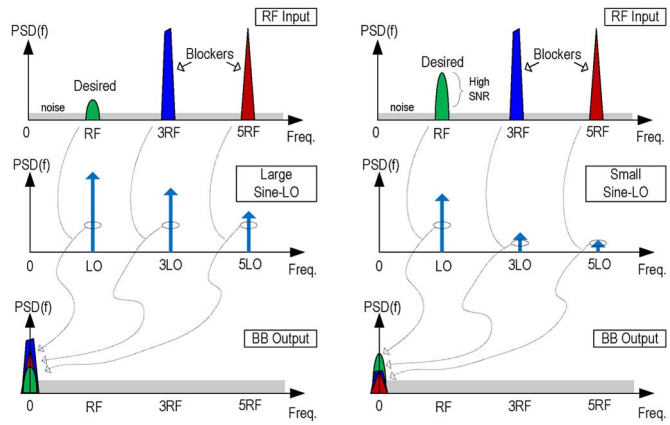

Fig. 14. RF-to-baseband (BB) downconversion. (a) Large sine-LO improves sensitivity, but suffering from strong harmonic mixing. (b) Small sine-LO, alternatively, significantly rejects the LO harmonics. It is especially relevant when the SNR of the desired signal is reasonably high.

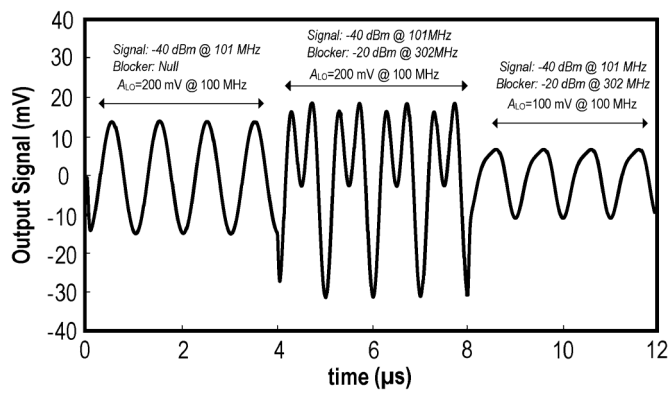

Fig. 15. Transient simulations showing the control of LO amplitude to avoid harmonic mixing when there is a blocker located at the third harmonic of the LO.

VII. Conclusions

A novel sine-LO SL-HRM has been proposed, analyzed, and experimentally verified. It enables a tunable HRR against the LO amplitude, and the rejection of all unwanted LO harmonics without complicated circuitry. The performances under SL mixing including the gain, NF, IIP3, and HRR have been analyzed with respect to the amplitude and purity of the sine-LO. The implementation is based on a voltage-boosted SL-HRM with a supply startup circuit and a node-voltage protection circuit to optimize the performances, while ensuring the device reliability. A digital-intensive square-to-sine LO generator followed by an LPF ensures a high-purity sine-LO. The fabricated VHF-/UHF-band SL-HRM measures a wide range of tunable gain, NF, and HRR versus the LO amplitude. The LO leakage is low and the IIP3 is stable as expected. The achieved power and area efficiencies are also attractive when compared with prior art.

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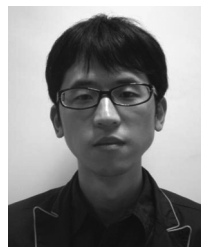

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