A High-Voltage-Enabled Class-D Polar PA Using Interactive AM-AM Modulation, Dynamic Matching, and Power-Gating for Average PAE Enhancement

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***Abstract*— This paper describes a 2.4-GHz digitally-modulated class-D polar power amplifier (PA) with novel circuit techniques to enhance the average power-added efficiency (PAE_{ave}) that becomes increasingly crucial to prolong the battery lifetime. The PA features 5+5-b interactive AM-AM modulation between the class-D unit amplifiers and a novel high resolution dynamic matching network (DMN) to improve the back-off PAE. A novel power-gating technique tailored for class-D PAs is also proposed and embedded into each unit amplifier and its driver (tapped inverter chain), alleviating leakage-current suppression, area reduction of the DMN, and direct-powering by a standard 1.5-V AA battery. An high back-off power efficiency is made possible by introducing a multi-bit capacitively-tuned DMN, which adds low loss while improving the PAE of the unit amplifiers using the load-pull optimization. The DMN also can correct the antenna impedance mismatch for better average P_{out} ($P_{out,ave}$) and PAE_{ave} under a practical VSWR (2.5 : 1), and aids to reconfigure the PA between the P_{out} -optimized and the PAE-optimized modes. For a 20-MHz 64-QAM OFDM output at a typical EVM (< −25 dB), the 65-nm CMOS PA exhibits 40.7% PAE_{ave} at a 16.3-dBm P_{out}. The mode switching is demonstrated as a prospective function for battery lifetime extension.**

***Index Terms*— AA Battery, antenna impedance mismatch, class-D, CMOS, digital AM modulation, dynamic matching network (DMN), error-vector magnitude (EVM), inverter chain, leakage current, matching network (MN), polar, power amplifier (PA), power-added efficiency (PAE), power gating.**

I. Introduction

INSIDE the landscape of Internet of Things, Wi-Fi Direct [1] is an emerging data-exchange paradigm for electronic gadgets to be freely connected without a fixed access point.

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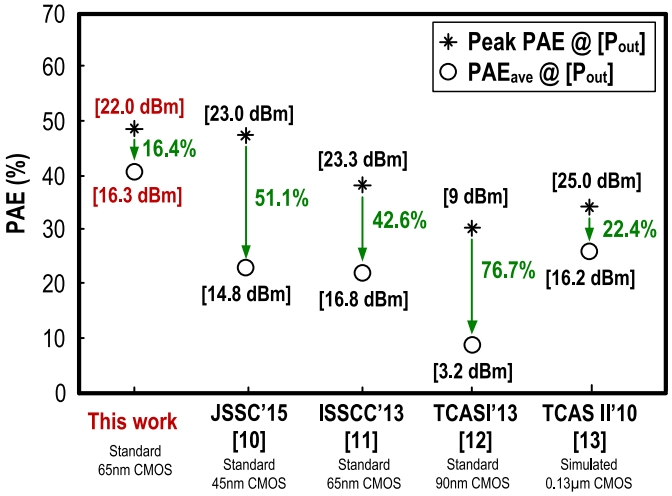


Fig. 1. Benchmark of this work with the state-of-the-art 2.4-GHz CMOS PAs for 802.11g. This work features a number of circuit techniques to improve the back-off PAE, closing the gap between peak PAE and PAE_{ave}.

This forethought is prospective for the controller side (e.g., smartphones), but broadening it to massively manufacturing products (e.g., lightings and computer mouses) will demand even lower cost and longer battery lifetime wireless radios, especially for those that rely on off-the-shelf AA batteries [2]. Moreover, the static power of those radios must be minimized as they are mostly in the off state while the battery remains connected.

For wireless transmitters, a digitally-modulated polar power amplifier (PA) [3], [4] offers the opportunity to use an array of switchable unit amplifiers to improve the power efficiency while lowering the static power. It can effectively combine the amplitude-modulated (AM) and phase-modulated (PM) components as a non-constant envelop RF output, circum- venting the high-performance supply modulator essential in analog-type polar PAs such as Envelope Elimination and Restoration [5]. Although the state-of-the-art CMOS PAs (Fig. 1) [6]–[13] have achieved a high *peak PAE* up to 45% under continuous-wave (CW) measurements, their *average PAE* (PAE_{ave}) is practically <28% when transmitting a complex modulated signal (e.g., 64-QAM OFDM), which has a high peak-to-average power ratio (PAPR) in the time domain. Thus, improving the PA operation during the power back-off

becomes crucial to narrow down the gap between the peak PAE and PAE_{ave} (Fig. 1).

Digital polar PAs exploit the envelope code to activate the unit amplifiers, rendering the power back-off inherently effective by switching-off the unused units. Yet, maximizing PAE_{ave} requires attention to the power efficiency of each unit amplifier in both on and off states. The class-D amplifier is a promising topology for implementation in ultra-downscaled CMOS technologies, owing to its low dynamic loss in active mode and almost no static power (only leakages) [6], [10]. Nevertheless, fine-linewidth CMOS devices have low breakdown voltages exacerbating the loss and increasing the area of the output matching network (MN), i.e., a higher MN transform ratio (n) is entailed to boost the output power (P_{out}) when the supply voltage (V_{DD}) is low, yielding more MN loss.

Although power back-off can aid to accommodate high PAPR signals, the V-I cross area enlarges given that the load impedance can only be optimized at the highest P_{out}. To surmount this constraint, dynamic load modulation (DLM) has been proposed in the discrete forms [14] and found useful in recent integrated works: *Outphasing* [8], [9], *Doherty* [15], *Tunable Transformer* [11], and *Switched Capacitor* [6], [7]. Regrettably, their shortcomings are of concern: *Outphasing* involves a power combiner and suffers from diverging imaginary impedance; both limit the benefit of DLM to the PAE during the power back-off. *Doherty* requires quarter wavelength phase shifters implemented in input and output MNs, impacting both the power and area efficiencies. *Tunable Transformer* has very limited DLM steps due to ineffectual switching. *Switched-Capacitor* has more DLM steps, but only can offer a sub-optimal impedance trace and relatively low P_{out} due to the off-state voltage stress.

This paper describes a digitally-modulated class-D polar PA with circuit techniques to enhance PAE_{ave}. Unlike the existing DLM mechanisms, a *multi-bit dynamic* MN (DMN) is proposed, which tracks the maximum-PAE load impedance for each amplitude control word between the peak power and 5-dB back-off point. The key principles are a novel load-pull-based design method and a PAE optimization algorithm. This refined dynamic approach substantially moderates the loss of the MN during the power back-off. Each unit amplifier is driven by a tapped inverter chain for PM, and switched by a digital amplitude code for AM. Differing from the power-gating technique [16] commonly found in digital chips, our power- gating technique is tailored for class-D PAs to suppress the leakage currents without explicit power switches, reducing the area of the MN and allowing direct-powering by a 1.5-V AA battery (i.e., no extra power management unit). The fabricated 65-nm CMOS 2.4-GHz PA prototype achieves a high PAE_{ave} of 40.7% favorably comparable with the recent art (Fig. 1). Also, the multi-bit DMN offers two interesting properties: 1) antenna impedance correction, and 2) mode selection by introducing a P_{out}-/PAE-tradable calibration scheme. The former improves the average P_{out} ($P_{out,ave}$) and PAE_{ave} under a practical VSWR, whereas the latter constitutes a new variety for battery lifetime extension.

Section II introduces the background of PAE_{ave} under a 64-QAM OFDM signal. Section III details the PA architecture and circuits design. Section IV describes and elaborates the effectiveness of the proposed multi-bit DMN, and Section V summarizes the experimental results.

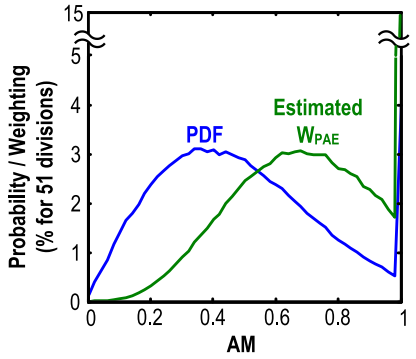


Fig. 2. PDF and estimated weighting (W_{PAE}) for 802.11g signals after clipping.

II. PAE_{ave} Under a 64-QAM OFDM Signal

For simplicity, only the 64-QAM OFDM signal is employed to study the relationship between the back-off PAE (PAE_{BO}) and the overall PAE_{ave} of a PA,

$$PAE_{ave} = \int PAE_{BO}(AM) \times W_{PAE}(AM)\, dAM \quad (1)$$

where W_{PAE} is the weighting of PAE_{BO} at each AM level, reflecting the impact of PAE at each AM level (V_{AM}) to the overall PAE_{ave}. PAE_{ave} can also be re-expressed with P_{out} and the DC power consumption (P_{DC}),

$$PAE_{ave} = \frac{\int Pout(t)\, dt}{\int P_{DC}(t)\, dt}. \quad (2)$$

where $P_{DC}(t)$ is the instantaneous DC power consumption in the time domain.

The integration period is assumed to be adequately long to reflect the actual probability density function (PDF) of the modulation. By assuming the PA as a time-invariant system (i.e., no temperature drift), and AM is the only independent variable, (2) can be mapped into the AM domain as,

$$PAE_{ave} = \frac{\int P_{out}(V_{AM}) \times PDF(V_{AM})\, dV_{AM}}{\int P_{DC}(V_{AM}) \times PDF(V_{AM}) dV_{AM}} \quad (3)$$

where V_{AM} is the RMS amplitude of the RF signal, and it is proportional to the AM level by assuming perfect linearity in the amplifier.

Hence, the definition of PAE at a certain AM level is defined as,

$$PAE_{BO}(V_{AM}) = \frac{P_{out}(V_{AM})}{P_{DC}(V_{AM})}. \quad (4)$$

Moreover, V_{AM} also has a direct relationship with P_{out} related to the load impedance (R_L),

$$P_{out}(V_{AM}) = \frac{V_{AM}^2}{R_L}. \quad (5)$$

By substituting (4) and (5) into (3), we have,

$$PAE_{ave} = \frac{\int V_{AM}^2 \times PDF(V_{AM})\, dV_{AM}}{\int \frac{V_{AM}^2}{PAE_{BO}(V_{AM})} \times PDF(V_{AM}) dV_{AM}}. \quad (6)$$

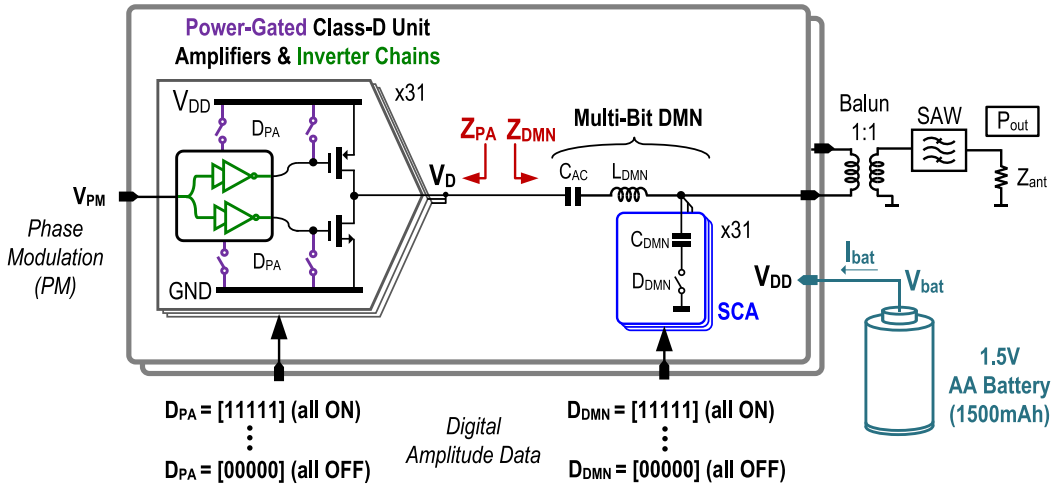


Fig. 3. Proposed class-D polar PA. It features 5+5-bit interactive AM-AM between the class-D unit amplifiers and multi-bit DMN to allow PAE_{ave} or P_{out} optimization using the load-pull optimization. Direct 1.5-V AA-battery powering and low leakage currents are achieved by embedding power-gating techniques.

(6) describes how PAE_{BO} contributes to PAE_{ave}. In addition to PDF dependency, PAE_{ave} has a weighting of V_{AM}^2. Thus, the highest weighting of W_{PAE} should be located at the *higher AM region* for the best possible PAE_{ave}, instead of the highest PDF density region. To estimate W_{PAE}, the PAE impulse functions at each V_{AM} are substituted into (6) and plotted in Fig. 2. The impulse function has a PAE of 100% ideally at the V_{AM} level, and a PAE of 10% at the other V_{AM} levels. Note that clipping is applied to maximize the P_{out} and PAE. The targeted EVM is set at -26 dB for clipping with a corresponding PAPR of 5.2 dB similar to [9]. Observing Fig. 2, the value of PAE below the 6-dB back-off point has a relatively low impact to the final PAE_{ave}, while the peak PAE contributes strongly to the final PAE_{ave}. In fact, the PAE between the peak and 6-dB back-off point is still critical but was not specifically explored in prior works for OFDM 64-QAM modulation. This insight inspires our work here and outlines the inadequacy of the existing DLMs [11] (i.e., a single-bit switching to the 6-dB back-off point does not optimally contribute to the PAE_{ave}).

III. Circuit Implementation

A. PA Architecture

The proposed polar PA (Fig. 3) is differential and comprises 31 equal-weighted class-D unit amplifiers and inverter chains activated by a 5-bit control word (D_{PA}). Another 5-bit control word (D_{DMN}) is introduced to tune the capacitance C_{DMN} in the DMN. D_{PA} and D_{DMN} work interactively for AM. Although 6-bit AM resolution is sufficient for an 802.11g signal [6] to have a satisfactorily low close-in noise floor, we propose 5+5-bit AM-AM modulation that offers extra freedom to optimize PAE_{ave} (details in Section IV). From simulations, the in-band quantization noise of the proposed AM modulation scheme is < -50 dBr for the 802.11g signal, which is 10 dB lower than the specified (-40 dBr) from the spectral mask.

The PM signal (V_{PM}) is buffered by an inverter chain such that each class-D unit amplifier can be driven by a pulse-shape PM signal to maximize P_{out}. In order to reduce the switching loss, when the corresponding D_{PA} is in the off state, both the inverter chain and unit amplifier are deactivated with power gating to lower their leakage power.

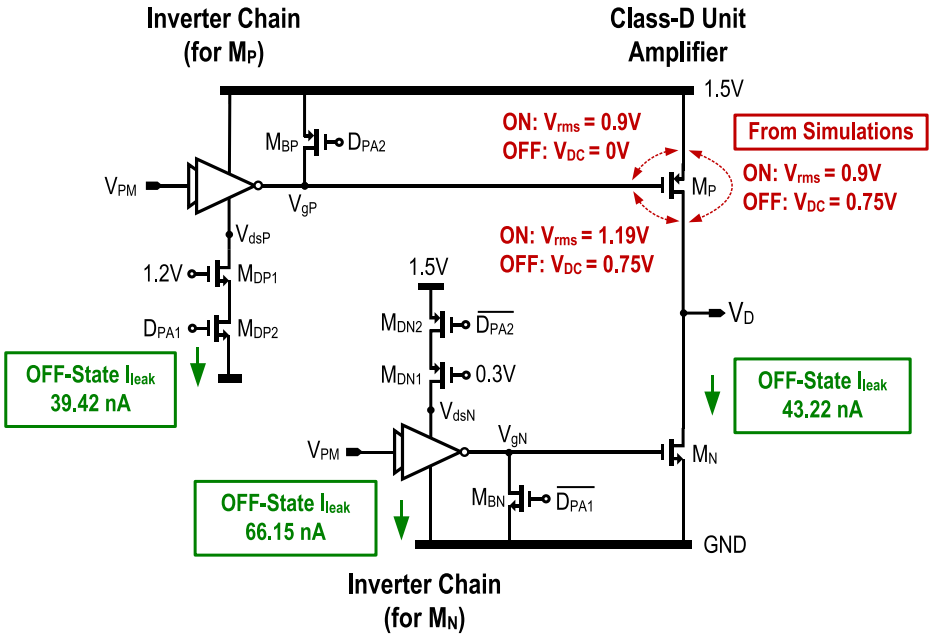
The MN is an L-type LC network with a capacitor C_{AC} to block the DC current. The involved switched-capacitor array (SCA) is implemented to tune C_{DMN}, which can be switched to the ground terminal, resulting in low power loss.

The unit amplifiers and inverter chains are based on standard 1.2-V CMOS devices but are high-voltage-enabled to 1.5 V, such that an AA battery can be directly adopted, avoiding any power-management units that otherwise penalize the PAE and induce extra cost. Such a voltage-headroom enlargement allows size and loss reduction of the MN for the same P_{out} with a single LC resonator [17].

In overall, the power efficiency of the PA can be estimated,

$$PAE_{PA} = \frac{P_{out}}{P_{out}/\eta_{PA} + P_{leak} + P_{INV}} \times \eta_{MN} \tag{7}$$

where PAE_{PA} refers to the general PAE at all output levels; η_{MN} is the MN power efficiency; η_{PA} is the power efficiency of the standalone class-D PA mainly attributed to the switching loss; P_{leak} is the leakage power of the inverter chains and unit amplifiers in off state, and finally P_{INV} is the power consumed by the inverter chains. (7) can be read by firstly ignoring the MN power loss. P_{out} is divided by η_{MN} since P_{out} refers to the final P_{out} after the MN, and P_{out} before the MN should be larger to account for the MN insertion loss. The same reason holds for the switching loss of the unit amplifiers. P_{leak} and P_{INV} are also divided by the same ratio since the device sizes of the unit amplifiers and inverter chains have to be proportionally enlarged for the same output power. Thus, the MN power efficiency dominates the final PAE_{PA}. Also, because P_{INV} and P_{leak} will also be affected by the MN power efficiency (η_{MN}), the MN is more effective than zero-voltage-switching (ZVS) [12] that mainly reduces the PA switching loss (η_{PA}). P_{leak} does not affect the PAE_{ave} but the battery lifetime as the PA is mostly in off state or in standby mode.



	ON D_{PA1} = 1.2V, D_{PA2} = 1.5V	OFF D_{PA1} = 0V, D_{PA2} = 0.3V
V_{gP}	Switching	1.5V
V_{gN}	Switching	0V
V_{dsP}	0V	1.5V
V_{dsN}	1.5V	0V

	ON	OFF (Power Gating)
M_P	Switching	Open
M_N	Switching	Open
$M_{DP1,2}$	Close	Open
$M_{DN1,2}$	Close	Open

Fig. 4. Schematic of the class-D unit amplifier and its driver (inverter chain) that are 1.5-V-enabled. All terminal voltages (rms) are ensured <1.2 V. Power-gating reduces the off-state leakage currents.

B. Class-D Unit Amplifier and Inverter Chain With Power-Gating

Both the unit amplifier and inverter chain feature power-gating (Fig. 4). To enable 1.5-V operation, the RMS voltage for a frequency >60 MHz (i.e., RF signal) should be lower than the maximum rating [18]. For the typical inductor-loaded PAs, the instantaneous drain voltage would exceed the standard supply voltage for higher P_{out} and PAE at operation (e.g., inverse class-D PA [11] and class-E PA [12]).

Alternatively, during the off state, the gate-drain-source voltage trajectories must be evaluated to guarantee the device overdrives are not violating the reliability constraints given in the Process Design Rule Manual [19], [20]. The simulated RMS and DC voltages during the on and off states across each critical node are labeled in Fig. 4. The voltage stress is limited by V_{gd} during the on state of M_P and M_N. The off-state reliability is ensured by the inherent power gating of class-D, i.e., both M_P and M_N are switched off to share the voltage stress, via biasing the power transistors through M_{BP} and M_{BN}. The size of M_{BP} and M_{BN} is minimized to lower their added parasitic capacitances. The voltage stress on M_P and M_N is designed to be evenly distributed, so that each transistor is stressed by 0.75 V, reserving a safe voltage margin of 0.45 V from the 1.2-V voltage limit [21].

During the power-on transient, the switch-on timing of NMOS and PMOS has a 280 ps difference introduced by the single stage inverter delay in D_{PA2} and $\overline{D_{PA1}}$ as shown in Fig. 4. From simulations, while the D_{PA} changes from [00000] to [11111], a worst case of 10% peak voltage variation is observed during this short period. Yet, the instantaneous voltage is still within the absolute breakdown voltage, and its impact on overall RMS voltage is limited due to a very short period. Thus, a reliable power-on transition can be ensured.

The power-gating not only ensures the device reliability during the off state, but also significantly reduces the leakage current: when M_P and M_N are turned off, the off-resistance from supply to ground is doubled comparing to typical single-device power-gating. It is noteworthy that the power-gating of M_P and M_N is inherent, avoiding the need of extra switches between the supply rails that otherwise significantly degrade both the P_{out} and PAE.

For the inverter chain, the power-gating is implemented with the cascode devices (M_{DP1}, M_{DP2}, M_{DN1} and M_{DN2}). Since the drain nodes (V_{gP} and V_{gN}) have to be biased, the voltage stress cannot be evenly distributed between the NMOS and PMOS. From simulations, the PMOS (NMOS)-driving inverter chain has a leakage current of 39.42 nA (66.153 nA), and it is 43.22 nA for the class-D unit PA. Overall, the leakage current of the entire PA with 31 unit elements is 9.23 μA (i.e., 13.85 μW leakage power).

The power-gating also eases non-overlap pulse generation, and size reduction of the bias devices M_{BP} and M_{BN}. An overlap V_{PM} pulse is undesired for switching-mode PAs as it will

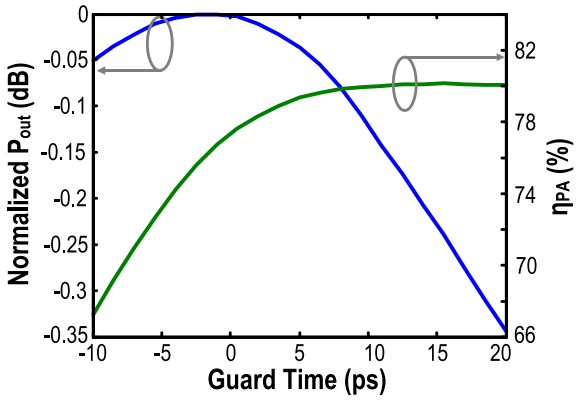


Fig. 5. Simulated normalized P_{out} of class-D unit amplifier and its drain efficiency (η_{PA}) over different guard times of the non-overlap pulses with 20-ps rise and fall times without DMN loss.

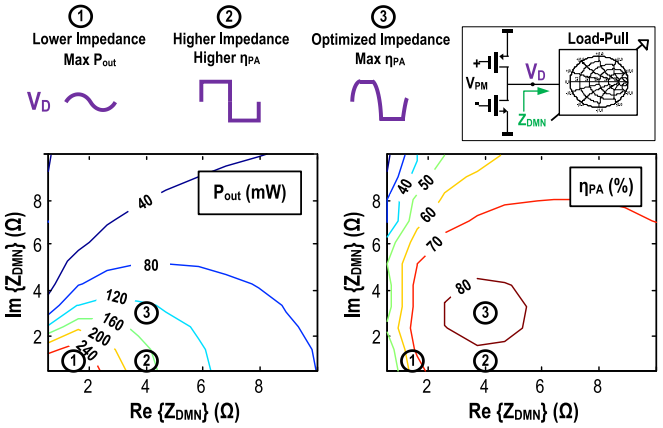


Fig. 6. Load-pull simulations using a simplified class-D PA in 65-nm CMOS, showing the waveform variations of V_D to the achievable P_{out} and η_{PA} without DMN loss.

cause a large crowbar current drawing from the supply to ground, degrading the power efficiency. Contradictorily, a non-overlap pulse will prolong the rise and fall times including the guard time at V_D, limiting the achievable P_{out} of each unit amplifier. The simulated η_{PA} and P_{out} penalties with respect to the non-overlap guard time are shown in Fig. 5, where the guard time refers to the pulse-width difference of V_{gP} and V_{gN}. Suggested by simulations, without the non-overlap pulse, η_{PA} will be degraded by 3%, but it will be negligibly small for a practical 10-ps guard time. Compared to the degradation of η_{PA} in the case of guard time variations, the P_{out} penalty is low. In our design, a non-overlap guard time of 15 ps was chosen to accommodate certain guard time variations while ensuring low P_{out} penalty of 0.23 dB. As mentioned before, M_{BP} and M_{BN} are minimally sized to prevent extra switching loss. In the off state, the power-gating switches significantly increase the impedance of the drain nodes (V_{gP} and V_{gN}), and hence the bias voltage can be effectively held with small M_{BP} and M_{BN}.

M_P and M_N are sized according to the required on-resistance (Z_{PA}) to generate the targeted P_{out} under limited V_{DD}. Without considering source impedance (Z_{PA}) variation as P_{out} changes, P_{out} is maximized when the impedance is conjugately matched. However, at lower load impedance (Z_{DMN}), as the swing at V_D decreases, M_P and M_N start to leave the triode region hence increasing Z_{PA} at lower Z_{DMN}. Therefore, a load-pull simulation is performed as shown in Fig. 6 to observe the maximum available P_{out} for each transistor size including the Z_{PA} variation effecting as Z_{DMN} changes. In this work, the combined sizes of M_N (W/L: 868/0.06 μm) and M_P (W/L: 1736/0.06 μm) ensure a low equivalent on-resistance of 1.6 Ω, delivering a maximum of 280 mW at a lower Z_{DMN} (excluding the DMN loss) in the simulation. In most cases, the Z_{DMN} will not be placed at the maximum P_{out} impedance, since η_{PA} is typically low due to lower voltage swing at V_D. In fact, higher impedance with a correct load angle can result in a better power efficiency as shown in Fig. 6. The proposed polar PA with a multi-bit DMN is able to tune the Z_{DMN} at lower impedance for maximum P_{out} while preserving high Z_{DMN} impedance for optimum η_{PA} details later.

The upscaling ratio within the inverter chain determines the rise and fall times of the driving pulses arrived at M_P and M_N. The pulse duration has to be short to reduce the dynamic power loss as discussed. Meanwhile, a driving pulse with a long rise and fall times will raise the on-resistance of the class-D unit amplifiers, degrading P_{out}. In this design, a 4-stage inverter chain of 1.4x to 1.5x ratio is designed to provide a 15.79 dB gain with 20-ps rise and fall times, leaving the class-D unit amplifier to secure just a 5.93-dB gain. From simulations, the overall PA offers a gain of ~21.7 dB (20.5 dB) excluding (including) the MN power loss. Each inverter chain consumes 1.3 mW of dynamic power. Totally, the 62 inverter chains (differential) consume ~81 mW, 20% of the total power budget. Such power consumption will downscale proportionally with D_{PA} during the power back-off.

IV. Multi-Bit DMN

A. Load-Pull of Class-D PA

Load-pull is common in MN design for load-impedance selection. A set of load-pull simulations using a simplified 65-nm CMOS class-D PA is plotted in Fig. 6 illustrating the tradeoff between P_{out} and η_{PA}. When Z_{DMN} is close to Z_{PA}^*, a higher P_{out} is achieved. However, at this load impedance, the drain voltage (V_D) is more sinusoidal with a voltage swing of only half V_{DD}. Thus, η_{PA} is relatively low due to a large V-I crossing area. On the other hand, when the load impedance goes higher, the voltage will be transformed to a square-wave benefiting η_{PA}. Moreover, with slightly inductive loading, the switching voltage gets low, improving η_{PA}. η_{PA} can be further improved by harmonic load-pull to achieve ZVS, but it requires a larger MN and is beyond the focus of this work. Here, η_{PA} can be as high as 82% in the inductive region, which is mainly limited by the drain parasitic capacitance. This simulation shows that a 30% improvement of η_{PA} is expected comparing to highest P_{out} impedance. Of course, during such a process, P_{out} drops by 37.5% (–2 dB). Unlike the typical load-pull impedance selection [22] that only uses one impedance value for the MN as the optimum condition,

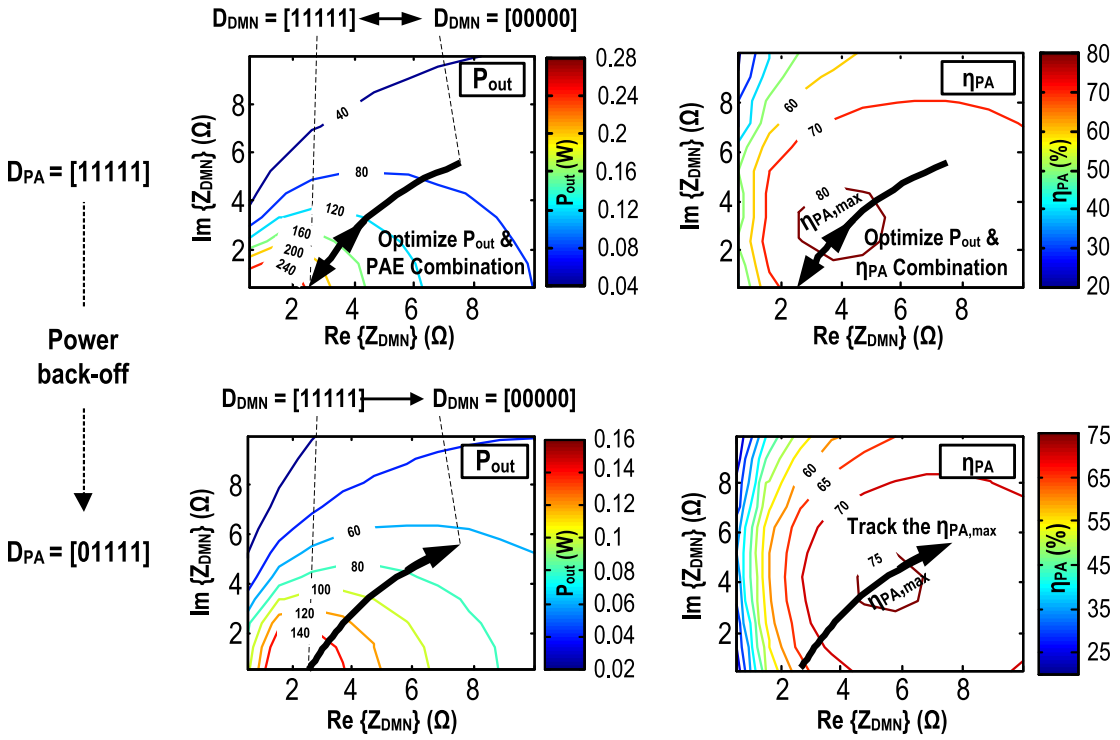


Fig. 7. Simulated 3-D load-pull of the polar PA under different D_{PA} during the power back-off without DMN loss.

the proposed multi-bit DMN allow trading of P_{out} and η_{PA} (details in Section V-B).

B. Load-Pull Optimization

To secure a high η_{PA}, not only at the maximum P_{out}, the load-pull is carried in simulation for each D_{PA} state. Two D_{PA} states (D_{PA} = [11111] and D_{PA} = [01111]) are plotted in Fig. 7 to illustrate the principle. Inside, the traceable track of the DMN is marked. At the highest D_{PA}, the multi-bit DMN is able to find suitable impedance for high P_{out} or η_{PA}. When D_{PA} gets lower (i.e., more unit amplifiers are switched off), a shift in the maximum P_{out} and η_{PA} impedance can be observed due to a higher Z_{PA}. If the DMN is untunable and Z_{DMN} was designed at maximum η_{PA} at peak P_{out}, η_{PA} is expected to drop from 82% to 65% when D_{PA} is backed-off from [11111] to [01111]. With the proposed multi-bit DMN, Z_{DMN} can be transformed into the highest η_{PA} impedance and maintains a η_{PA} of 76% when D_{PA} is backed-off. Thus, 17% improvement of η_{PA} is expected. The fall of peak η_{PA} is mainly caused by the rise of Z_{PA} and unchanged CMOS drain parasitic capacitance. From the full set of 3-D load-pull simulation results, the maximum η_{PA} can be tracked down to the 5.73-dB back-off point, where η_{PA} is improved from 55.85% to 67.68% when comparing with the static load that is fixed at the optimum peak power η_{PA}. Also, limited by the impedance trace trajectory of the LC-based DMN, Z_{DMN} trace does not pass through the impedance with the highest P_{out} to better track the maximum η_{PA}. At the highest D_{PA}, the simulated peak P_{out} on the Z_{DMN} trace is 240 mW (excluding the MN insertion loss).

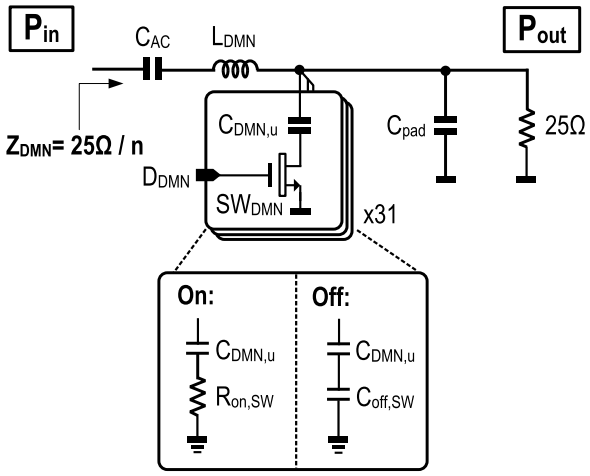


Fig. 8. Schematic of the multi-bit DMN. SW_{DMN} is a thick-oxide MOS for reliability.

The DMN can also be utilized to correct the antenna impedance mismatch.

C. Implementation

The DMN is modified from a simple LC network (Fig. 8). It features a 5-bit SCA to tune the impedance with adequate resolution and small loss. Unlike the typical SCA that is mainly used for frequency-band adjustment in PAs, the SCA here serves for dynamic impedance transformation under a fixed carrier frequency.

L_{DMN} is a single-turn spiral inductor with an inductance of 0.57 nH, and the equivalent series resistance (ESR_L) is

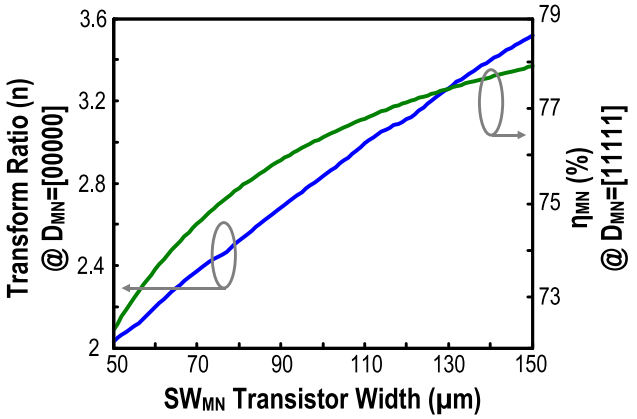


Fig. 9. Simulated minimum transform ratio (n) at D_{DMN} = [00000], and DMN power efficiency at D_{DMN} = [11111], with respect to the transistor width of SW_{DMN}.

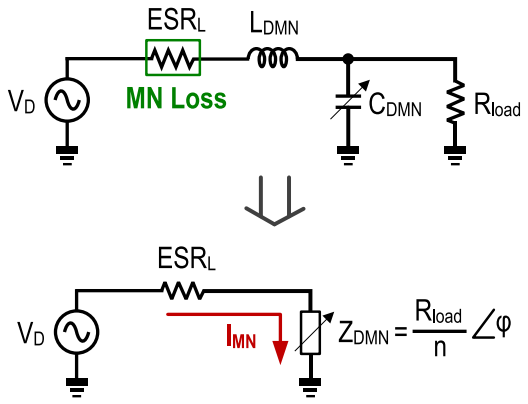


Fig. 10. Equivalent circuit model of the multi-bit DMN for η_{MN} analysis.

0.5 Ω. The SCA has a total on-capacitance of 9.47 pF, and C_{AC} is 28 pF to block the DC. The transformed load impedance is 2.5 Ω for an optimum load at peak P_{out}. The SCA features 31 equally divided capacitors ($C_{MN,u}$ = 0.3 pF) switched by the 5-bit D_{DMN} to cover a wide range of transform ratio (n). L_{DMN} and C_{DMN} together provide ~27-dB rejection at the 3rd harmonic, relaxing the requirement of the output SAW filter.

SW_{DMN} of each SCA unit is implemented with thick-gate NMOS to prevent device breakdown during the off-state. The size of SW_{DMN} determines the tradeoff between η_{MN} at higher n, and the amount of the off-state capacitance $C_{off,SW}$. Obviously, a large SW_{DMN} ensures a small on-resistance $R_{on,SW}$ and therefore lower loss from the MN (i.e., η_{MN}) during the on-state, but the induced parasitic capacitance $C_{off,SW}$ will be in series with $C_{DMN,u}$ during the off-state, limiting the SCA tuning range. To observe this tradeoff, we plot n at D_{DMN} = [00000] and η_{MN} at D_{DMN} = [11111] with respect to the size of SW_{DMN} in Fig. 9. Note that η_{MN} is obtained with contributions from $R_{on,SW}$ and ESR_L. The width of SW_{DMN} is sized as 85 μm for an on-state η_{MN} of 75.68%, and the total off-state capacitance is 3.15 pF, which sets the practical range of n from 11.42 down to 2.6. Comparing with the typical fixed MN (i.e., same LC network) without the dynamic SCA units, η_{MN} of the DMN is 3% lower at the highest n (i.e., 78.68% η_{MN} without the dynamic switches). Yet, DMN can significantly improve η_{MN} at lower n (i.e., better back-off PAE), as discussed in the next part.

To estimate the power consumption of switching SW_{DMN} during operation, the switching loss calculation can be used,

$$P_{SW} = \frac{1}{2} f_s C_{SW} V_{SW}^2 \tag{8}$$

where P_{SW} is the estimated power consumption of switching SW_{DMN}, f_s is the average frequency of switching SW_{DMN}, C_{SW} is the total capacitance (i.e., 31×0.3pF) of SW_{DMN} and V_{SW} (i.e., 2.5 V) is the switching voltage entailed for SW_{DMN}. Considering the worst case, assuming all SW_{DMN} switches are switched in each clock cycle (i.e., 100 MHz). The calculated highest power consumption P_{SW} is 3 mW, which is small out of the overall power consumption.

From simulations, when D_{DMN} reduces from [11111] to [00000], the resonance frequency of the DMN shifts from 2.4 to 3.5 GHz, and the 3rd harmonic filtering from DMN is degraded from 24.5 to 10.3 dB. The AM signal is not affected since it operates within a narrow bandwidth. With a modulated signal, however, the 3rd harmonic introduced by this effect is limited, since a larger harmonic is only produced at a low P_{out}. Thus, the harmonic power is also limited. From simulations, when the PA delivers at the highest P_{out} with D_{DMN} = [11111] and switched to D_{DMN} = [00000] with a 6-dB P_{out} back-off at the same period, the 3rd harmonic raises only from −34.04 to −26.35 dBc. To further validate this effect, the harmonic measurement with a modulated signal can be found in the next section.

D. η_{MN} Improvement

The multi-bit DMN not only improves η_{PA}, but also improves η_{MN} of itself. From simulations, ESR_L contributes >90% to the power loss and dominates η_{MN}. Thus, a simplified circuit model can be built in Fig. 10 for η_{MN} analysis. The power loss in ESR_L can be expressed as,

$$P_{loss,MN} = |I_{MN}|^2 \cdot ESR_L. \tag{9}$$

where I_{MN} refers to the RMS current in MN. The impedance of ESR_L (0.5 Ω) is small compared to the impedance of Z_{DMN} (>2.5 Ω), thus I_{MN} can be assumed to be controlled by Z_{DMN} only. Therefore,

$$P_{loss,MN} = |I_{MN}|^2 \cdot ESR_L \approx \frac{V_d^2 n^2 ESR_L}{R_{load}^2} \tag{10}$$

and the output power can be directly formulated as,

$$P_{out,MN} = V_d \cdot I_{MN} \approx \frac{V_d^2 n}{R_{load}} \cos\varphi. \tag{11}$$

Thus, η_{MN}can be expressed by,

$$\eta_{MN} = \frac{P_{out,MN}}{P_{out,MN} + P_{loss,MN}} \approx \frac{R_{load}\cos\varphi}{R_{load}\cos\varphi + nESR_L}. \tag{12}$$

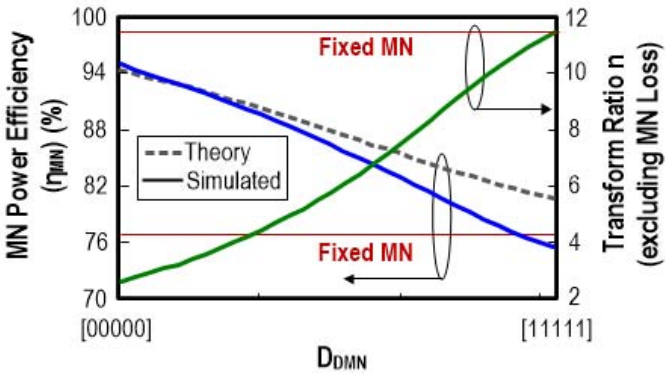


Fig. 11. Simulated DMN transform ratio (n) and power efficiency (η_{MN}) for each D_{DMN} input code.

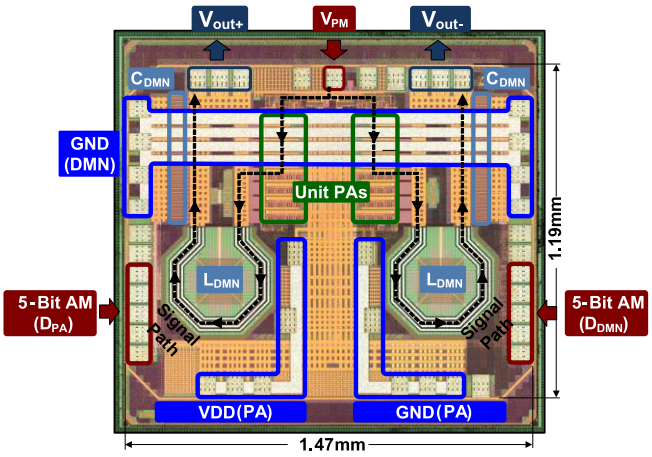


Fig. 12. Chip photo of the fabricated polar PA in 65-nm CMOS.

(12) shows that η_{MN} depends on both ESR_L and n. ESR_L is limited by the process, but n can be easily transformed through the SCA in the DMN. The reason for such improvement can also be observed from (10), as the capacitance is switched to a lower value, the current in L_{DMN} decreases, reducing the I^2R loss in ESR_L. The simulated n and η_{MN} with respect to the DMN input codes are shown in Fig. 11. C_{DMN} drops from 9.47 to 3.15 pF implying n drops from 11.42 to 2.6. Such a flexible n leads to an improvement of η_{MN} from 75.68% to 95.38%. The theoretical value from (12) is also plotted in Fig. 11 for comparison. They match well when n is small, but depart from each other when n goes up since the assumption of I_{DMN} made in (10) gets weaker. Nevertheless, the improvement trend of η_{MN} is observed when n is backed-off.

V. Experimental Results

A. CW Tests

The PA prototype is fabricated in a standard 1.2-V 65-nm CMOS and occupies a die size of 1.47 × 1.19 mm^2 (Fig. 12). All V_{DD} and ground node are differentially shorted on chip through the top metal, reducing ground bouncing effects introduced by the bondwires. The testbench is sketched in Fig. 13. The off-chip balun is 1:1. The on-chip MN has an n of 11.42 and has a similar insertion loss as other works. In CW tests, the 5+5 bit (D_{PA}, D_{DMN}) input is swept while the PM is fixed. P_{out} and PAE at each input code word are plotted on the scatter diagram (Fig. 14). The maximum P_{out} (for the fundamental tone) is measured as 22.03 dBm at 2.33 GHz, and the corresponding PAE is 42%. Note that the PAE calculation includes all the powers consumed by the driver-inverter-chain (~81 mW) and the unit power cells. The measured P_{out} is 0.56 dB lower than the simulated value discussed before (i.e., 240 mW × 75.68% η_{MN}). The measured PAE is 2.07% lower than the simulated value (i.e., 44.07%). The maximum PAE is 48.65% and the improvement of PAE at 1-dB back-off is 15.8%, when comparing to the peak PAE. The PAE enhancement is related with the η_{MN} improvement at lower n (i.e., back-off region), while Z_{PA} is tuned from the maximum power region to the maximum PAE region. It is also related to power consumption reduction in driver chain when power gated. The maximum PAE can be tracked until 3.6 dB back-off limited by P_{INV}, and the PAE is upheld over 37% at a 6-dB power back-off (essential to ensure the PAE_{ave} is high for OFDM signals). Fig. 15 shows the measured P_{out} and PAE with respect to the input codes: D_{PA} and D_{DMN}. Assuming D_{DMN} of [11010] is selected for the maximum P_{out} at D_{PA} of [11111], the measured PAE at 6-dB back-off with fixed D_{DMN} is measured as 27.42% (D_{PA} = [00100] and D_{DMN} = [11010]). Here, with the DMN, an input code D_{PA} of [00011] and D_{DMN} of [00000] can be selected with a PAE of 36%. This improvement not only comes from the higher η_{PA} and η_{MN}at the back-off region, but also the power reduction in the driver-inverter-chain when D_{PA} is reduced. This power reduction comes from the power efficiency improvement in the matching network as discussed in (8). From the experimental results, a PAE improvement of 31.29% from DMN at 6-dB back-off can be concluded. To compare the measured back-off PAE with the simulated one, we can observe that, at D_{PA} = [01000], the PAE improves from 42.32% to 47.44% (i.e., 11.0% higher) when D_{DMN} gets small. This result is consistent with the simulated η_{PA} and η_{MN} improvements reported in Fig. 7 and Fig. 11, respectively. The enhancement in PAE can be calculated as 1.21 (Fig. 7) × 1.09 (Fig. 11) = 1.32 (i.e., 32% improvement). Since the ratio of power consumption in driver chain to P_{out} is higher at a higher Z_{DMN}, a ratio of 0.87 needs to be multiplied by the enhanced PAE. The resulted overall PAE becomes 1.32 × 0.87 = 1.15 (15% higher). Note that the P_{out} and PAE measured at D_{PA} = [00000] is mostly generated by the PM pulse feedthrough, and it is a rough estimation. The measured leakage current while D_{PA} = [00000] is ~20 μA, which includes not only the PA itself but also the ESD pads without any extra power switches. The center frequency of the PA is slightly drifted to 2.33 GHz, but still P_{out} = 21.88 dBm and peak PAE = 47.58% at 2.4GHz, and P_{out} = 20.53 dBm and peak PAE = 34.77% at 2.5 GHz. The loss from the off-chip Balun and SAW filter are compensated as a common practice (e.g., [6] and [10]) to demonstrate the actual performance of the PA. The proposed PA, alike other reported switched-mode PAs [6]–[12], has strong baseband non-linearity in order to achieve a higher PAE. Therefore, this PA cannot be used without digital predistortion (DPD).

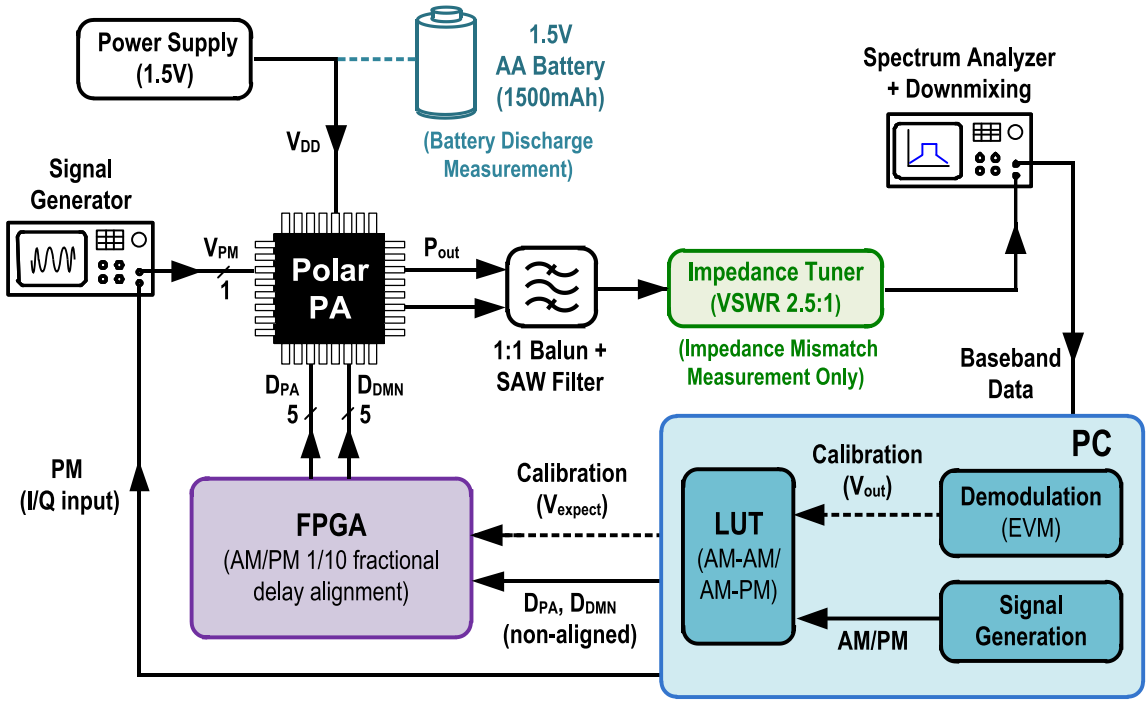


Fig. 13. Measurement setup.

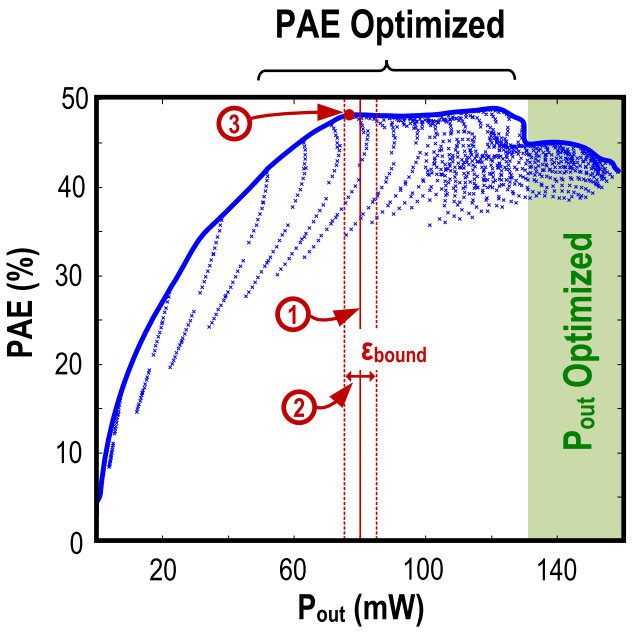


Fig. 14. PAE and P_{out} under CW measurements.

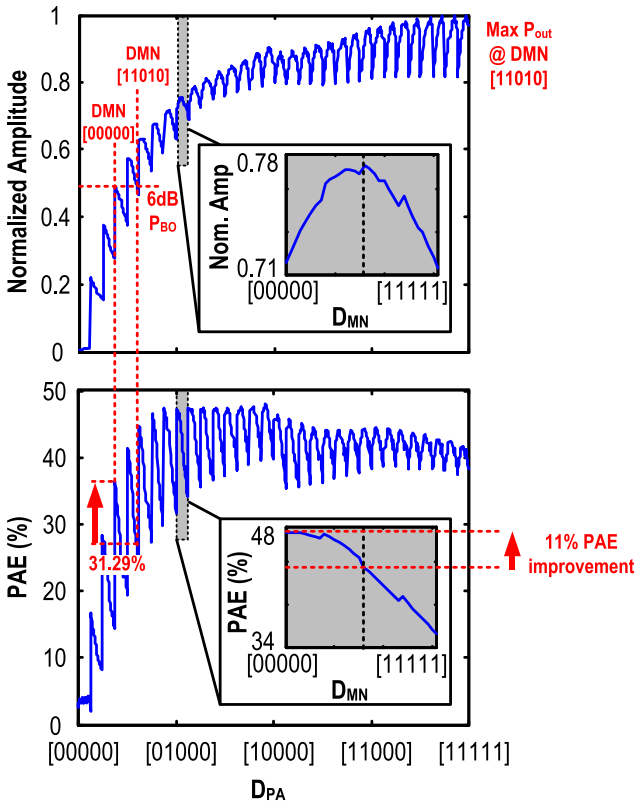


Fig. 15. P_{out}/PAE over control words, D_{PA} and D_{DMN}.

B. P_{out}/PAE Tradable LUT Calibration

A look-up-table (LUT) based calibration scheme is proposed. Unlike the typical DPD, it can calibrate the nonlinearity (i.e., memoryless digital pre-distortion [23]) and helps the trade-off between P_{out} and PAE (Fig. 16). The key steps are also referred to Fig. 14 to ease the understanding. In Step 1, at each expected AM level (V_{expect}), the 5+5 bit AM input will be swept, and P_{out} and PAE at each data will be measured and recorded into a table. From it, V_{out} error (ε') can be calculated by subtracting the measured V_{out} and V_{expect}. In Step 2, the value of ε (error upper bound) is set to trade P_{out} and PAE. The data with $\varepsilon' < \varepsilon$ will be included in a temporary data set for PAE optimization. In Step 3, the maximum-PAE data are mapped to the corresponding V_{expect} in the LUT.

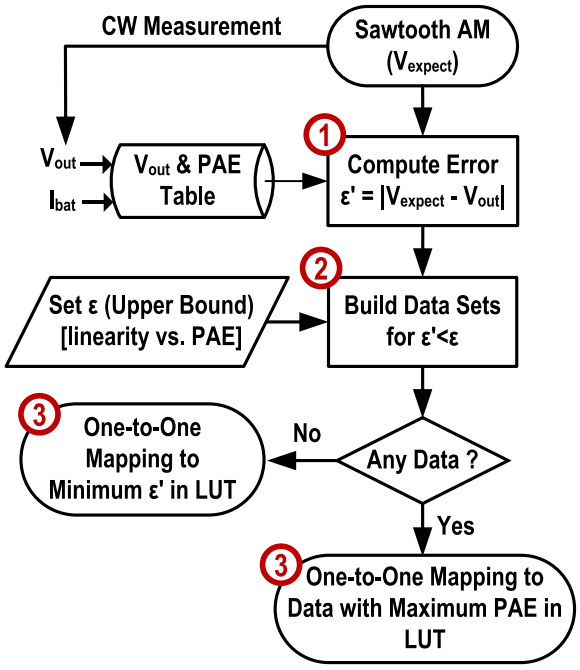


Fig. 16. P_{out}/PAE tradable LUT calibration.

A higher ε means more CW data will be included in the data set, and a higher PAE can be achieved. If ε is excessive, the error tolerance will be enlarged, degrading the PA linearity. In order to pass the EVM and mask requirements, the clipping ratio has to be changed. This leads to a reduced Pout. Thus, the P_{out} and PAE can be traded via varying ε. The highest P_{out} is at $\varepsilon = 0$.

The V_{expect} resolution is a tradeoff between linearity and complexity. A 10-bit AM resolution allows better measurement accuracy. The gain (maximum value) of V_{expect} also needs to be selected in order to avoid using the high power region that has a low back-off PAE. In the P_{out}-optimized mode, such gain is set to unity. When PAE_{ave} is the priority, the gain is reduced to 0.95 to place the maximum P_{out} at an AM code with a higher PAE.

During the active operation, only one or two (for mode switching) LUTs are entailed. Each LUT draws much smaller power (e.g., 875 μ W with 10-bit resolution in 65nm CMOS from simulation) when comparing with the total power consumption of the PA (100 to 200 mW). Here, the PA nonlinearity model includes not only the nonlinearity of the class-D PA unit cell [3] and the gain and phase non-linearity of the MN but also the interaction between these two nonlinearities. For the applied DPD algorithm, the AM signal is sensed from the output node directly, and the input code includes both D_{PA} and D_{DMN}, thus the DPD calibrates the non-linearity as a whole.

C. 64-QAM OFDM Tests

A 64-QAM 52 sub-carrier OFDM signal is polarized into separated AM and PM off-line in a computer (Fig. 13). V_{PM} is given by the signal generator, whereas D_{PA} and D_{DMN} are obtained from a pre-calibrated 5+5 bit LUT. The AM-PM alignment is based on a FIR filter in a typical FPGA, offering 1:10 fractional delay. Note that no obvious misalignment is observed for D_{PA} and D_{DMN} at 100 MHz. For a 2-MHz signal bandwidth, the spectrum mask and EVM in the P_{out}-optimized mode are plotted in Fig. 17(a). The achieved $P_{out,ave}$ at maximum P_{out} ($\varepsilon = 0$) is 16.89 dBm with PAE_{ave} of 34.79%. By reselecting ε as 3.25, the PAE_{ave}-optimized mode results in a PAE_{ave} of 40.66% at 16.25-dBm $P_{out,ave}$. $\varepsilon > 3.25$ will cause strong quantization noise in the spectrum. The same signal is also down-sampled for a 20-MHz bandwidth (802.11g) as shown in Fig. 17(b) with the same P_{out} and PAE_{ave}. Limited by the 100-MHz baseband sampling rate and internal filter of the signal generator (Agilent E4438C), strong out-band V_{PM} error is induced, and the 2nd adjacent channel leakage ratio (ACLR2) is 12-dB short from the expected value. Such bandwidth limitation and the out-of-band replicas (–30 dBr at 10/50 MHz) due to direct digital-to-RF conversion can be resolved with wideband phase mixing and upsampling in the baseband signal generation [11]. Nevertheless, the measured in-band EVM and ACLR1 match well with the expected values. Besides, all 64-QAM OFDM signals are clipped according to the −25-dB EVM and spectrum mask requirements, thus maximizing $P_{out,ave}$ and PAE_{ave}. It is possible to further improve the linearity by backing-off more $P_{out,ave}$. For instance, at the P_{out}-optimized mode, –30-dB EVM can be achieved under 1.35 dB back-off of P_{out} (i.e., 15.54 dBm) while upholding a high PAE_{ave} of 31.72%.

A similar P_{out} and PAE is expected for IEEE 802.11n or 802.11ac signals due to their similar PAPR level. Yet, the AM and PM paths will entail significant baseband bandwidth extension.

The out-of-band 2nd and 3rd harmonics with a modulated signal measure −63.5 and −60.4 dBc with the SAW filter, and −26.5 and −25.4 dBc without the SAW filter, respectively.

D. Battery Lifetime Extension via P_{out}/PAE Mode Switching

Mode switching from PAE- to P_{out}-optimized modes at appropriate timing can help extending the battery lifetime. Assume the long-term power target is 14.5 dBm under a 1.5-V AA battery to reach out the interested access point, if the PA continuously operates at the PAE-optimized mode, only 9 hours of operation is achieved in real-time. A similar result (8.8 hours) is achieved under the P_{out} optimized mode. Yet, if the PA is switched to P_{out}-optimized mode after the 5th hour, the PA successfully operates for 11.5 hours as shown in Fig. 18. In other words, the lifetime of the battery is extended by 2.5 hours. A 27.78% battery lifetime extension is achieved. By boosting up the power through mode switching when the access point is beyond the reachable distance as the voltage in battery drops, the access point has a higher chance to be reached again at the cost of extra power. In fact, re-reaching the access point is more important than reserving the power.

No obvious linearity degradation is observed during the battery voltage drop. Moreover, the slow voltage drop will not impact the 802.11g communication quality since each packet length is only 4 μs.

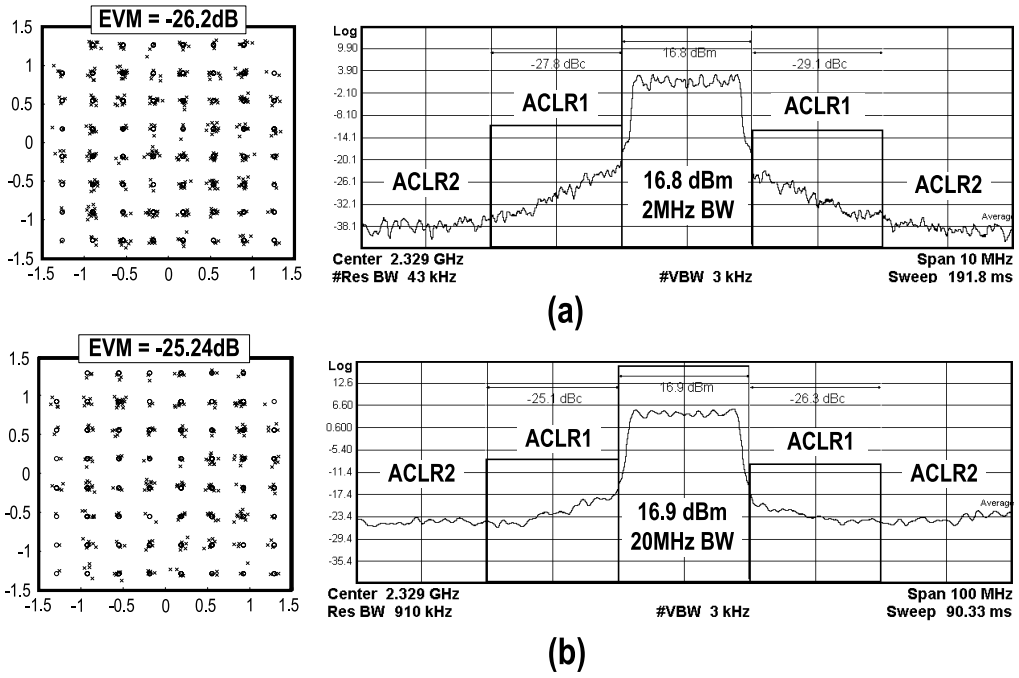


Fig. 17. Measured RF outputs under (a) 2-MHz and (b) 20-MHz 64-QAM OFDM signals.

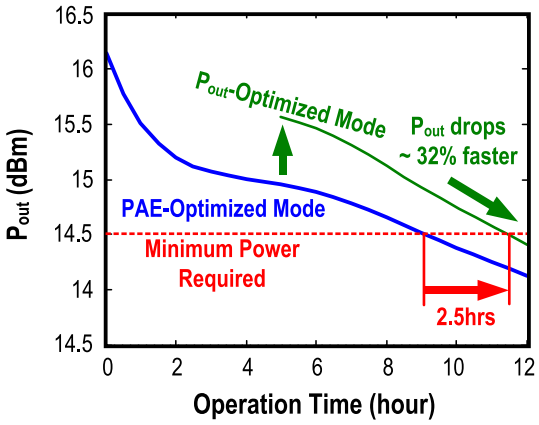


Fig. 18. Measured battery lifetime extension via switching between P_{out}/PAE-optimized modes.

E. Antenna Impedance Correction

An interesting feature of the proposed polar PA is that its high-resolution DMN can correct partially the antenna impedance mismatch. As discussed, the DMN can be utilized to change the load impedance Z_{DMN} under a fixed antenna impedance (Z_{ANT}). In fact, it can also work in the opposite manner, correcting the antenna to a fixed Z_{DMN}.

To study the accessible Z_{ANT}, the DMN is simulated and modeled with Z-parameters since the Z-parameters are independent of the impedance from the two terminals of the network, and they also have a well-defined relationship between the input and output impedance of the network as,

$$Z_{DMN}=Z_{11}-\frac{Z_{12}Z_{21}}{Z_{22}+Z_{ANT}}. \tag{13}$$

Thus, the accessible Z_{ANT} with given Z_{DMN} can be calculated as follow,

$$Z_{ANT}=\frac{Z_{12}Z_{21}}{Z_{11}-Z_{DMN}}-Z_{22}. \tag{14}$$

Fig. 19 shows the calculated Z_{ANT}'s trace that can be corrected to achieve a maximum P_{out} (i.e. $Z_{DMN} = 2.5\ \Omega$) from (14) with different D_{DMN}. A wider accessible impedance range can be achieved with a higher order DMN, at the cost of higher insertion loss and larger chip area. However, in practice, for Z_{ANT} outside the trace, P_{out} and PAE can still be enhanced by applying DMN antenna impedance correction, even though the maximum P_{out} cannot be achieved.

The antenna impedance can be automatically calibrated with the proposed LUT calibration scheme as well as the linearity. For each quantization step, the best PAE and P_{out} can be automatically re-searched from the DMN impedance traces, avoiding the need of extra calibration. The experimental validation was done with an impedance tuner as shown in Fig. 13. An impedance mismatch of 2.5:1 VSWR was commonly chosen for impedance mismatch calibration [24], and the reflection angle was chosen randomly as 180 °. From the results, the calibration successfully improves $P_{out,ave}$ from 11.47 to 11.86 dBm, and PAE_{ave} from 15.49% to 15.91%. The impedance correction mechanism can be further improved by increasing the impedance tuning range.

F. Chip Summary and Performance Summary

Benchmarking with the recent 2.4-GHz CMOS PAs (Table I), this work succeeds in improving the PAE_{ave} by >13.7% under a single 1.5-V supply. Thanks to the power-gating, the total leakage current (PA + ESD pads)

TABLE I
CHIP SUMMARY BENCHMARK WITH THE STATE-OF-THE-ART 2.4-GHz CMOS PAs

	This Work		R. Hezar et al. JSSC'15 [10]	V. Chironi et al. TCAS I'13 [12]	L. Ye et al. ISSCC'13 [11]	P. Madoglio et al. ISSCC'12 [9]	Y. Yin et al. TCAS II'10 [13][e]
	P_{out}-Opt. Mode	PAE-Opt. Mode					
Frequency	2.4 GHz		2.4 GHz	2.4GHz	2.4 GHz	2.4 GHz	2.4 GHz
Key Techniques	**Power-Gated Class-D PA + Multi-Bit DMN + Mode Switching**		PWM + Sigma-Delta	Class-E PA + DMN	Inverse Class-D PA + Single-Bit DLM	Delay Line + Class-D PA + Out-Phasing	Power Combining
Technology	Standard 65nm CMOS		Standard 45nm CMOS	Standard 90nm CMOS	Standard 65nm CMOS	32nm CMOS + Ultra-Thick Metal	Simulated 0.13µm CMOS
Supply Volt. (V)	1.5 [a]		1.7/1.2	1.2	1.2	1/2.05	1.2
Peak P_{out} (dBm)	22.0		23	9	23.3	25.9	25.1
Peak PAE (%)	**48.7**		47	30	38	N/A	33.5
$P_{out,ave}$ (dBm) [b]	**16.9 (15.54)**	**16.3**	14.8	3.2[d]	16.8	20.0	16.2
PAE_{ave} (%) [b]	**34.8 (31.7)** [c]	**40.7** [c]	23	7[d]	21.8	22	26
EVM (dB) [b]	-25.2 (-30)	-25	-29	N/A	-28	-25	-25
Leakage Current (µA)	**20 (TX + ESD pads)**		N/A	N/A	N/A	N/A	N/A
Antenna Impedance Correctability	**VSWR 2.5 : 1 @ 180°** **$P_{out,ave}$ = 11.47→11.86 dBm** **PAE_{ave} = 15.49→15.91%**		No	No	No	No	No

a : For direct 1.5-V AA battery powering, and P_{out} is >14 dBm over 12-hour of continuous operation.
b : For a 20-MHz 64-QAM OFDM signal, the EVM target is –25 dB for 802.11g [9].
c : PAE_{ave} = 52% by mode-switching from P_{out}-optimized to PAE-optimized modes under the AA battery test. The ACLR2 is verified at 2-MHz signal [Fig. 17(a)], but not 20 MHz [Fig. 17(b)] due to the limited 100-MHz baseband sampling rate and internal filter of the signal generator.
d : Estimated value from reported back-off PAE with same PAPR from this work.
e : Simulated result with 16.25MHz 64-QAM signal with no OFDM. PAPR is similar, and therefore comparable.

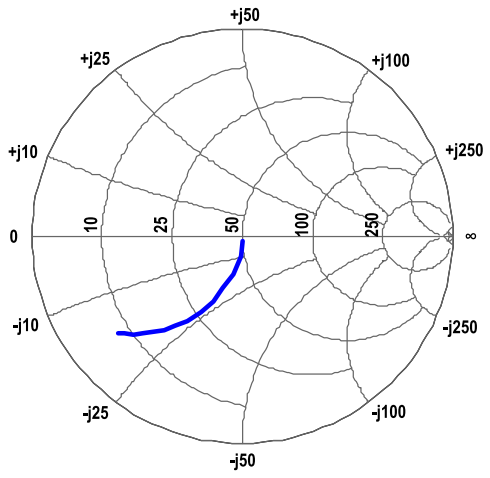


Fig. 19. Simulated Z_{ANT} that can be corrected with DMN antenna impedance correction to produce a maximum P_{out} on a smith chart.

in off state is minimized to 20 μ A. The antenna-impedance correctability and dual operating modes (P_{out}-optimized and PAE-optimized) are the added new features.

VI. CONCLUSIONS

Architectural and circuit techniques were introduced for a digitally-modulated class-D polar PA to achieve a high PAE_{ave}. Load-pull optimization is realized by a 5+5-bit interactive AM-AM modulation between the unit amplifiers and DMN, improving their power efficiency during the power back-off. The DMN also can aid the antenna impedance correction for better $P_{out,ave}$ and PAE_{ave}, offers two operating modes: P_{out}-optimized and PAE-optimized. Switching from P_{out}-optimized to PAE-optimized modes can virtually reconfigure the PA for the battery lifetime extension. The embedded power gating technique enables the PA to reliably operate at 1.5 V and reduces the leakage current (20 μ A). For a 20-MHz 64-QAM OFDM output at a typical EVM (< -25 dB), the achieved PAE_{ave} is 40.7%, and is improvable to 52% by mode switching.

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