An Analog-Proportional Digital-Integral Multiloop Digital LDO With PSR Improvement and LCO Reduction

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***Abstract*— This article presents a low-dropout regulator (LDO), with analog-proportional (AP) and digital integral (DI) controls. The design concerns are discussed at first, on how to improve the load transient response, enhance the power supply rejection (PSR), and reduce the limit cycle oscillation (LCO). For a good output dc accuracy, the DI section is implemented with shift-register-based coarse- and fine-tuning loops. Meanwhile, the AP section, based on a low-supply flipped-voltage follower (FVF), can respond fast to the load step and input supply ripple. A replica loop is used to define the steady-state output current of AP, allowing a sufficient dynamic swing against the supply ripple. To lower the load current range with no LCO, the AP section will output all the current at very light load. An error amplifier (EA) with moderate gain is added to improve the light-load output accuracy. This EA also improves the PSR by approximately 6 dB. Fabricated in a 65-nm CMOS process, a 65-mV undershoot is measured with a 0–10-mA load current step under 0.6-V supply voltage and 50-mV dropout. Due to the fast AP, a 5-MHz operation clock is applied to the digital section, reducing the overall quiescent current to 29 μA. A 0.37-ps figure of merit (FoM) is then achieved. A −22-dB PSR at 1 MHz is measured at 0.6-V supply, 100-mV dropout, and 10-mA load current.**

***Index Terms*— Digital, fast response, low dropout regulator (LDO), power supply rejection (PSR), proportional-integral (PI) control.**

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I. Introduction

RESOURCES are used in a dynamic way in power-efficient digital integrated circuits (ICs) nowadays. To fulfill the dynamics, multiple integrated voltage regulators (IVRs) are used to supply the fine-grained voltage domains independently [1], [2], as a granular power management [3]. Each IVR typically combines a switched-capacitor power converter and a low-dropout regulator (LDO), where the LDO should work with a small dropout (typically <100 mV) for high efficiency. Hence, conventional analog LDOs (ALDO) [4]–[6] are not suitable for these applications, because the power transistor needs to work in saturation region with a relatively high dropout voltage (V_{dropout}). Instead, digital LDOs (DLDO) [7]–[28] are attractive since the digitized power transistors (controlled by a digital word n) can work like switches with a low V_{dropout}. This switch-like feature also helps to conduct more load current under the same power transistor size. Meanwhile, the control of DLDO works with a low voltage and enjoys the benefits of process scalability, which is inherently compatible to digital ICs.

One of the major design challenges of a conventional DLDO is the power-speed tradeoff. To prevent a large spike on the output voltage (V_{OUT}), the DLDO should find the correct n within a very short time. This typically requires the controller to work with a high operation frequency (f_{CLK}) and, thus, a high power consumption. Several previous works have been proposed to mitigate this tradeoff by sizing unequal power transistors [3], [8]–[12] or asynchronous control [13]–[16]. For instance, large grain power transistors are activated for a fast transient response (coarse-tuning), while small ones are used to ensure steady-state accuracy (fine-tuning) [3], [8]–[10]. Also, recovery time can be further reduced by changing the control word in a binary [11] or an exponential [12] way. Asynchronous control [13]–[16] tries to save power by removing the global clock signal and driving the control logics from their previous stage. Nevertheless, without a power-hungry quantizer, these schemes may still have difficulty in dealing with a sharp I_{LOAD} change [17].

Proportional-integral (PI) control [18]–[24] can also be a good candidate for the power-speed tradeoff, as conceptually explained in Fig. 1. The conventional shift-register (SR) - based DLDO [7] is essentially an I-only control, offering a high dc gain/accuracy but slow response. Inversely, the P-only control responds fast but fails to reduce the steady-state error. Hence, it is straightforward to combine these two controls, for simultaneously fast response and high

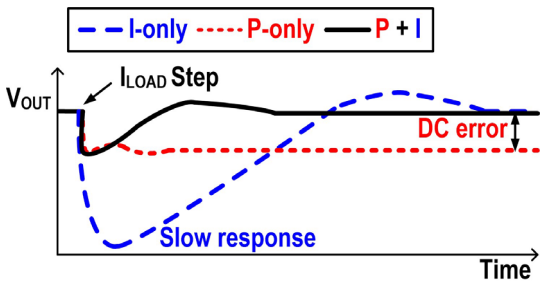


Fig. 1. Conceptual transient waveforms of $V_{\rm OUT}$, under I-only, P-only, and PI controls.

dc accuracy. In [20] and [23], the analog loop is used for I-control, while the digital part compensates the large transient current step. However, regarding the low $V_{\rm IN}$ and low $V_{\rm dropout}$ scenarios, the implementation of the I-/P-controls is still worth investigating.

Furthermore, for digital IC applications, a moderate power supply rejection (PSR) is typically required to resist the MHz-level input noise, mainly from the prestage switching converter. A good PSR can be achieved by ALDOs [4]–[6], but it will be degraded when the loop gain of ALDO is reduced under low $V_{\rm IN}$ and $V_{\rm dropout}$. For DLDO, the PSR is inherently worse due to the discontinuous operation, which will be explained in Section II.

Finally, the minimum load current ($I_{\rm LOAD,min}$) of the DLDO may be constrained if only a small on-chip output capacitor ($C_{\rm OUT}$) is used. A large steady-state limit cycle oscillation (LCO) will be excited at light load. Tsou *et al.* [25] uses a tracking bound method to reduce the LCO under process, voltage, temperature (PVT) variations. Huang *et al.* [26] uses a feed-forward path to reduce the LCO to mode-1, i.e., one least significant bit (LSB) power transistor turns on and off at steady state. However, even this mode-1 LCO may not be acceptable at a very light-load condition. Designing a smaller LSB current ($I_{\rm LSB}$) can reduce the LCO, but it trades with an increased complexity to cover a wide $I_{\rm LOAD}$ range.

To address the aforementioned issues, we propose an analog-proportional, digital-integral (AP-DI) LDO in this article, as an extension of [27]. We aim at an improved PSR, a reduced LCO, an $I_{\rm LOAD,min}$ extension to 0, and a fast transient response. These are achieved under a low $V_{\rm IN}$ and $V_{\rm dropout}$ and a small quiescent current I_Q. This article is organized as follows. Section II describes the design considerations of the AP-DI LDO. Section III presents the working principle and circuit implementations. Section IV shows the measurement results, and finally, Section V draws the conclusions.

II. Design Considerations on the AP-DI LDO

For DLDO, it is convenient to design I-control in a digital way, i.e., conventionally using an SR [7], which is essentially an integrator providing a dc pole and, thus, a high dc gain and good steady-state accuracy. However, how to design P-control is worth further investigation. This section discusses the design considerations from the aspects of load transient response, PSR, and LCO.

A. Load Transient Response

For an LDO with the P-control, the undershoot voltage $\Delta V_{\rm OUT}$ can be approximately presented by

$$\Delta V_{\rm OUT} = \max\left\{\frac{\Delta I_{\rm LOAD}\cdot\tau_{\rm DELAY}}{C_{\rm OUT}}, \frac{\Delta I_{\rm LOAD}}{A_P\cdot g_{\rm mP}}\right\} \quad (1)$$

where $\Delta I_{\rm LOAD}$ is the load current step, $\tau_{\rm DELAY}$ is the P-control response delay to the $\Delta V_{\rm OUT}$, $g_{\rm mP}$ is the transconductance of the output power transistor, and A_P is gain of P-control. The $\Delta I_{\rm LOAD}\cdot\tau_{\rm DELAY}/C_{\rm OUT}$ term is the voltage droop caused by the delay, while the $\Delta I_{\rm LOAD}/(A_P\cdot g_{\rm mP})$ term represents the $V_{\rm OUT}$ droop for P-control to compensate $\Delta I_{\rm LOAD}$.

Fig. 2 shows the multiple models of the P-control, and the possible response to the load step. In Fig. 2(a), the P-control is implemented in a digital way (DI-DP control). The DP control can be beneficial to obtain a large P-gain ($A_{\rm P1}$), minimizing the $\Delta I_{\rm LOAD}/(A_P\cdot g_{\rm mP})$ term in (1). However, the discontinuous sampling of the digital P-control stage, represented by z^{-1}, will cause a delay time $\tau_{\rm D1}$ in response. Then a significant $\Delta V_{\rm OUT}$ will still take place for a sharp $I_{\rm LOAD}$ step, since a large quantity of instant charge (shaded area) is needed from the output capacitor within the delay interval. To shorten the delay, a power-consuming sensor is often utilized [18].

The P-control can also be achieved in an analog way (AP control). Huang *et al.* [19] proposed an "analog-assisted"-AP [see Fig. 2(b)], feeding the $\Delta V_{\rm OUT}$ back through a first-order RC high-pass filter (HPF) almost without delay and I_Q overhead. This minimizes the $\Delta I_{\rm LOAD}\cdot\tau_{\rm DELAY}/C_{\rm OUT}$ term. However, the passive HPF only contributes a P-gain ($A_{\rm P2}$) smaller than 1, hence a relatively large undershoot still occurs. In addition, this scheme is effective only with a certain number of power transistors turned on, limiting the $I_{\rm LOAD,min}$. The turned-off power transistors are designed to make contribution in [20], by using the n-type power transistor. Nevertheless, to turn on the NMOS, the gate-drive voltage is required higher than the $V_{\rm IN}$. Still, large undershoot takes place because of the insufficient P-gain. Wang and Mercier [24] feed the $\Delta V_{\rm OUT}$ back using a capacitor between gate-drain of the power transistor, fulfilling a larger p-gain.

Now the proposed realization of PI control is given in Fig. 2(c), where AP is implemented with active circuits. Consequently, a moderate P-gain ($A_{\rm P3}$) and small delay ($\tau_{\rm D2}$) can be achieved. Now both terms in (1) are smaller than that of DI-DP or "analog-assisted" DI-AP cases making the overall $\Delta V_{\rm OUT}$ smaller. It should be noticed that under a low $V_{\rm IN}$ and $V_{\rm dropout}$ in digital ICs, the AP with moderate P-gain and small delay should be achievable, such as using a flipped-voltage follower (FVF) topology to be discussed afterward.

B. PSR

For a conventional DLDO, the PSR is typically not as good as its analog counterpart, which is explained in Fig. 3.

First, significant glitch will be excited by the discontinuous sampling and n changing. Assume control word n is synchronized at the rising edge of the operation clock (CLK). We define the optimum $n(n_{\rm opt})$ that makes $V_{\rm OUT} = V_{\rm REF}$ at the steady state. Also, we assume the controller manages to find out the $n_{\rm opt}$ at each synchronization (t_0, t_1, t_2, t_3), which

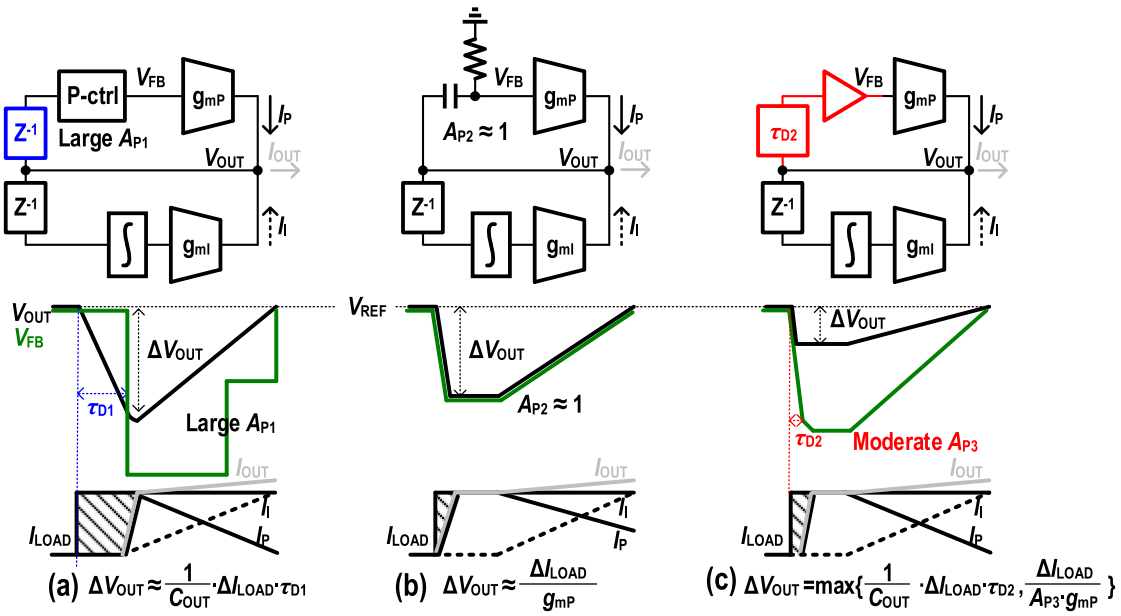


Fig. 2. Models and transient waveforms of the LDO with (a) DI-DP, (b) DI-"analog-assisted" AP, and (c) proposed DI-AP control.

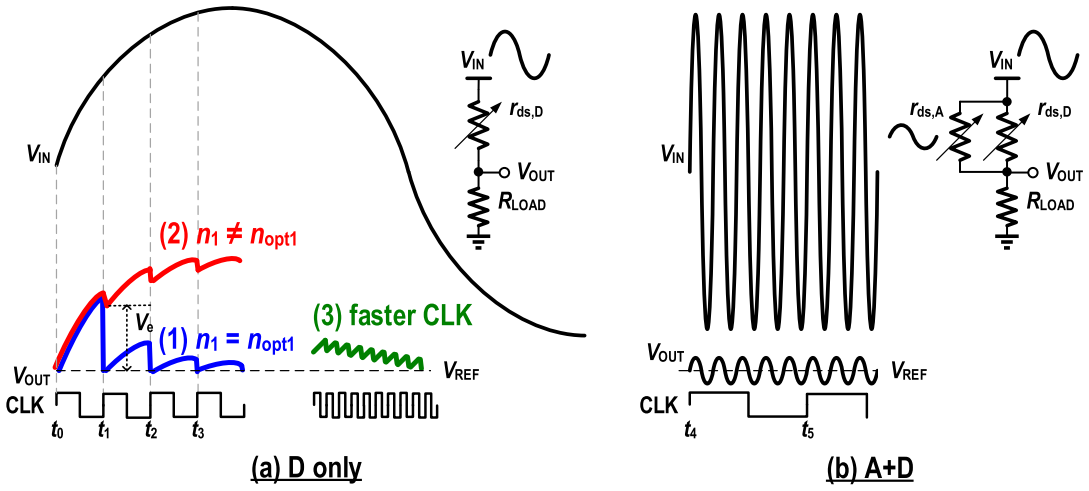


Fig. 3. Waveforms of V_{OUT} with a V_{IN} ripple for (a) digital-only and (b) analog-digital combined implementations. For digital-only control, the controller may ideally find out the optimum n and cannot find out the optimum n in time. PSR can be improved by a faster CLK.

is the most ideal case, if not impossible. Then, V_{OUT} is pulled back to V_{REF} at every CLK rising edge. However, even in this ideal case, the V_{OUT} ripple is partially reduced, because n is not adjustable during the sampling intervals, e.g., from t_0 to t_1. Hence, during the intervals, the PSR can be written as a resistive divider

$$\text{PSR} = \frac{1}{\frac{R_{\text{LOAD}}}{r_{\text{ds},D}} + 1} \tag{2}$$

where R_{LOAD} is the load resistance, and $r_{\text{ds},D}$ is the instant resistance of the power transistor array. This makes LDO still vulnerable to V_{IN} noise.

Second, the nonoptimum n further increases the amplitude of the V_{OUT} ripple. Assume the control word n is the same for both optimum and nonoptimum cases at the starting point t_0. If $n_1 \neq n_{\text{opt1}}$ at t_1, an error of $V_e = V_{OUT} - V_{REF}$ exists (typically $n_1 < n_{\text{opt1}}$ and $V_e > 0$). Then, from t_1 to t_2, V_{OUT} starts to increase from V_e, making the V_{OUT} ripple larger.

Third, it is true that the V_{OUT} glitch can be reduced by minimizing the sampling interval (a much faster CLK), but this contradicts the power-efficient prerequisite.

Based on the analysis, the PSR of DLDO may only be improved by continuous quantization and n changing, which should incorporate an analog circuit. Fortunately, the aforementioned analog P-control offers the benefit to continuously change the output current, as shown in Fig. 3(b), by parallelizing an analog resistance $r_{\text{ds},A}$ to $r_{\text{ds},D}$. For one thing, the instant $r_{\text{ds},A}$ can be continuously changed. For another thing, feedback loops can take effort to adjust $r_{\text{ds},A}$ according to V_{IN} noise, which will be discussed afterward. Consequently,

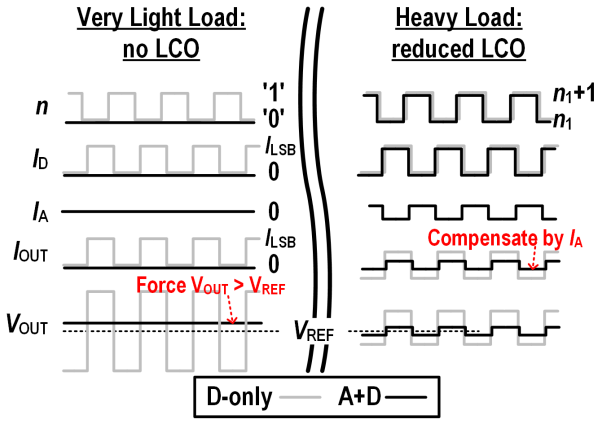


Fig. 4. Waveforms of LCO with digital-only and analog-digital combined controls, at the very light load and heavy load, respectively.

the capability of resisting a high-frequency $V_{\rm IN}$ noise is determined by the AP section, and the sampling interval (t_4 to t_5) can be longer to save I_Q.

C. LCO and $I_{\rm LOAD,min}$

The principle of LCO was explicitly analyzed in [26]. Conceptually, it is caused by quantization errors as in Fig. 4 (assume only mode-1 LCO exists). For a very light-load case where $I_{\rm LOAD} < I_{\rm LSB}$, if n changes from "0" to "1," the digitized output current I_D of the conventional DI-only LDO will change from 0 to $I_{\rm LSB}$. Then, the amplitude of steady-state $V_{\rm OUT}$ ripple can be $I_{\rm LSB} \times R_{\rm LOAD}$, if only a small $C_{\rm OUT}$ is employed. The smaller the $I_{\rm LOAD}$, the larger the $R_{\rm LOAD}$ and the steady-state LCO will be.

The large LCO at light load can also be mitigated with an AP-DI control ($A + D$). When the $I_{\rm LOAD}$ is small or even close to 0, if the AP section can take up the load current, the relatively low analog gain (typical for a low $V_{\rm IN}$ and $V_{\rm dropout}$) will force $V_{\rm OUT} > V_{\rm REF}$. This eliminates $V_{\rm OUT}$ crossing $V_{\rm REF}$, hence the DI section is deactivated and no LCO exists. However, the high dc gain feature from the DI section can no longer be enjoyed. Therefore, to avoid $V_{\rm OUT}$ deviating too much from $V_{\rm REF}$, it still requires a moderate analog loop gain for a soft regulation.

At heavy load and still assume mode-1 LCO exists, where n changes from n_1 to $n_1 + 1$. The LCO will be smaller than that of light load due to a smaller $R_{\rm LOAD}$. However, the AP section offers another benefit to further reduce the LCO. The fast-response analog current I_A provided by the AP section always compensates I_D, reducing the overall output current $I_{\rm OUT}$ ripple. Here, the degraded light-load output accuracy is no longer an issue, because the output regulation task can be taken by the digital integrator automatically.

The steady-state LCO can also be eliminated by preventing the digital logics from flipping in [23]. This can be achieved by setting a dead zone in the comparator. However, the $V_{\rm OUT}$ accuracy may be sacrificed since it is unregulated when within the dead zone. In [23], the analog part is used for the steady-state regulation.

As a brief summary, AP-DI is beneficial to the transient response. Additionally, the AP section can be reused to improve the PSR. Finally, if $I_{\rm OUT}$ is generated by AP at very light load, the steady-state LCO can be removed and $I_{\rm LOAD,min} = 0$ is allowed. Some loop gain is required for a soft regulation at light load. The heavy-load LCO can also be reduced by AP.

III. Working Principles and Implementations of the Proposed LDO

A. General Structure

The schematic of the proposed AP-DI LDO is shown in Fig. 5. In the AP part, an LDO based on an FVF is designed. The analog power transistor $M_{\rm PA}$ and the common-gate (CG) amplifier M_2 compose the fastest loop (Loop-1), to deal with the fast transient. The FVF can be achievable with a low $V_{\rm IN}$, since only $3 \times V_{\rm DS}$ or $V_{\rm GS} + V_{\rm DS}$ voltage headroom is required. To reduce the $V_{\rm OUT}$ overshoot, C_1 and M_{10} are added. In the steady state, M_{10} is biased in subthreshold region to save I_Q. The high-frequency components of $V_{\rm OUT}$ will be coupled through C_1, and M_{10} can absorb a large instantaneous current for overshoot reduction.

As discussed above, when the AP section takes over all the current at a very light load, another loop (Loop-2) should be added for regulation. Except for $M_{\rm PA}$ and M_2, Loop-2 consists of a 2-stage error amplifier (EA), made from a differential input pair M_3 and M_4, a load of current mirror M_7 and M_8, and the common-source output stage M_9. Loop-2 sets the gate voltage of M_2 based on the difference between $V_{\rm OUT}$ and $V_{\rm REF}$. Capacitor $C_{\rm B}$ is added to the output of the EA, making this node the dominant pole of Loop-2. Under a low $V_{\rm IN}$, the gain of Loop-2 might not be as high as that in a conventional ALDO, but it helps the light-load regulation and PSR, which is discussed in Section III-B.

For the DI part, it consists of three subsections (L, M, H), with 16-, 8-, and 8-bit SR-controlled power switch arrays, respectively. The power switches in these subsections are sized to achieve equivalent $16 \times 8 \times 8 = 1024$ current steps for a high dc accuracy, with carry/borrow operations between the adjacent subsections as in [19]. Hence, the overall control word n can be written as

$$n = l + 16 \cdot m + 128 \cdot h \tag{3}$$

where l, m, and h are the control word of the corresponding subsections. The coarse tuning (Loop-4) is made from M and H subsections, 64 steps in total, triggered by two comparators ($\rm CMP_2$ and $\rm CMP_3$) when $V_{\rm OUT}$ exceeds a preset boundary ($V_{\rm REF+}$ to $V_{\rm REF-}$). In the coarse tuning, n is changed by 16 every cycle, allowing a fast recovery. Finally, a fine-tuning loop (Loop-5), made from the L subsection, is enabled when $V_{\rm OUT}$ is pulled back within the ($V_{\rm REF+}$ to $V_{\rm REF-}$) boundary, and l changes according to the output of another comparator ($\rm CMP_1$). The fine-tuning ensures a high dc gain.

We notice that the analog steady-state output current $I_{A,\rm dc}$ is not defined by Loop-2 when the DI section is activated, as explained in Fig. 6(a). Since the DI section should have a larger dc gain than Loop-2, $V_{\rm OUT}$ is actually defined by the

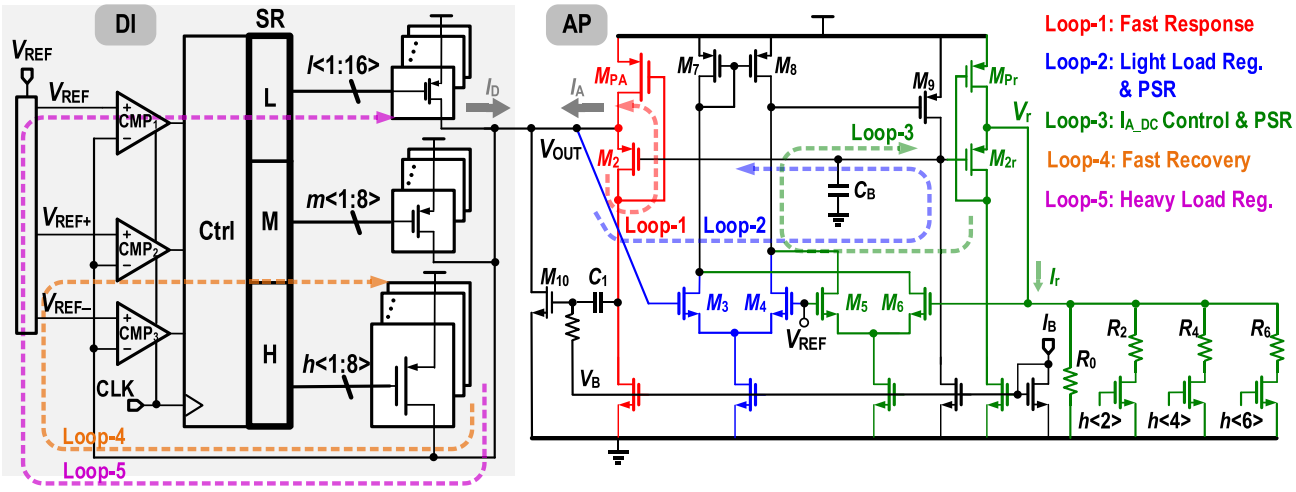


Fig. 5. Full schematic of the proposed LDO.

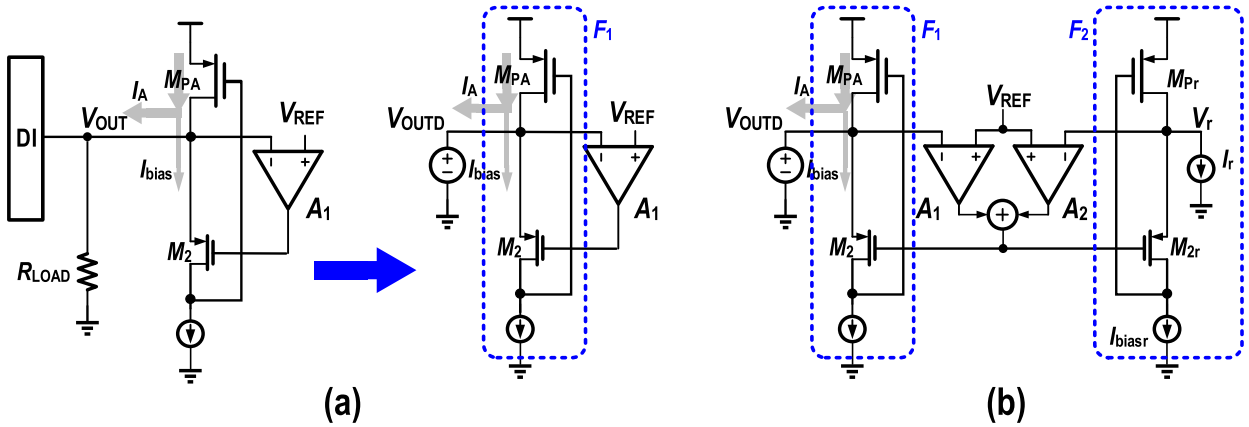


Fig. 6. I_A generation (a) without Loop-3 and (b) with Loop-3.

DI section. Hence, the DI section can be modeled by a voltage source V_{OUTD}, whose difference from V_{REF} comes from the input offset of the comparator. Then the current of M_{PA} can be written as

$$I_{\mathrm{PA}} = I_{A,\mathrm{DC}} + I_{\mathrm{bias}} \approx F_1[A_1 \cdot (V_{\mathrm{REF}} - V_{\mathrm{OUTD}})]. \quad (4)$$

Here, I_{bias} is the bias current of the FVF, A_1 is the dc gain of EA, and F_1 is a function only related to the operating points of the analog circuits. As can be seen from (4), $I_{A,\mathrm{dc}}$ is determined by V_{OUTD} and the operating points. Consequently, $I_{A,\mathrm{dc}}$ may be small or even negative if $I_{\mathrm{PA}} < I_b$. This will nullify the AP effort on transient response and PSR.

To prevent this, another loop (Loop-3) should be added to determine $I_{A,\mathrm{dc}}$. Loop-3 employs a replica path (M_{Pr} and M_{2r}), an EA, and a switched-resistor array to generate the replica current I_r. The EA uses a separate differential EA input pair (M_5 and M_6), while the rest are shared with Loop-2. The I_r can be adjusted by turning on/off the resistor array (R_2, R_4, R_6), controlled by $h\langle 2, 4, 6\rangle$ from the DI H subsection, which adaptively increases $I_{A,\mathrm{dc}}$ with I_{LOAD}. A fixed resistor R_0 is employed to ensure the AP section to take over the very light-load regulation. The M_{Pr} and $M_{2\mathrm{r}}$ are sized to be $1/300$ of M_{PA} and M_2. With Loop-3 as shown

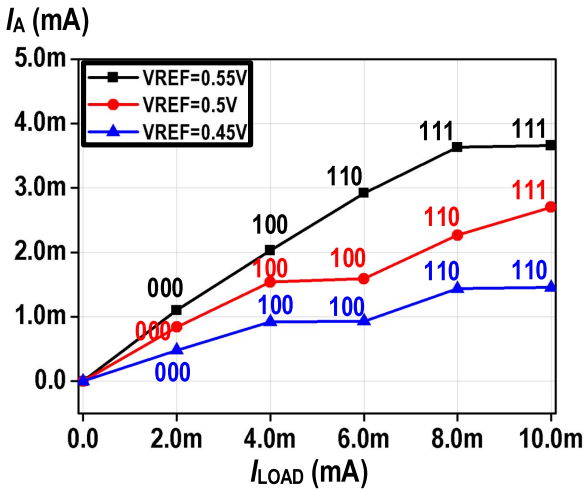


Fig. 7. Simulated $I_{A,\mathrm{dc}}$ when $V_{\mathrm{IN}} = 0.6$ V and I_{LOAD} ranges from 0 to 10 mA. The value of $h\langle 2, 4, 6\rangle$ is annotated.

in Fig. 6(b), $I_{A,\mathrm{dc}}$ and I_r can be expressed as

$$\begin{cases} I_{A,\mathrm{DC}} \approx F_1 \left[\dfrac{A_1 \cdot (V_{\mathrm{REF}} - V_{\mathrm{OUTD}}) + A_2 \cdot (V_{\mathrm{REF}} - V_r)}{2} \right] \\ I_r \approx F_2 \left[\dfrac{A_1 \cdot (V_{\mathrm{REF}} - V_{\mathrm{OUTD}}) + A_2 \cdot (V_{\mathrm{REF}} - V_r)}{2} \right] \end{cases} \quad (5)$$

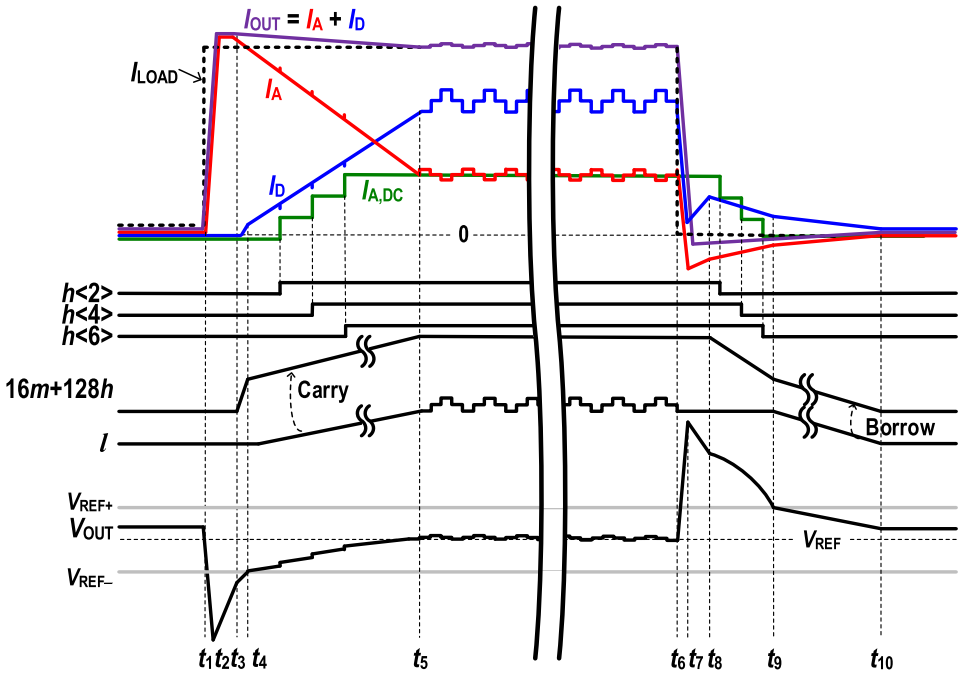


Fig. 8. Working principle of the proposed LDO at light-to-heavy and heavy-to-light load transitions.

where A_2 is the dc gains of EA in replica loop, and F_2 is the function defining I_r from the EA output. From (5), $I_{A,\mathrm{dc}}$ can be roughly defined by I_r, if the main and replica loops match, i.e., $F_1 = F_2$.

The simulated $I_{A,\mathrm{dc}}$ with I_{LOAD} ranging from 0 to 10 mA is given in Fig. 7. The respective $h\langle 2, 4, 6\rangle$ is annotated. As can be seen, this method effectively prevents $I_A < 0$ and allows a large I_A swing to resist V_{IN} noise. The accuracy should be enhanced by sensing I_A and feeding the sensed information back to control I_r in future works. At light load, the simulated quiescent current of the AP section is 23.5 μA and that of the DI section is 4.2 μA.

B. Working Principles

The working principle of the proposed LDO is illustrated in Fig. 8. It begins with an I_{LOAD} step up at t_1. The fast Loop-1 will respond to the load step, providing most of the momentary I_{OUT} and preventing a significant V_{OUT} undershoot (peaking out at t_2). The I_D will not increase until the next sampling at t_3, where the coarse-tuning drives V_{OUT} back quickly, because of the $\times 16$ control word shifting. After the DI activation, I_A decreases with I_D increasing. When V_{OUT} reaches $V_{\mathrm{REF}-}$ at t_4, the coarse-tuning is changed to the fine-tuning. The $\times 1$ control word shifting regulates V_{OUT} to V_{REF} slowly but accurately. Carry-in operation will take place when l overflows. The I_r and $I_{A,\mathrm{dc}}$ will also increase step by step, according to the current indictor $h\langle 2, 4, 6\rangle$. The LDO reaches a steady state until I_A gets close to $I_{A,\mathrm{dc}}$ at t_5. The DI section will still excite a steady-state LCO, but as discussed, the LCO will be partially compensated by the fast-changing I_A.

When I_{LOAD} steps down at t_6, a V_{OUT} overshoot occurs. The AP section can still respond to the step by providing a negative momentary I_A but mostly from M_{10}. Unlike the undershoot

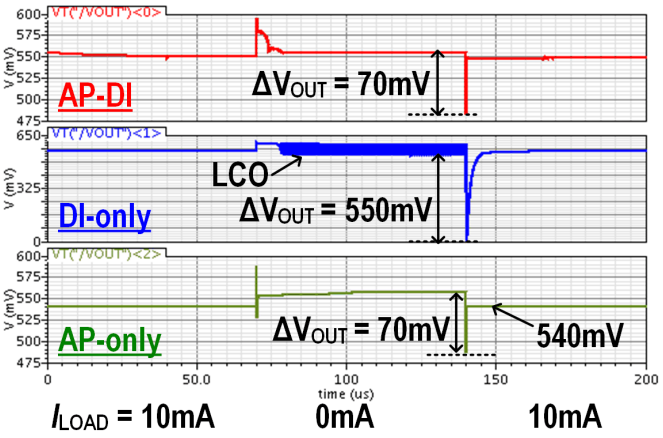
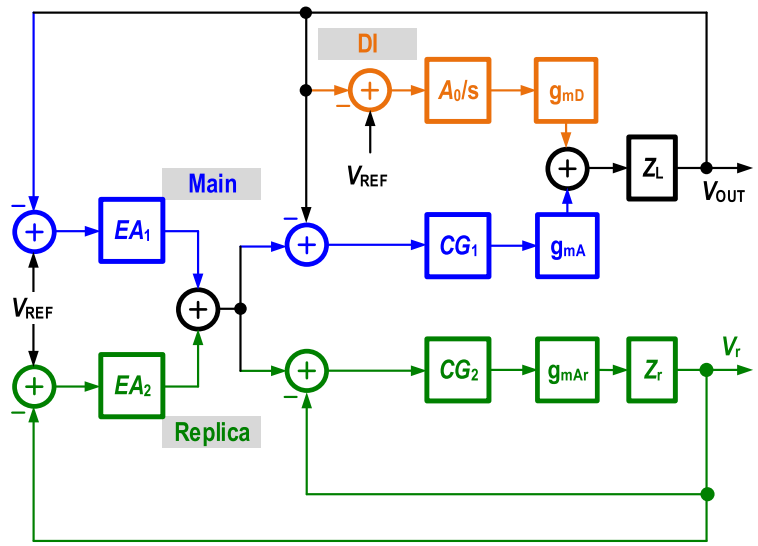


Fig. 9. Simulated V_{OUT} load transient waveforms when I_{LOAD} changes between 0 and 10 mA. $V_{\mathrm{IN}} = 0.6$ V, $V_{\mathrm{REF}} = 0.55$ V, and $f_{\mathrm{CLK}} = 5$ MHz.

case, I_D will also be reduced momentarily, because many DI power transistors are still turned on while their V_{DS} reduces. The coming sampling occurs at t_8, the LDO is first controlled by Loop-4 if $V_{\mathrm{OUT}} > V_{\mathrm{REF}+}$ and then by Loop-5 since t_9. Inverse to the operations between t_3 to t_5, borrow operation occurs, and $I_{A,\mathrm{dc}}$ will also decrease. As discussed, for the very light-load condition, I_{OUT} will be provided by I_A only. V_{OUT} is then forced larger than V_{REF}, disabling the DI section and removing the LCO.

Regarding the recovery time (t_2 to t_3 for undershoot and t_7 to t_9 for overshoot), the overshoot recovery should be longer. It is because I_{LOAD} is zero, M_{10} and the FVF bias current are the only two transistors that can provide pull-down currents for V_{OUT}, which limit the settling time for the heavy-to-light-load transient. The recovery time can be possibly reduced by



$$\begin{cases} EA_1(s) = \dfrac{A_1}{(1+sT_1)(1+sT_{11})} \\ EA_2(s) = \dfrac{A_2}{(1+sT_2)(1+sT_{22})} \end{cases} \quad (6)$$

$$\begin{cases} CG_1(s) = \dfrac{A_3}{1+sT_3} \\ CG_2(s) = \dfrac{A_4}{1+sT_4} \end{cases} \quad (7)$$

$$\begin{cases} Z_L(s) = \dfrac{r_{dsA} \parallel r_{dsD} \parallel R_{LOAD}}{1+sT_{33}} = \dfrac{K_{33}}{1+sT_{33}} \\ Z_r(s) = \dfrac{r_{dsr} \parallel R_r}{1+sT_{44}} = \dfrac{K_{44}}{1+sT_{44}} \end{cases} \quad (8)$$

Fig. 10. Small-signal model of the proposed AP-DI LDO.

the asynchronous techniques, through maximizing the usage of the digital controller [15], [16], [23].

Here, the proposed AP-DI LDO is compared with the DI-only and AP-only LDOs. We define the DI-only LDO to be the conventional coarse-fine-tuning DLDO in [8], consisting of Loop-4 and -5. The AP-only LDO employs the FVF-based ALDO topology in [5], essentially made from Loop-1 and -2. The simulated $V_{\rm OUT}$ waveforms of load transient response are shown in Fig. 9, where $V_{\rm IN} = 0.6$ V, $V_{\rm REF} = 0.55$ V, $f_{\rm CLK} = 5$ MHz, and $I_{\rm LOAD}$ changes between 0 and 10 mA within a 5-ns edge time. At light load, the large LCO in DI-only is removed. Also, the AP-DI undershoot is comparable with that of AP-only but much smaller than DI-only. This simulation verifies the effectiveness of the analysis.

C. Stability

The small-signal model of the AP section is shown in Fig. 10. The EA_1 and EA_2, CG_1 and CG_2, and Z_L and Z_r represent the EA stage, CG stage, and $V_{\rm OUT}$ and V_r impedance of the main loop and replica loop, respectively. $g_{\rm mA}$, $g_{\rm mr}$, and $g_{\rm mD}$ are the transconductances of $M_{\rm PA}$, $M_{\rm Pr}$, and power transistor array of the DI section. The A_0/s term represents the effect of the digital integrator. The transfer functions (6)–(8) can be written as shown in Fig. 10, where A_3 and A_4 are the dc gains of CG stages of the main loop and replica loop, respectively. T_1 and T_2 and T_{11} and T_{22} are the output time constants at the EA second and first stages, respectively, while T_3 and T_4 are the CG output time constants. K_{33} and K_{44} are the resistances at $V_{\rm OUT}$ and V_r, respectively.

The frequency response of this multiple-loop LDO can be conceptually presented in Fig. 11. As discussed in [11], the DI section has two poles, one of which locating at dc cause the slow response (integrator). For the AP section, its bandwidth should be wider. Once AP and DI are connected in parallel, a zero locates near the intersection of the loop gain curves [29]. This zero cancels the dc pole from DI section, and therefore, the LDO stability depends on the AP section.

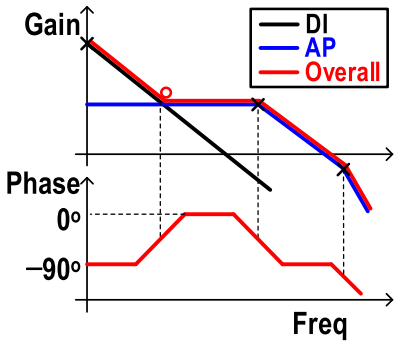


Fig. 11. Conceptual frequency response of the AP-DI LDO.

To check the stability, the three analog loops are simulated first. Their breaking points are shown in Fig. 12. Loop-1 is broken at the EA output, and the ac stimulus is added to the gate of $M_{\rm PA}$. Then, the open-loop transfer function can be written as

$$T_{\rm OL1} = -g_{\rm mA} \cdot Z_L(s) \cdot {\rm CG}_1(s). \quad (9)$$

Hence, the dc gain of Loop-1 is related to the loading conditions.

For Loop-3 and -2, their transfer functions are expressed as

$$\begin{cases} T_{\rm OL2} = \dfrac{{\rm CG}_1(s) \cdot g_{\rm mA} \cdot Z_L(s)}{1 + {\rm CG}_1(s) \cdot g_{\rm mA} \cdot Z_L(s)} \cdot {\rm EA}_1(s) \\ T_{\rm OL3} = \dfrac{{\rm CG}_2(s) \cdot g_{\rm mAr} \cdot Z_r(s)}{1 + {\rm CG}_2(s) \cdot g_{\rm mAr} \cdot Z_r(s)} \cdot {\rm EA}_2(s) \end{cases} \quad (10)$$

Notice that at low frequency, the dc gains of Loop-2 and Loop-3 are approximated to the gains of EA_1 and EA_2 (A_1 and A_2). Therefore, they are insensitive to the loading conditions. To estimate the overall analog loop stability, it is broken at the output of the EA. A variable resistor is used to manually tune $V_{\rm OUT} = V_{\rm REF}$. This emulates the DI section effect in dc, while break it in ac.

Simulated in the TT corner and 27 °C, the Bode plots of these three analog loops are given in Fig. 13. As analyzed, the Loop-1 gain, which is essentially the p-gain for fast response,

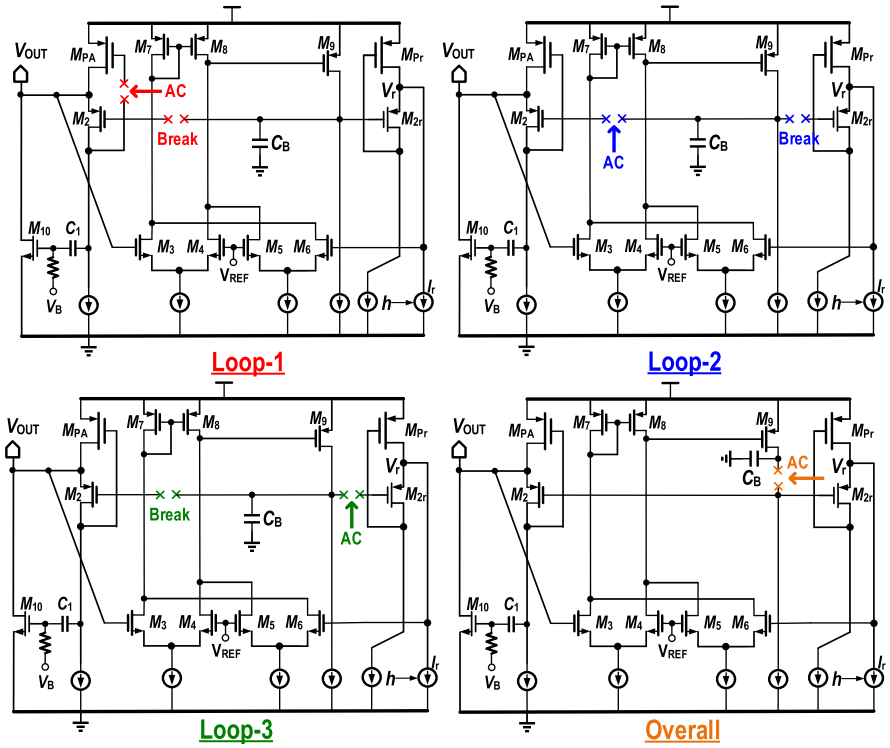


Fig. 12. Breaking point of Loop-1, -2, -3, and overall analog loops, for the stability simulation.

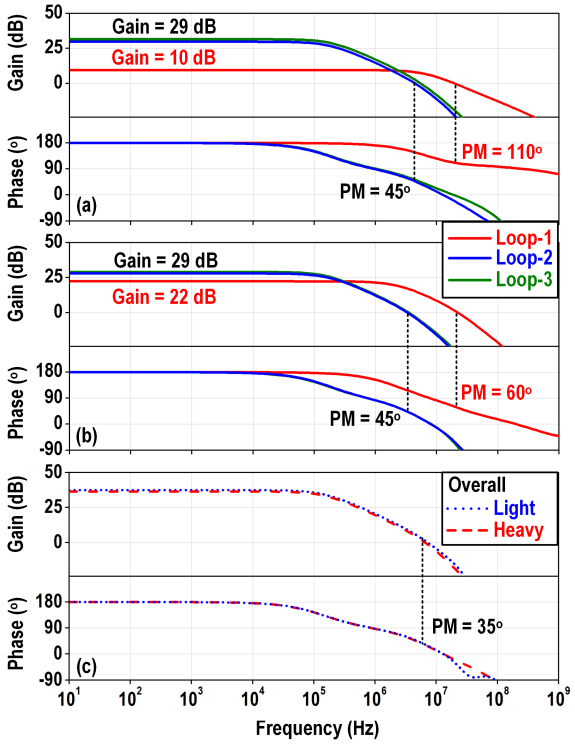


Fig. 13. Bode plots of Loop-1, -2, and -3 at (a) heavy load, $I_{A,dc} = 2$ mA, $I_D = 8$ mA, (b) light load, $I_{A,dc} = 1$ μA, $I_D = 0$, and (c) bode plots of the overall analog loops under heavy and light loads. All cases are with $V_{IN} = 0.6$ V and $V_{OUT} = 0.55$ V.

is 10 and 22 dB at heavy load and light load, respectively. Also, the frequency responses of Loop-2 and -3 are almost the same. The 29-dB Loop-2 gain can provide a soft regulation at very light load. The phase margins of Loop-1, -2, and -3 are 110°, 45°, and 45°, respectively. The worst phase margin of Loop-2 and Loop-3 is 35°, found in the SS corner, 0 °C, $V_{IN} = 0.5$ V. The phase margins of Loop-2 and -3 can be improved by increasing C_B. The overall phase margin is about 35° for both heavy and light loads, as given in Fig. 13(c).

D. PSR

The PSR improvement of this work can be explained from both small-signal and large-signal perspectives.

From the small-signal perspective, the PSR model of the conventional FVF-based ALDO is shown in Fig. 14(a). Its PSR can be expressed as

$$\mathrm{PSR_{ALDO}} \approx \frac{1}{1 + \frac{r_{dsA}}{R_{LOAD}||(1/sC_{OUT})} + \mathrm{EA_1}(s)\mathrm{CG1}(s) r_{dsA} g_{mA}}. \tag{11}$$

For the main loop of the proposed AP-DI LDO as shown in Fig. 14(b), the $\mathrm{PSR_{LOOP1+2}}$ expression is the same as (11) but replacing the r_{dsA} term with $r_{ds} = r_{dsA}||r_{dsD}$. It should be noticed that the PSR here is worse than that of the conventional ALDO. The reason is that the $r_{dsA}||r_{dsD}$ here is smaller than r_{dsA}, but the overall g_m is not increased proportionally, since the g_{mD} can be neglected when the supply ripple frequency f_{ripple} is comparable with f_{CLK}. This phenomenon will be exacerbated at heavy load, because $r_{ds} \cdot g_{mA}$ can be written as

$$\begin{aligned} r_{ds} \cdot g_{mA} &= \frac{V_{dropout}}{I_{LOAD}} \cdot \sqrt{2\mu_{PA} C_{OX} \frac{W}{L} I_A} \\ &= V_{dropout} \cdot \sqrt{\alpha \cdot \frac{2\mu_{PA} C_{OX} \frac{W}{L}}{I_{LOAD}}} \end{aligned} \tag{12}$$

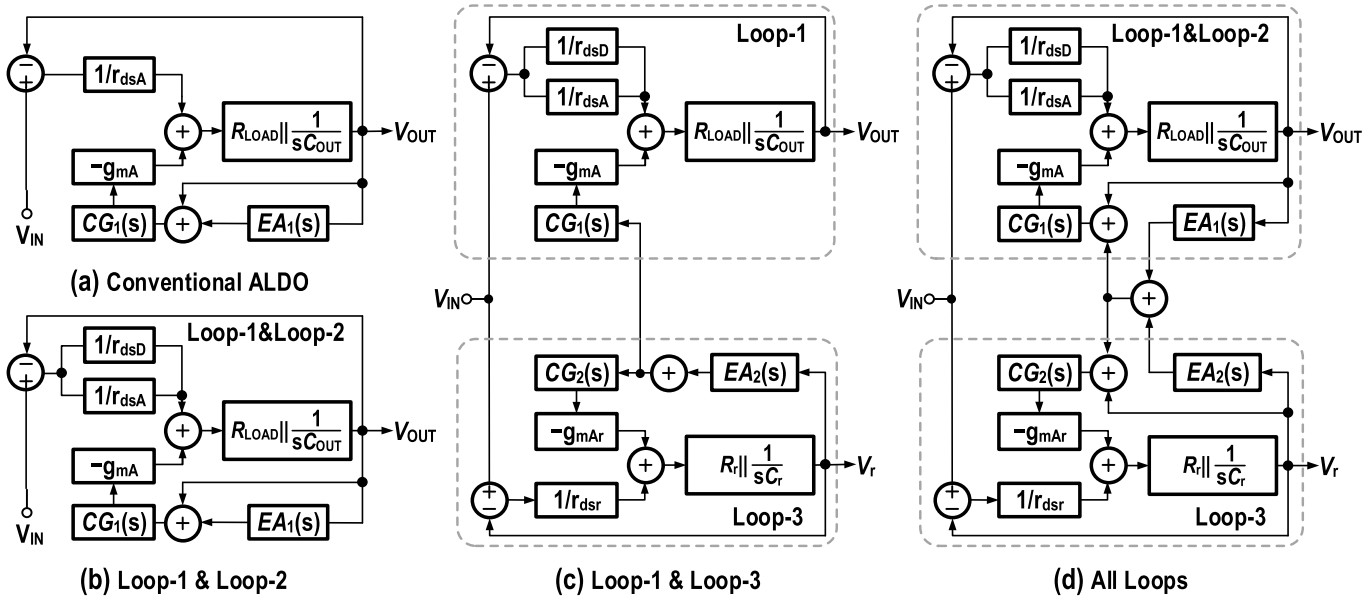


Fig. 14. PSR small-signal model of (a) conventional FVF-based ALDO, (b) AP-DI with Loop-2, (c) AP-DI with Loop-3, and (d) AP-DI with all loops.

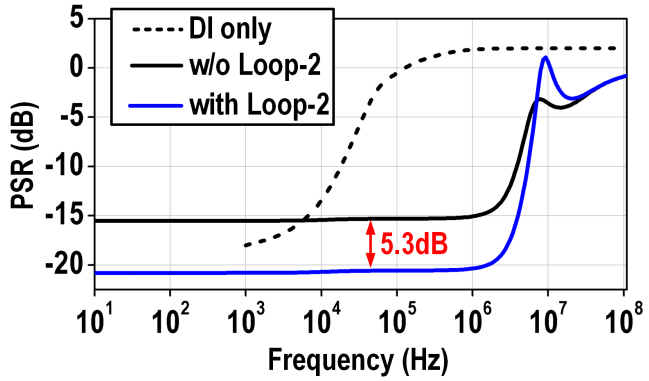


Fig. 15. Simulated PSRs versus frequency for DI only, DI-AP without Loop-2, and DI-AP with Loop-2.

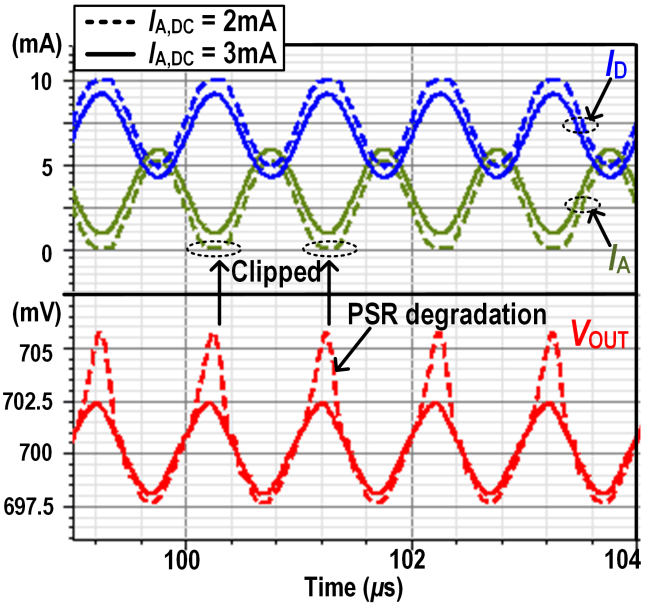


Fig. 16. Simulated I_D, I_A, and V_{OUT} transient waveforms when I_{LOAD} = 10 mA, with $I_{A,dc}$ = 2 and 3 mA.

where μ_{PA} is the hole mobility, and C_{OX} is the gate-oxide unit capacitance. If the I_A/I_{LOAD} ratio α is small at heavy load, $r_{ds} \cdot g_{mA}$ becomes small, and PSR will be degraded.

To mitigate this, we add Loop-3 to control $I_{A,dc}$, making it to adaptively increase when I_{LOAD} increases, maintaining the α value roughly. The PSR small-signal model of the Loop-1 and Loop-3 is included in Fig. 14(c). Also, the derived PSR expression is given in (13), as shown at the bottom of the next page. C_r is the capacitance at V_r node. Comparing (11) and (13), if the replica loop matches the main loop, the $PSR_{LOOP1+3}$ can be close to $PSR_{LOOP1+2}$. However, consider the mismatch, the PSR will be degraded.

In this article, the Loop-2 can be reused to offer about 6-dB improvement for the PSR. The small-signal model of all loops is shown in Fig. 14(d) and the derived expression in (14), as shown at the bottom of the next page. Compared to (13), (14) has the same numerator. However, if matched, the $EA_2(s)\cdot[r_{dsr}\cdot g_{mAr}\cdot CG_2(s) + r_{ds}\cdot g_{mA}\cdot CG_1(s)]$ term in the denominator almost doubles. However, still, the 6-dB improvement can be degraded by the mismatch.

This analysis can be verified by the simulation results shown in Fig. 15, where V_{IN} = 0.75 V, V_{REF} = 0.7 V, and I_{LOAD} = 10 mA. Both the curves of w/o and with Loop-2 are obtained from the ac small-signal simulation with $I_{A,dc}$ = 3 mA, while that of DI-only case is simulated using transient analysis with f_{CLK} = 5 MHz. The amplitude of V_{IN} ripple (V_{ripple}) equals to 40 mV_{PP}. From the results, Loop-2 improves the PSR by 5.3 dB. Also, as predicted, the PSR of DI-only begins to degrade at 10 kHz, which is much lower than f_{CLK}.

From the large-signal perspective, the adaptive changing on $I_{A,dc}$ allows an enlarged I_A swing. This is helpful to

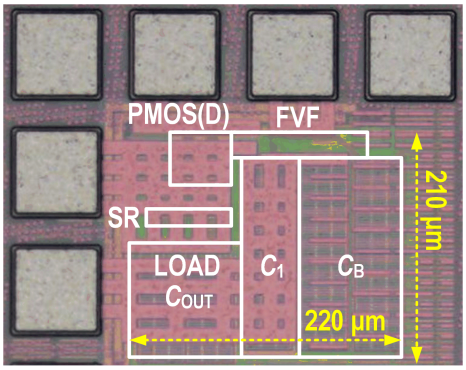


Fig. 17. Chip microphotograph of the proposed LDO.

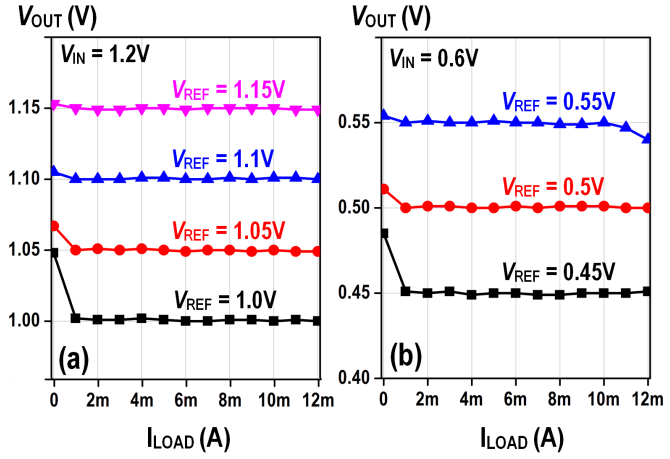


Fig. 18. Measured load regulation for V_{IN} = (a) 1.2 and (b) 0.6 V.

handle the large current ripple caused by the supply noise, as explained in Fig. 16. The simulated transient waveforms of I_A, I_D, and V_{OUT} are shown when I_{LOAD} = 10 mA. I_A can respond with the opposite phase to I_D to maintain a reduced V_{OUT} ripple. If $I_{A,dc}$ is set to 3 mA, the full swing of I_A is allowed, and V_{OUT} ripple can be reduced to 4.5 mV. In contrast, if $I_{A,dc}$ = 2 mA, the I_A is clipped to 0 but expected to swing to an even lower level. When clipped, the LDO is vulnerable to the input noise, hence the V_{OUT} ripple is deteriorated by 3.5 mV (5-dB PSR degradation).

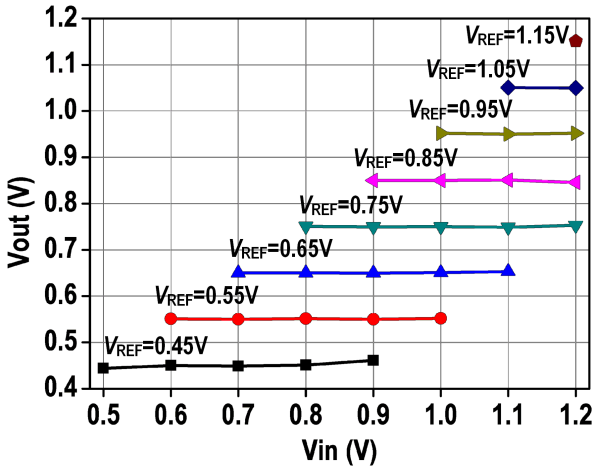


Fig. 19. Measured line regulation for I_{LOAD} = 10 mA.

IV. Measurement Results

The proposed LDO is fabricated in a 65-nm CMOS process. Fig. 17 shows the chip micrograph, with an active area of 0.04 mm^2, including a 20-pF on-chip C_{OUT}, a 13-pF C_1, and a 26-pF C_B. The CLK is externally generated.

One chip was measured at the room temperature. The measured load regulation is presented in Fig. 18, for V_{IN} = 0.6 and 1.2 V. Due to the adaptive I_{A-dc} scheme, a precise regulation can be achieved when I_{LOAD} > 1 mA. The output accuracy becomes degraded at light load, because the AP section takes over the LDO with a relatively low gain. Nevertheless, this helps to remove the light load LCO. The measured line regulation performance for I_{LOAD} = 10 mA is given in Fig. 19.

Fig. 20(a) shows the measured transient response with V_{IN} = 0.6 V, V_{REF} = 0.55 V, f_{CLK} = 5 MHz, when I_{LOAD} changes from 0 to 10 mA within a 5-ns transition edge times (T_{EDGE}). A 64-mV undershoot and a 46-mV overshoot are achieved, which are mainly determined by the Loop-1 and the M_{10}, respectively. For I_{LOAD} = 0, the steady-state V_{OUT} deviates about 8 mV from V_{REF}, but LCO is then removed as predicted. For the 3-to-10-mA I_{LOAD} step shown in Fig. 20(b), the V_{OUT} undershoot is reduced to 44 mV, and V_{OUT} is well regulated to V_{REF} in the steady state, with a 3-mV LCO. The dynamic voltage scaling (DVS) transient waveforms are shown

$$\mathrm{PSR}_{\mathrm{Loop1+3}} \approx \frac{1+\frac{r_{\mathrm{dsr}}}{R_r||(1/sC_r)}+\mathrm{EA}_2(s)[r_{\mathrm{dsr}}\cdot g_{\mathrm{mAr}}\cdot \mathrm{CG}_2(s)-r_{\mathrm{ds}}\cdot g_{\mathrm{mA}}\cdot \mathrm{CG}_1(s)]}{\left[1+\frac{r_{\mathrm{dsr}}}{R_r||(1/sC_r)}+\mathrm{EA}_2(s)\cdot \mathrm{CG}_2(s)\cdot r_{\mathrm{dsr}}\cdot g_{\mathrm{mAr}}\right]\left[1+\frac{r_{\mathrm{ds}}}{R_{\mathrm{LOAD}}||(1/sC_{\mathrm{OUT}})}\right]} \tag{13}$$

$$\begin{aligned}\mathrm{PSR}_{\mathrm{Loop1+2+3}} &\approx \frac{1+\frac{r_{\mathrm{dsr}}}{R_r||(1/sC_r)}+\mathrm{EA}_2(s)[r_{\mathrm{dsr}}\cdot g_{\mathrm{mAr}}\cdot \mathrm{CG}_2(s)-r_{\mathrm{ds}}\cdot g_{\mathrm{mA}}\cdot \mathrm{CG}_1(s)]}{\left[1+\frac{r_{\mathrm{dsr}}}{R_r||(1/sC_r)}+\mathrm{EA}_2(s)\cdot \mathrm{CG}_2(s)\cdot r_{\mathrm{dsr}}\cdot g_{\mathrm{mAr}}\right]\left[1+\frac{r_{\mathrm{ds}}}{R_{\mathrm{LOAD}}||(1/sC_{\mathrm{OUT}})}\right]+\mathrm{EA}_1(s)\cdot \mathrm{CG}_1(s)\cdot r_{\mathrm{ds}}\cdot g_{\mathrm{mA}}\left[1+\frac{r_{\mathrm{dsr}}}{R_r||(1/sC_r)}\right]} \\ &\approx \frac{1+\frac{r_{\mathrm{dsr}}}{R_r||(1/sC_r)}+\mathrm{EA}_2(s)[r_{\mathrm{dsr}}\cdot g_{\mathrm{mAr}}\cdot \mathrm{CG}_2(s)-r_{\mathrm{ds}}\cdot g_{\mathrm{mA}}\cdot \mathrm{CG}_1(s)]}{\left\{1+\frac{r_{\mathrm{dsr}}}{R_r||(1/sC_r)}+\mathrm{EA}_2(s)\cdot[r_{\mathrm{dsr}}\cdot g_{\mathrm{mAr}}\cdot \mathrm{CG}_2(s)+r_{\mathrm{ds}}\cdot g_{\mathrm{mA}}\cdot \mathrm{CG}_1(s)]\right\}\cdot\left[1+\frac{r_{\mathrm{ds}}}{R_{\mathrm{LOAD}}||(1/sC_{\mathrm{OUT}})}\right]}\end{aligned} \tag{14}$$

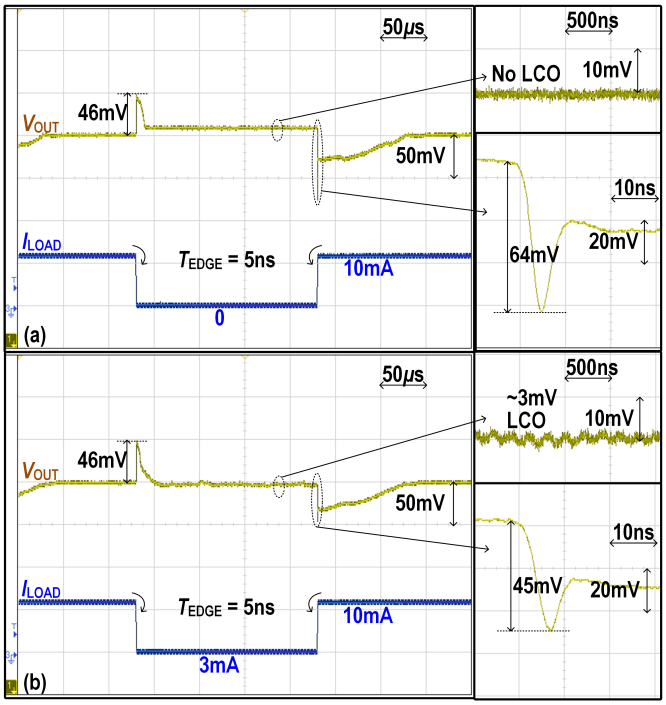


Fig. 20. Measured transient responses with a (a) 0–10- and (b) 3–10-mA I_{LOAD} step, both within a 5-ns T_{EDGE}. $V_{IN} = 0.6$ V, $V_{REF} = 0.55$ V, and $f_{CLK} = 5$ MHz.

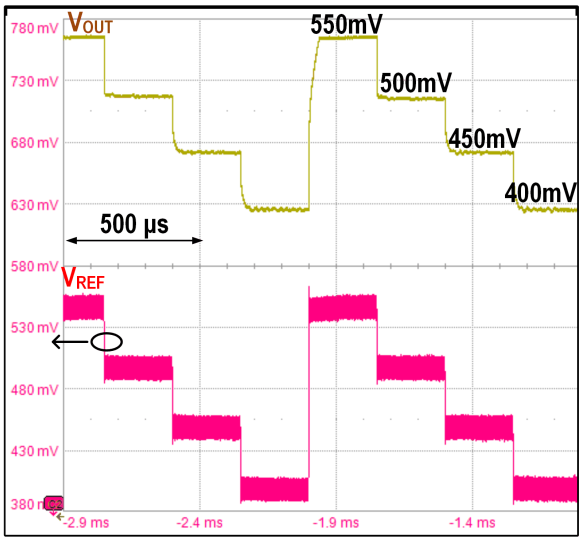


Fig. 21. Measured DVS transient response with $V_{IN} = 0.6$ V, and V_{REF} changes from 550 to 400 mV with a 50 mV/step.

in Fig. 21, where $V_{IN} = 0.6$ V, V_{REF} changes from 550 to 400 mV with a 50 mV/step. As can be seen, V_{OUT} can track the V_{REF} changing.

Figs. 22 and 23 show the measured PSR performances. Two measurement conditions are defined here: (Case-1): $V_{IN} = 0.75$ V, $V_{REF} = 0.7$ V, while (Case-2): $V_{IN} = 0.6$ V, $V_{REF} = 0.5$ V. Both cases are with $f_{CLK} = 5$ MHz and $I_{LOAD} = 10$ mA. Fig. 22(a) for Case-1 shows the measured V_{IN} and V_{OUT} transient waveforms, where a 5-mV_{pp} V_{OUT} ripple is recorded with an input ripple of $f_{ripple} = 1$-MHz

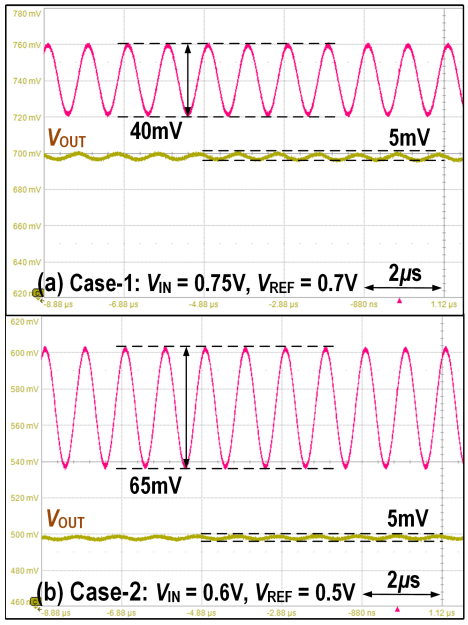


Fig. 22. Measured transient waveforms of V_{IN} and V_{OUT}, with $I_{LOAD} = 10$ mA, $f_{ripple} = 1$ MHz, $f_{CLK} = 5$ MHz when in (a) Case-1 and (b) Case-2.

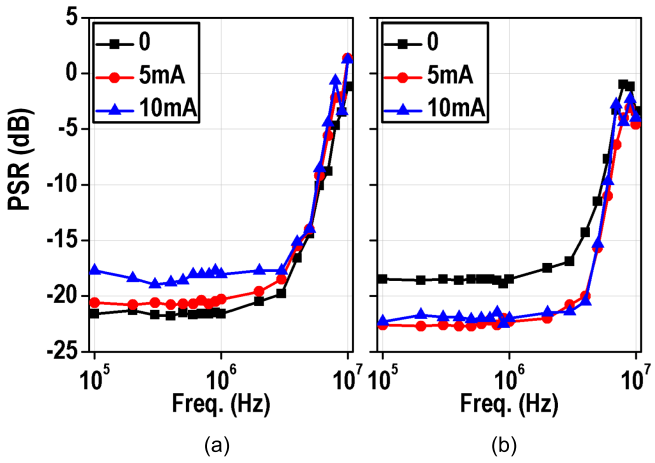


Fig. 23. Measured PSR from 100 kHz to 10 MHz, $f_{CLK} = 5$ MHz, $I_{LOAD} = 0$, 5, 10 mA, for (a) Case-1 and (b) Case-2.

and 40-mV_{pp} amplitude. In Fig. 22(b) for Case-2, the PSR is −22-dB at 1 MHz when the amplitude of input ripple is 65 mV_{pp}. The measured PSR curves versus frequency are given in Fig. 23, under $I_{LOAD} = 0$, 5, and 10 mA. The PSR variation against I_{LOAD} is reduced because I_A can be adaptively increased with I_{LOAD}.

The proposed LDO is compared with the state-of-the-art works in Table I. Thanks to the AP-DI architecture, the proposed LDO is endowed with the fast response feature of an ALDO, together with the high dc gain property of a conventional DLDO. The maximum output current is 10 mA, and the measured quiescent current is 29 μA, hence the calculated maximum current efficiency is 99.71%. Meanwhile, it achieves a 0.37-ps figure-of-merit-1 (FoM1) [31] and

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART WORKS

	[11] Salem, JSSC'18	[19] Huang, ISSCC'17	[20] Nasir, JSSC'18	[21] Ma, ISSCC'18	[22] Kundu, JSSC'19	[23] Liu, ISSCC'19***	[24] Wang, CICC'19	**This work**
Process [nm]	65	65	130	28	65	14	65	**65**
Area [mm^2]	0.0023	0.034	0.08	0.0055	0.037	0.024	0.04	**0.04**
P-path	Digital	RC HPF	Digital	NMOS	Digital	ALDO	D-G couple	**FVF**
I-path	Digital	SR	Analog EA	SR	VCO	Digital	CP	**SR**
V_{IN}[V]	0.5-1	0.5-1	0.6, 1.1-1.2	0.4-0.55	0.6-1.2	1-1.2	0.5-1	**0.5-1.2**
V_{OUT}[V]	0.3-0.45	0.45-0.95	0.5-0.55, 0.8-1.1	0.35-0.5	0.4-1.1	0.7-0.85	0.45-0.95	**0.45-1.15**
Max. f_{CLK} [MHz]	240	10	560	4	>3.9	N.A.	1	**5**
C_{OUT} [pF]	400	0	500	24	40	200	0-10,000	**20**
I_{LOAD} range [mA]	0.01-2	2-20	0.03-12	0.5-20.5	10-100	0.01-530	0.001-105	**0-10******
ΔV_{OUT} [mV] @ ΔI_{LOAD} [mA]	40@1.06	105@10	240@10.3	117@20	108@50	83@15	185@100	**64@10******
PSR enhanced by	N.A.	N.A.	Analog gain	N.A.	N.A.	Analog gain Feedforward	N.A.	**Analog gain Replica loop**
1MHz PSR [dB] @ $V_{IN}/V_{dropout}$ [V] @V_{ripple} [V_{pp}]	N.A.	N.A.	−12 @1.2/0.4 @N.A.	N.A.	−35 @1/0.2 @N.A.	−18 (1LDO) @N.A.@N.A. −42 (8LDO) @N.A.@N.A.	N.A.	**−18 @ 0.75/0.05@0.04 −22 @ 0.6/0.1@0.065**
I_Q [μA]	14	3.2	26	0.81	10-1070	4.35-27.4	4.9	**29******
Max. Current efficiency (%)	99.8	99.97	98.6	99.99	99.5	99.97	99.99	**99.71******
FoM1 [ps]*	199	0.23	166	0.0057	0.47	1.38	0.0038	**0.37******
Edge time ratio K	5	5	1	15	4000	2.5	5	**25**
FoM2 [V]**	0.0026	0.00015	0.0006	0.00007	9.2	0.00035	4.50E-05	**0.0044******

*FoM1 = $C_{OUT}\cdot\Delta V_{OUT}\cdot I_Q/I_{OUT}^2$ [30]. **FoM2=$K\cdot\Delta V_{OUT}\cdot I_Q/\Delta I_{OUT}$ [31]. ***High PSRR mode. ****V_{IN} = 0.6V, V_{REF} = 0.55V.

0.0044-V FoM2 [32], which are comparable or better than the state-of-the-art works.

In addition, this article achieves a moderate PSR performance. Due to the moderate analog loop gain and about 6-dB PSR improvement from Loop-2, this article improves PSR with a larger V_{ripple} at a low V_{IN} and low $V_{dropout}$, compared with the hybrid LDOs in [20] and [23]. Also, the PSR can be further improved by allocating the load current to more ALDO tiles as in [23].

Finally, this article reaches $I_{LOAD,min} = 0$ without LCO. To extend the $I_{LOAD,max}$, the proportional part should be designed with higher gain and faster response, which will help to reduce the V_{OUT} spike under a larger ΔI_{LOAD} step.

V. CONCLUSION

This article analyses the reasons for slow transient response, bad PSR, and large LCO in a conventional DLDO. These issues are addressed through the AP control in the proposed AP-DI LDO. The feature of high output accuracy in a conventional DLDO is maintained by the DI section. The AP part, implemented with an FVF, responds fast to the load step. A replica loop is added to adaptively define the AP output current, resulting in a moderate PSR performance. To reduce the LCO and extend the $I_{LOAD,min}$ limit to zero, the AP will output all the I_{LOAD} at a very light load. An EA with moderate gain is not only helpful for a light-load regulation but also enhances the PSR by about 6 dB. The measurement results verify the effectiveness of the proposed scheme.

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