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# An Intermittent Frequency Synthesizer With Accurate Frequency Detection for Fast Duty-Cycled Receivers

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**ABSTRACT** An intermittent frequency synthesizer for fast duty-cycled receivers is presented in this paper. Different from state-of-art techniques which try to eliminate the initial phase error that degrades the intermittent frequency detection, a new frequency detector is proposed to maintain an accurate frequency detection regardless of the initial phase error. Moreover, an averaged fraction division scheme (AFDS) is integrated in the synthesizer to improve the frequency resolution. The frequency synthesizer is implemented and verified by using discrete devices and an FPGA. The measurement results show that the frequency detector provides a frequency detection accuracy of 0.88%, and the synthesizer achieves a frequency resolution of 0.625 MHz when controlled by a duty-cycled signal with a 6-$\mu$s period and a 2-$\mu$s time duration. The frequency synthesizer can perform an intermittent frequency hopping from 160MHz to 140MHz while requiring a period of 430 $\mu$s without disturbing the VCO's oscillation.

**INDEX TERMS** Duty cycle, frequency detector, frequency synthesizer, initial phase error, phase-locked loop.

## I. INTRODUCTION

Duty cycle scheme (DCS) is universally used to save power consumption in an electronic and electrical system. Especially in low-power radio-frequency wireless communication applications, the energy is mainly consumed by the receiver monitoring the channel, while DCS can decrease the receiver's average power consumption by operating its power-hungry components intermittently. Fig. 1 illustrates the power consumption of a duty-cycled receiver. As shown, the receiver's mean power consumption can be calculated by:

$$P_{mean} = \frac{1}{T_C}\left[P_{sp}t_{sp} + P_{on}t_{on} + P_{off}t_{off}\right] \quad (1)$$

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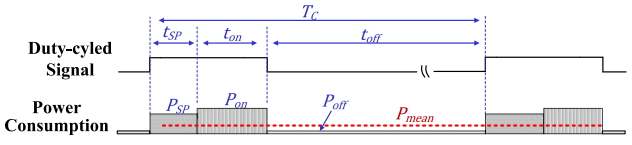


**FIGURE 1.** The power consumption of the duty-cycled receiver.

where $t_{on}$, $t_{off}$ and $t_{sp}$ are the operating duration, the inactive duration and the start-up duration respectively, $P_{on}$, $P_{off}$ and $P_{sp}$ are the power consumptions during the corresponding duration, while $T_C$ is the cycle period equal to $(t_{on} + t_{off} + t_{sp})$. For most receivers, $P_{sp}$ is at the same level of $P_{on}$ and several orders of magnitude larger than $P_{off}$. It means that $t_{sp}$ is critical to DCS. For a large $t_{sp}$,

a considerably long $T_C$ is necessary to keep $P_{mean}$ under an acceptable low level, however, will result in a significant communication latency. Unfortunately, $t_{sp}$ of most mainstream superheterodyne receivers can hardly meet DCS's requirement to fulfill low power consumption and low latency simultaneously [1].

For most of superheterodyne receivers, $t_{sp}$ mainly stems from the locking time of the phase-locked loop (PLL) in frequency synthesizer. For the sake of frequency resolution and noise characteristic, it is hard for the PLLs including those integrated with advanced fast locking techniques to achieve a locking time less than 10 $\mu$s while maintain a relatively low power consumption (less than 1mW) simultaneously [2]–[5]. In other words, it is challenging for a conventional PLL-based superheterodyne receiver to have a fast ($T_C < 100\ \mu$s) and deep (<10%) duty cycle scheme. To reduce or even eliminate $t_{sp}$, some receivers replace the superheterodyne architecture with the RF-envelop-detection techniques [6], [7]. Some opt for the uncertain-IF architecture using open-loop-controlled oscillators [8], [9]. However, those techniques suffer from process, voltage and temperature (PVT) susceptibility, sensitivity degradation and inferior channel selectivity compared to superheterodyne architecture.

Some designs resort to intermittent frequency synthesizers in which the PLL periodically conducts frequency/phase detection and adjustment during the DCS power-on period, preserves its state (the control voltage of voltage controlled oscillator or the control words of digital controlled oscillator in PLL) in the power-off period, and continues the frequency calibration based on the preserved state in next power-on period [10]–[13]. The initial phase error is identified as the main factor causing degradation to the performance of intermittent PLLs. In [10], the initial phase error is reduced by setting, at the start of the power-on period, the PLL's frequency divider with a specific division factor and then continuing with the normal division factor. However, it is challenging to calculate precisely the required start-up division factor. [12] and [13] used an initial phase error reduction circuit and an asynchronous trigger respectively to eliminate the initial phase error by synchronizing the PLL's feedback clock with the reference clock at the start of power-on period; nevertheless, both techniques depend on accurate delay circuits.

In this paper, we propose an intermittent frequency synthesizer with an accurate frequency detector for the fast duty-cycled receiver. The novel frequency detector can achieve a high frequency detection accuracy, regardless of the initial phase error. Moreover, an averaged fractional division scheme (AFDS) is devised to improve the frequency resolution. The proposed frequency synthesizer is implemented using discrete devices and an FPGA to make it applicable to mainstream available receivers.

The remainder of the paper is organized as follows: In Section II, the new frequency detector is analyzed. Section III describes the implement of the intermittent frequency synthesizer and the principle of AFDS. Section IV presents the experimental results and section V concludes the paper.

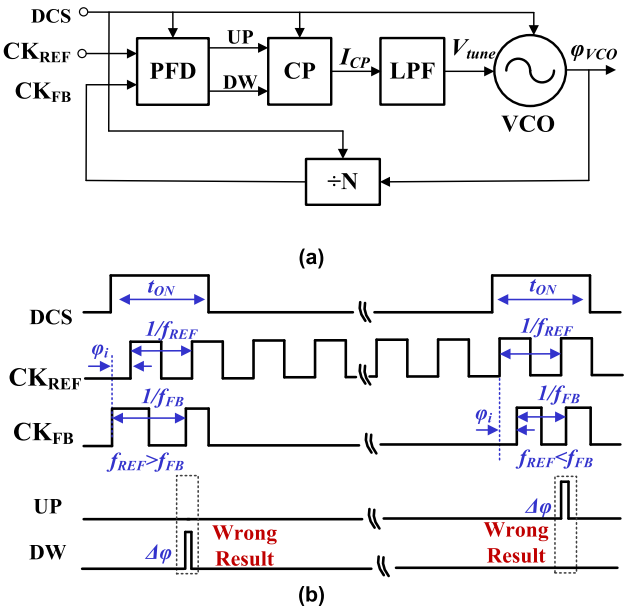


**FIGURE 2.** (a) the conventional PLL-based frequency synthesizer under DCS, (b) the timing diagram when it fails on the phase detecting due to the initial phase error.

## II. THE PROPOSED FREQUENCY DETECTOR

PLL is the most commonly used method to implement a frequency synthesizer and generate a stable and pure high-frequency signal in a superheterodyne receiver, however, its operations in a fast duty cycle scheme remains challenging. Fig. 2(a) shows the schematic of a conventional PLL under the control of a duty cycle signal (DCS). When DCS is active, the PLL detects the phase error between the phase $\varphi_{REF}$ of the reference input $\mathrm{CK_{REF}}$, and the phase $\varphi_{FB}$ of the feedback signal $\mathrm{CK_{FB}}$ generated from the voltage-controlled oscillator's (VCO) output phase $\varphi_{VCO}$, and then converts this phase error into a controlling voltage $V_{tune}$ to adjust VCO's frequency to be the desired one. When DCS turns off, all circuits are quenched to save power. Fig. 2 (b) shows the behavior of a PLL working in a fast duty-cycle mode which means the cycle period and its duty duration are very short. When the PLL is enabled by DCS, $\mathrm{CK_{REF}}$ and $\mathrm{CK_{FB}}$ are not synchronized and have an initial phase error $\varphi_i$ which impedes the frequency error detection between $\mathrm{CK_{REF}}$ and $\mathrm{CK_{FB}}$ correctly in a short time ($t_{on}$). The detected phase error $\Delta\varphi$ can be expressed as:

$$\begin{aligned}\Delta\varphi &= (\varphi_{REF} - \varphi_{FB}) + \varphi_i \\ &= \int_0^{t_{PD}} 2\pi\,(f_{REF} - f_{FB})\,dt + \varphi_i \end{aligned} \tag{2}$$

where $f_{REF}$ and $f_{FB}$ are the frequencies of $\mathrm{CK_{REF}}$ and $\mathrm{CK_{FB}}$ respectively, $t_{PD}$ is the available phase detection time which cannot exceed $t_{on}$ of the DCS. As shown in Fig. 2(b), $\varphi_i$ can degrade the phase detecting accuracy, or even cause wrong results if $(f_{REF} - f_{FB})$ or $t_{PD}$ are insufficient to offset an opposite value of $\varphi_i$. As a result, the final absolute value of

($f_{REF} - f_{FB}$) will be considerably large to compensate for the random $\varphi_i$ when the PLL settles down.

To improve the immunity to the initial phase error, a new frequency detector is presented in this paper to detect the frequency difference. Similar with the time registers used in [14] and [15], the proposed detector can directly convert the input clocks time difference into charges stored on two identical capacitors, and then detect the difference by discharging simultaneously the capacitors.

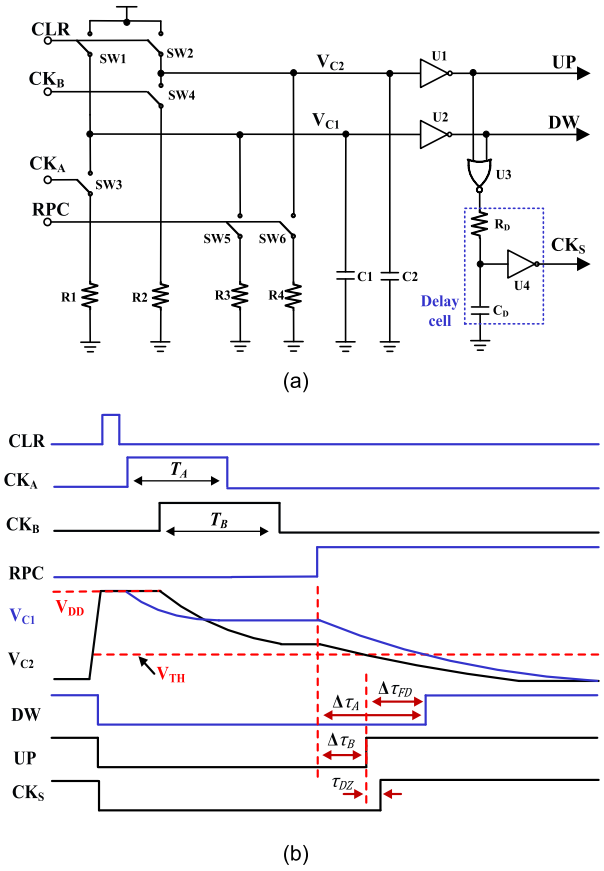


**FIGURE 3. (a). The schematic of the novel frequency detector, (b). Its timing diagram.**

Fig. 3 presents the schematic of the proposed frequency detector and its timing diagram. As shown in Fig. 3(a), the frequency detector is composed of switches SW1∼SW6, resistors R1∼R4, identical capacitors C1 and C2, inverters, a 2-NOR gate, and a delay cell. The circuit is controlled by a clearing signal CLR, two input clocks $CK_A$ and $CK_B$, and a synchronizing signal RPC. Combing with its timing diagram in Fig. 3(b), the operating principle is described below: prior to the presence of the positive pulses on $CK_A$ and $CK_B$, the switches SW1 and SW2 are turned on by CLR to charge the capacitors C1 and C2, and reset their voltages $V_{C1}$ and $V_{C2}$ to the supply voltage $V_{DD}$, and hence turns the outputs DW and UP low. When, positive pulses on $CK_A$ and $CK_B$ occur, C1 and C2 are discharged through R1 and R2 independently, and their voltages $V_{C1}$ and $V_{C2}$ drop proportionally. Afterwards, RPC turns high to discharge C1 and C2 at the same time through R3 and R4 respectively. The voltages $V_{C1}$ and $V_{C2}$ continue downward until crossing the threshold voltage $V_{TH}$ of the inverters U1 and U2, which trigger - DW and UP high. The time intervals $\Delta\tau_A$ and $\Delta\tau_B$, from the rising edge of RPC to the edges of DW and UP respectively, can be calculated as:

$$\begin{cases} \Delta\tau_A = R_3 C_1 ln\left(\dfrac{V_{DD}}{V_{TH}}\right) - \dfrac{R_3}{R_1} T_A \\ \Delta\tau_B = R_4 C_2 ln\left(\dfrac{V_{DD}}{V_{TH}}\right) - \dfrac{R_4}{R_2} T_B \end{cases} \tag{3}$$

where $T_A$ and $T_B$ are the pulse durations of $CK_A$ and $CK_B$ respectively.

It is definite that by setting $T_A$ and $T_B$ equal to the periods of $CK_{REF}$ and $CK_{FB}$ in the PLL which can be denoted by $1/f_{REF}$ and $1/f_{FB}$ respectively, the time difference between $\Delta\tau_A$ and $\Delta\tau_B$ can represent the frequency error between $CK_{REF}$ and $CK_{FB}$. Assuming that $R_3 = R_4$, $R_1 = R_2$, and $C_1 = C_2$, the time difference can be expressed as:

$$\Delta\tau_{FD} = \Delta\tau_A - \Delta\tau_B = \frac{R_3}{R_1}\frac{f_{REF} - f_{FB}}{f_{REF} f_{FB}} \tag{4}$$

As implied by (4), $\Delta\tau_{FD}$ is independent of the initial phase error.

In the proposed frequency detector, DW and UP are combined by an NOR gate, and the output is delayed by $\tau_{DZ}$ through a delay cell to create a sampling clock $CK_S$ used to sample DW and UP.By sampling with $CK_S$, UP is high and DW is low indicates that $f_{REF} > f_{FB}$, UP is low and DW is high means $f_{REF} < f_{FB}$, while both high means that $f_{FB}$ is very close to $f_{REF}$.

The delay $\tau_{DZ}$ behaves as a dead zone of frequency detection, which means the frequency detector is unable to detect the frequency error when $|\Delta\tau_{FD}| < \tau_{DZ}$. It is important to maintain a precise and stable $\tau_{DZ}$, and this can be achieved by using a master-slaver automatic pulse tuning circuit [16].

## III. THE INTERMITTENT FREQUENCY SYNTHESIZER

### A. SCHEMATIC AND OPERTATING PRINCIPLE

Fig. 4 illustrates the schematic of the intermittent frequency synthesizer which includes a common-base Colpitts-type VCO, a high-speed divider (HSD), the proposed frequency detector (FD), a digital-to-analog converter (DAC, MCP4921), two low-speed dividers (LSD), two one-shot pulse generators (OS-PG), a up/down counter (UDC), a serial peripheral interface (SPI), and a digital controller. The VCO, HSD,and FD are implemented with discrete devices while the other blocks are integrated in a FPGA. The VCO is designed to oscillate around 160MHz with a varactor (SMV1253) for frequency tuning, and a quenching switch (SW7). The HSD consists of a prescaler (MC12093), a NAND gate-based buffer, and a DFF-based divider to scale down the VCO's frequency to the FPGA's operating frequency range.

Fig. 5 (a) shows the timing diagram of the synthesizer's signals when it conducts a basic frequency calibration. the

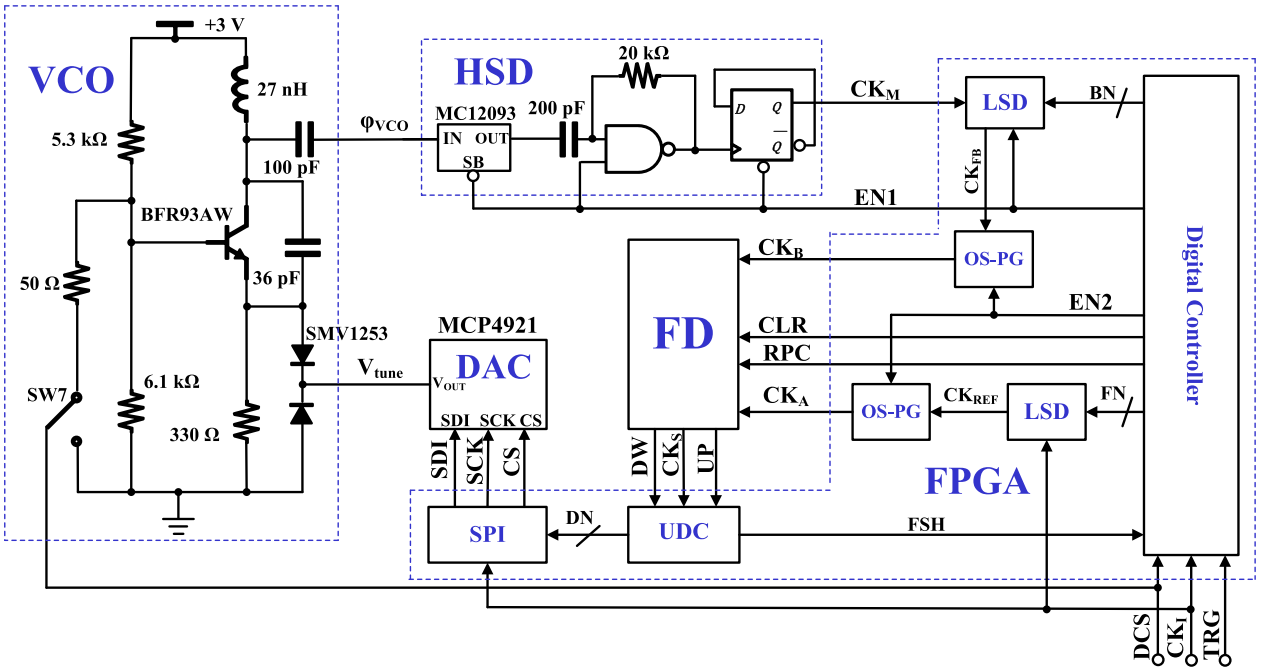


**FIGURE 4.** The schematic of the proposed frequency synthesizer.

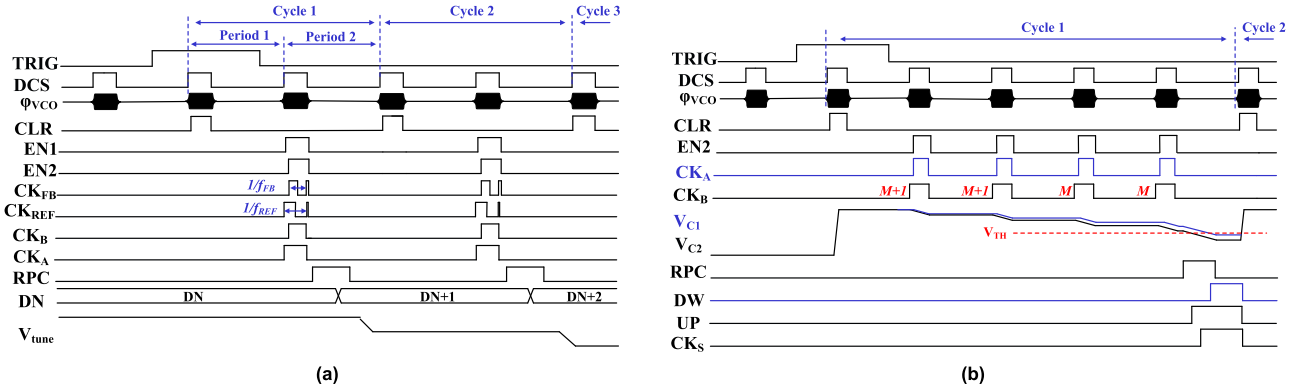


**FIGURE 5.** The timing diagrams of the main signals in the proposed synthesizer. (a). When a basic frequency calibration is conducted. (b). When AFDS ($N = 4$) is applied.

operation principle can be described as follows: the VCO is controlled by the duty cycle signal (DCS) to oscillate on and off. When the digital controller receives a pulse on the triggering signal TRIG, the frequency calibration starts. As shown, the frequency calibration operates on a cycle by cycle basis, where each cycle includes two successive periods of DCS. During the first period, the digital controller outputs a pulse on CLR to reset the frequency detector. In the second period, the controller sets the enable signal EN1 high to activate HSD and LSDs. Therefore, VCO's output $\varphi_{VCO}$ is divided by the combination of HSD and LSD to generate the feedback clock $CK_{FB}$. At the same time, the reference clock $CK_{REF}$ is generated from the global clock $CK_I$ by another LSD. Then, $CK_{REF}$ and $CK_{FB}$ are fed to the corresponding OS-PG to generate two one-shot pulses on FD's inputs $CK_A$ and $CK_B$ with pulse widths equal to $1/f_{REF}$ and $1/f_{FB}$ respectively when the control signal EN2 becomes positive. To avoid degradation in the frequency detection accuracy, caused by the instabilities of the VCO and the HSD during their settling [12], EN2 should lag behind EN1 by a sufficient amount of time (about 300ns in this design). Following these two one-shot pulses on $CK_A$ and $CK_B$, RPC turns high for an sufficient long period to give rise to the frequency detection results UP and DW along with the sampling clock $CK_S$ as described in Fig. 3(b). According to UP and DW, UDC, controlled by $CK_S$, updates its output DN which is sent to the DAC through an SPI to adjust the VCO's tuning voltage $V_{tune}$. If UP is high and DW is low, $V_{tune}$ increases, so does the VCO's oscillating frequency $f_{VCO}$, while UP is low and DW is high, $V_{tune}$ and $f_{VCO}$ decrease. UDC also outputs a signal FSH to indicate

the status of the frequency calibration. When UP and DW are both high, FSH holds a high level to indicate the end of calibration, and the controller ceases operation. Otherwise, the controller will start a next cycle to continue the frequency calibration.

Assuming HSD's with a division factor of $P$ and LSD's with a division factor of $m$. The pulse width of $CK_B$ can be calculated by:

$$T_B = m \cdot P \cdot T_{VCO} \tag{5}$$

where $T_{VCO}$ is the period of $\varphi_{VCO}$. Meanwhile, $CK_A$ has a pulse width of $T_A$ equal to $1/f_{REF}$. At the end of calibration, $T_B$ becomes equal to $T_A$, therefore, the VCO's oscillating frequency can be written as:

$$f_{VCO} \approx m \cdot P \cdot f_{REF} \tag{6}$$

The HSD is useful to reduce the power consumption of the entire loop divider (HSD and LSD), therefore, $P$ is generally constant and larger than 1 (As a demonstration, HSD in this design is mainly used to scale down the VCO's frequency to match the FPGA operating frequency). Hence, $f_{VCO}$ can be modified by changing the factor $m$, and the synthesizer's frequency resolution can be expressed as:

$$\Delta f_{VCO} = P f_{REF} \tag{7}$$

In low-power wireless transceiver, a fast and heavy-duty cycle, required to reduce power budget and restrain latency,, and consequently results in a high $f_{REF}$ and hence a coarse the frequency resolution which hardly meets the requirement of most duty-cycled wireless transceivers.

### B. THE AVERAGED FRACTION DIVISION SCHEME

To improve the frequency resolution, an averaged fraction division scheme (AFDS) is proposed. Fig. 5(b) depicts the timing diagram of signals when AFDS is applied. In contrast with the basic frequency calibration in Fig. 5(a), each cycle in AFDS is extended to include several successive periods of DCS. For $(N+1)$ DCS periods, aside from the first period used to reset the frequency detector, the circuit works intermittently to generate $N$ pairs of pulses on $CK_A$ and $CK_B$ in the remaining $N$ periods. The pulses drive the FD to discharge the capacitors $C_1$ and $C_2$ accordingly. As the figure shows, even if the differences between each pair of $T_A$ and $T_B$ is small, they will be stored and accumulated by FD, and the accumulation will become large enough to detect. Moreover, given that LSD's division factor is set to $(M+1)$ for $n$ times and $M$ for $(N-n)$ times within $N$ periods, according to (3) and (4), the final result can be expressed as:

$$\begin{aligned}\Delta\tau_{total} &= \sum_{i=1}^{N} \Delta\tau_{FD,i} = \frac{R_3}{R_1}\left(\sum_{i=1}^{N} T_{B,i} - NT_A\right) \\ &= \frac{R_3}{R_1} N\left[MPT_{VCO} + \frac{n}{N}PT_{VCO} - T_A\right]\end{aligned} \tag{8}$$

Therefore, when the frequency calibration settles, the calibrated VCO's frequency will be:

$$f_{VCO} \approx \left(MP + \frac{P}{N}n\right) f_{REF} \tag{9}$$

And the frequency resolution can be expressed as:

$$\Delta f_{VCO} = \frac{P}{N} f_{REF} \tag{10}$$

Compared with (7), (10) indicates that the frequency resolution has been improved by a factor of $N$.

## IV. MEASUREMENT RESULTS

For performance demonstration, we implemented the intermittent frequency synthesizer with discrete devices and an FPGA. As shown in Fig. 6(a), the frequency detector, HSD, VCO, and DAC are implemented on the PCB board by using discrete devices or chips, while the other circuits are integrated in a FPGA. Fig. 6(b) is the photo of the actual measurement setup. In the measurement, the period of the duty cycle is set to $6\mu s$ with a duty duration of $2\mu s$ ($t_{on}$). In the FD, R1∼R4 is set to 16.8 kΩ, and C1∼ C2 is 1 nF. The reference frequency $f_{REF}$ is set 0.625 MHz which is derived from the 10 MHz global clock $CK_I$, therefore, the pulse width $T_A$ of the reference $CK_A$ is $1.6\mu s$ which is shorter than $t_{on}$.

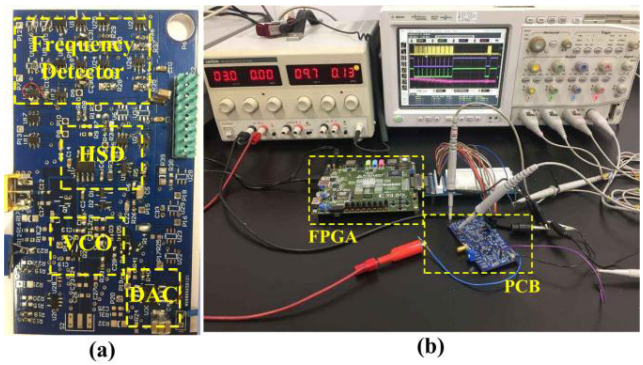


**FIGURE 6.** The photos of the PCB board photo(a), and the measurement setup.

Fig. 7 shows the measurements of FD when the feedback pulse duration $T_B$ is equal to $T_A$. As shown, the rising edges on FD's outputs UP and DW occur almost at the same time, and the sampling clock $CK_S$ lags by about14 ns. Combining with equation (4), the frequency error discriminating accuracy of FD can be calculated as:

$$\frac{\Delta f}{f_{REF}} = \frac{f_{REF} - f_{FB}}{f_{REF}} \approx f_{REF}\,\Delta\tau_D = 0.88\% \tag{11}$$

Fig. 8 shows the measurement of FD when AFDS is enabled. $T_B$ is set to less than $T_A$ in Fig. 8(a) while is greater than $T_A$ in Fig. 8(b). As shown, in the first periods, the difference between the voltages $V_{C1}$ and $V_{C2}$ is small. Thanks to the difference accumulation, the gap between them becomes more and more perceivable. At the ends of detection cycle, $V_{C1}$ is considerately lower/higher than $V_{C2}$ in Fig. 8(a) and

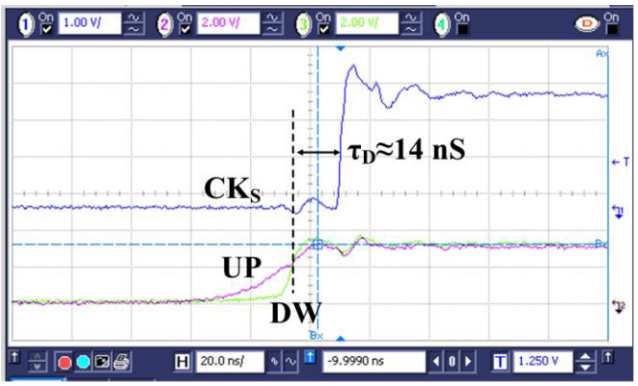


**FIGURE 7.** The measurement of FD when $T_A$=$T_B$.

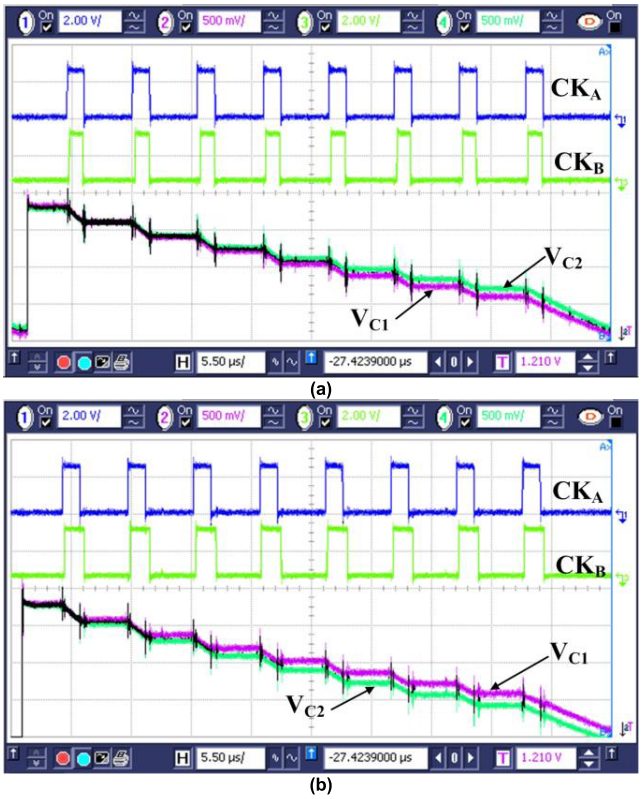


**FIGURE 8.** The measurement of FD when AFDS was enabled. (a) when $T_A$>$T_B$, and (b) when $T_A$<$T_B$.

in Fig. 8(b) respectively. The measured results coincided well with the theoretical analysis.

To demonstrate the performance of the proposed frequency synthesizer, the VCO was set to oscillate around 160MHz, HSD's division factor $P$ was set to 8 same as the number of DCS's periods in each cycle of AFDS ($N$= 8). Fig. 9 shows the measurement of the synthesizer's frequency hopping. In the measurement, LSD's division factor $m$ was changed from 256 to 224, and a pulse was generated on TRIG, to trigger the synthesizer switching its frequency from 160MHz to 140MHz. The frequency synthesizer requires 8 AFDS cycles of about 430 $\mu$s to settle down. After frequency hopping

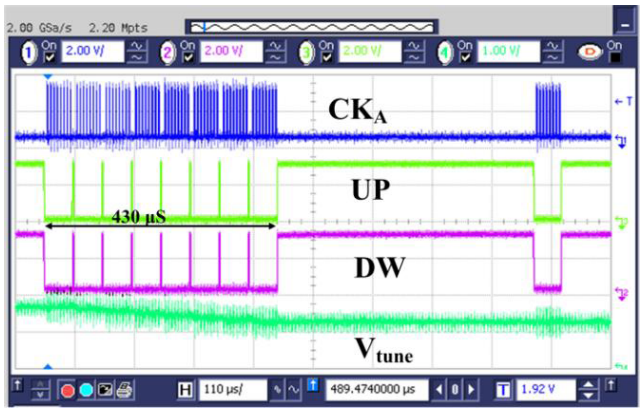


**FIGURE 9.** The measurement of the settling process of synthesizer's frequency hopping.

**TABLE 1.** Performance sumamary and comparision.

| | [8] | [12]* | [13] | This work |
|---|---|---|---|---|
| Type | Open loop | PLL | PLL | FLL |
| $f_{VCO}$ (GHz) | 1.9 | 2.4 | 0.4 | **0.16** |
| Cycle (µS) | - - | 1.25 | 0.17 | **6** |
| Duty Cycle | 100% | 24% | 10% | **33%** |
| Resolution (MHz) | 62 | 10 | -- | **0.625** |
| Accuracy (%) | 2.5% | -- | <3% | **0.88%** |

* Simulated results.

finished, the synthesizer was triggered again without altering the division factor. The circuit required only one AFDS cycle where the frequencies were matched, so that the frequency calibration is concluded.

Table 1 compares the proposed design with the state-of-art intermittent PLL designs. Compared with other designs, the proposed frequency synthesizer can achieve a better resolution and higher frequency accuracy. Considering that in the proposed design we had to use HSD to scale down VCO's oscillating frequency to match the FPGA operating frequency while other design did not have this constraint, the resolution can be substantially improved more under the same conditions.

## V. CONCLUSION

An intermittent frequency synthesizer suitable for the fast duty-cycled receiver is presented in this paper, wherein a new frequency detector is proposed to offer accurate frequency detection for the intermittent frequency calibration. Moreover, an averaged fraction division scheme is devised to improve synthesizer's frequency resolution. The proposed frequency synthesizer is implemented using discrete devices and a FPGA to make it applicable to mainstream available receivers. The measurement results coincide well with the analysis.

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