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Wide Input Range Supply Voltage Tolerant Capacitive Sensor Readout Using On-Chip Solar Cell

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In this paper, a wide input range supply voltage tolerant capacitive sensor readout circuit using on-chip solar cell is presented. Based on capacitance controlled oscillators (CCOs) for ultra-low voltage/power consumption, the sensor readout circuit is directly powered by the on-chip solar cell to improve the overall system energy efficiency. An extended sensing range with high sensing accuracy is achieved using a two-step successive approximation register (SAR) and delta-sigma ($\Delta\Sigma$) analog-to-digital (A/D) conversion (ADC) scheme. Digital controls are generated on-chip using a customized sub-threshold digital standard cell library. Systematic error analysis and optimization including the finite switch on-resistance, buffer input-dependent delay, and SAR quantization nonlinearity are also outlined. High power supply rejection ratio (PSRR) is ensured by using a pseudo-differential topology with ratiometric readout. The complete sensing system is implemented using a standard 0.18 μm complementary metal-oxide-semiconductor (CMOS) process. Simulation results show that the readout circuit achieves a wide input range from 1.5 pF to 6.5 pF with a worst case PSRR of 0.5% from 0.3 V to 0.42 V (0.67% from 0.3 V to 0.6 V). With a 3.5 pF input capacitance and a 0.3 V supply, the $\Delta\Sigma$ stage achieves a resolution of 7.1-bit (corresponding to a capacitance of 2.2 fF/LSB) with a conversion frequency of 371 Hz. With an average power consumption of 40 nW and a sampling frequency of 47.5 kHz, a figure-of-merit (FoM) of 0.78 pJ/conv-step is achieved.

Keywords: On-chip solar cell; capacitive sensor readout; ultra-low voltage; ultra-low power; two-step conversion; PSRR.

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1. Introduction

Nowadays, wireless sensors are actively deployed in various applications including human healthcare, smart building, predictive maintenance and radio-frequency identification (RFID).[1] Limited energy storage has always been one of the major bottlenecks in wireless sensing systems which require prolonged system operating lifetime such as implantable biomedical devices and distributed wireless sensor networks.[2] As a result, high accuracy sensor readout circuits with ultra-low power consumption are an essential building block in such systems. Various energy harvesting techniques (e.g., thermoelectric, piezoelectric and photovoltaic energy harvester, etc.) have also been extensively investigated to achieve autonomous system operation.[3,4]

The design of an energy efficient high accuracy capacitive sensor readout circuit that can be directly powered by on-chip solar cells can be beneficial to autonomous wireless sensing applications. Due to the ambient energy fluctuations, the open circuit voltage of on-chip solar cells typically varies from 0.3 V to 0.6 V (depending on different illumination conditions).[5] This low supply voltage and input energy-dependent supply noise poses a major design challenge to achieve a high sensor readout accuracy. As observed in Ref. 6, the sensor readout circuit, which is directly powered by on-chip solar cell, suffers from such an input energy-dependent supply noise and achieved only limited readout accuracy. Typically, this supply noise issue can be resolved by using linear regulators as in Ref. 7. However, introducing regulators inevitably lead to extra energy conversion loss. The high supply voltage requirement also mandates extra step-up rectification stages, penalizing the system energy efficiency. To solve this problem, a supply insensitive sensor readout circuit is demonstrated in Ref. 8 to achieve high sensing accuracy by using of a force-balanced Wheatstone bridge and a differential Maneatis-cell with ratiometric readout. However, the readout circuit requires a relatively high supply voltage of 0.85 V and cannot be powered directly by on-chip solar cells. In Ref. 9, an ultra-low voltage sensor readout that can operate down to 0.3 V is presented. By using a fully-digital pseudo-differential architecture and a ratiometric readout scheme, an estimated power supply rejection ratio (PSRR) of 1.2% is achieved. Yet, it only exhibits an input sensing range of 300 fF due to the distortion introduced in the readout paths and customized solutions are required in different application scenarios.

This work targets wireless sensor network applications where solar energy harvesting can be exploited to prolong the system operation lifetime. The proposed sensor readout can be directly powered by the on-chip solar cell. One possible application is for indoor air quality control where the system can be powered by lighting fixtures to monitor the CO_2 level.[10] Another application area is for habitat-modeling or precision farming[11,12] where the system is generally required to operate mainly during the daytime. The proposed sensor readout system can also be equipped with a rechargeable energy source to further extend the possible application area.[13]

The proposed energy efficient supply voltage tolerant fully-digital two-step successive approximation register/delta sigma (SAR/$\Delta\Sigma$) capacitive sensor readout can be directly powered by the on-chip photodiode from 0.3 V to 0.42 V (corresponding to an illumination level from 500 Lux to 20 kLux using a 0.144 μm^2 on-chip photodiode) with a wide input-range from 1.5 pF to 6.5 pF. An extended supply voltage range up to 0.6 V is also possible. By using two capacitance controlled oscillators (CCOs) in a pseudo-differential configuration and a ratiometric readout scheme, a PSRR of 0.67% is achieved. At 3.5 pF input capacitance and 0.3 V supply, the $\Delta\Sigma$ stage accomplishes a resolution of 7.1-bit (corresponding to a capacitance of 2.2 fF/LSB). With an average power consumption of 40 nW and a sampling frequency of 47.5 kHz, a figure-of-merit (FoM) of 0.78 pJ/conv-step is achieved.

This paper is organized as follows. Section 2 outlines the system overview of the solar cell driven two-step wide-range sensor readout circuit. Section 3 discusses the system design considerations and the major error sources. Section 4 provides the simulation results of the proposed readout circuit using a standard 0.18 μm CMOS technology. The conclusion is given in Sec. 5.

2. System Overview

Figure 1 shows the block diagram of the proposed solar cell driven capacitive sensor readout system. The sensor readout system comprises an on-chip solar cell, a CCO-based time-to-digital converter (TDC) and a sub-threshold SAR/$\Delta\Sigma$ digital controller. The complete sensing system is powered by the on-chip solar cell with a targeted operating condition from 500 Lux (indoor environment) to 20 kLux

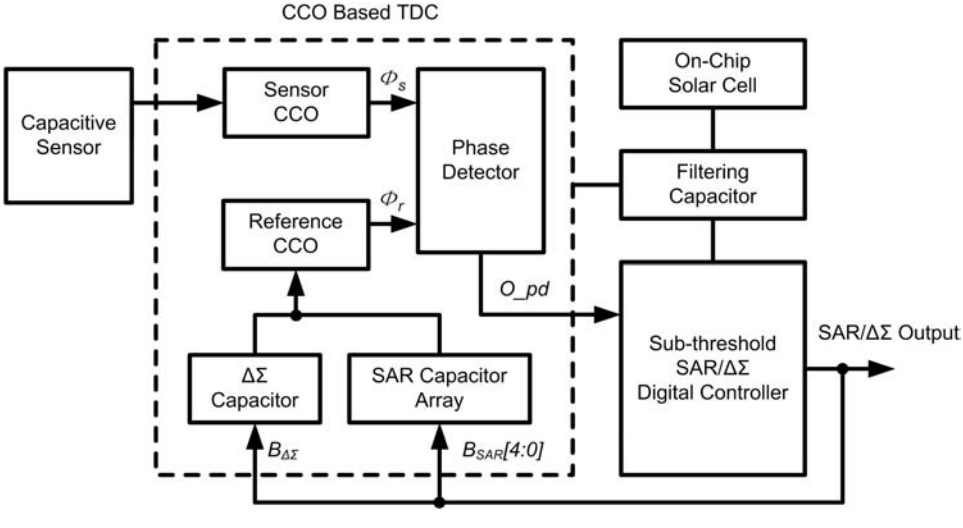


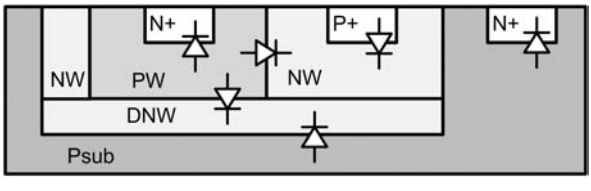
Fig. 1. The proposed solar cell driven capacitive sensor readout system.

(outdoor environment). The CCO-based TDC topology (instead of the voltage domain analog-to-digital conversion (ADC)) is utilized to achieve ultra-low voltage operation. The digital controller is synthesized using a customized sub-threshold digital standard cell library optimized at 0.3 V supply. According to the SAR/$\Delta\Sigma$ output, the controller generates the control signals for the SAR/$\Delta\Sigma$ conversion.

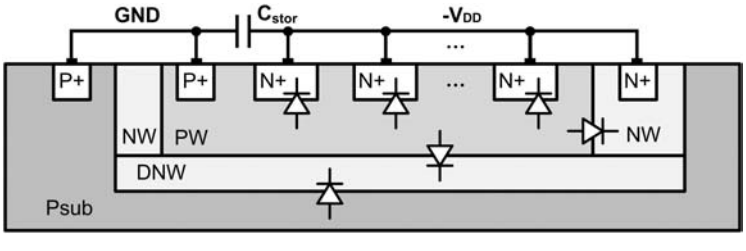
2.1. *On-chip solar energy harvesting*

The equivalent circuit for the on-chip solar cell includes a forward-biased diode, a current source I_{ph}, a shunt resistance R_{sh} and a series resistance R_s. In a standard triple-well p-substrate CMOS process, the bulk is generally referenced to ground (GND). In order to harvest the most solar energy per unit area, the substrate photodiode should also be utilized. This results in a negative supply for the capacitive sensor readout circuit, and NMOS transistors should be built within the deep-Nwell (DNW) to prevent forward biasing the parasitic diodes.

Figure 2(a) shows the six possible PN photodiode configurations in a standard triple-well CMOS process: (i) PW/N+, (ii) P+/NW, (iii) PW/NW, (iv) PW/DNW, (v) Psub/DNW and (vi) Psub/N+. Intuitively, in order to achieve improved conversion efficiency, the total PN junction areas should be maximized. In order to fulfill the design rule requirements, we make use of the PW/DNW photodiode with split N+ fingers to increase both the lateral and vertical PN junction areas. As a result, four types of PN junctions (i.e., Psub/DNW, PW/DNW, PW/NW and PW/N+) can be connected in parallel in the same substrate, increasing the overall generated



(a)



(b)

Fig. 2. (a) Six different types of PN junctions in the CMOS process. (b) Parallel connected photodiodes (Psub/DNW, PW/DNW, PW/NW and PW/N+) on the same substrate.

photocurrent per unit area. The implementation of the on-chip photodiode is shown in Fig. 2(b). A filtering capacitor C_{stor} (implemented using MOSCAP) is needed to avoid excessive ripple in the supply for accurate sensing. The expected supply voltage $|V_{DD}|$ is approximately 0.3 V and will be detailed in Sec. 3.1.

2.2. *CCO-based TDC with sub-threshold digital controller*

Unlike the traditional ADC topology, TDC provides an effective way to surmount the voltage headroom limitations and is preferred in ultra-low voltage designs. As shown in Fig. 3, the designed TDC is composed of two CCOs, a phase detector, a sub-threshold SAR/$\Delta\Sigma$ digital controller, a SAR capacitor array and a $\Delta\Sigma$ capacitor C_d.

As discussed before, the signal conversion is divided into two quantization steps, which are the coarse SAR conversion and the fine $\Delta\Sigma$ conversion. With a unit capacitance C_{LSB}, the binary coded SAR capacitor array is controlled by the SAR/$\Delta\Sigma$ digital controller to form a capacitive digital-to-analog converter (DAC). The coarse SAR conversion can be used to cancel the sensor offset capacitance C_o as well as to perform coarse signal conversion. The sensor residue capacitance C_{rsd} is then quantized by the $\Delta\Sigma$ conversion. Figure 4 shows a complete conversion cycle of the proposed two-step conversion scheme. At the beginning of the coarse conversion, the control logic first configures the converter into SAR mode. During this period, the two CCOs convert the sensor capacitance C_s and the reference capacitance C_r into two time signals T_s and T_r, respectively. Their phase difference is then digitized by the phase detector. The generated digital output is then fed back to the SAR capacitive DAC for subsequent conversions. At the end of the coarse conversion, C_o is determined by the 5-bit digital output B_{SAR}. The digital controller ensures T_r to be strictly smaller than T_s for proper $\Delta\Sigma$ operations.

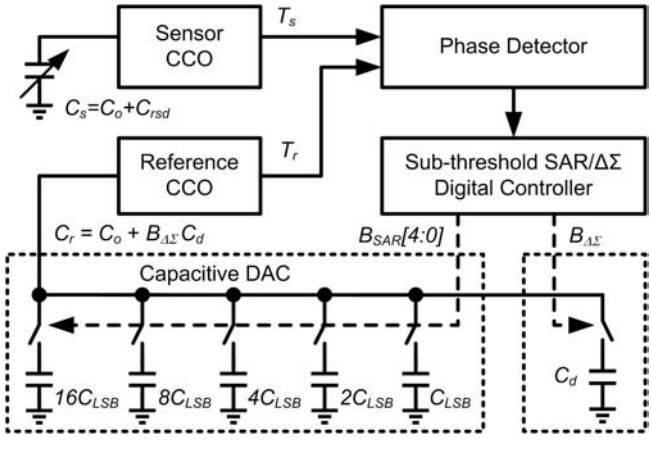


Fig. 3. The proposed CCOs-based TDC with digital controller.

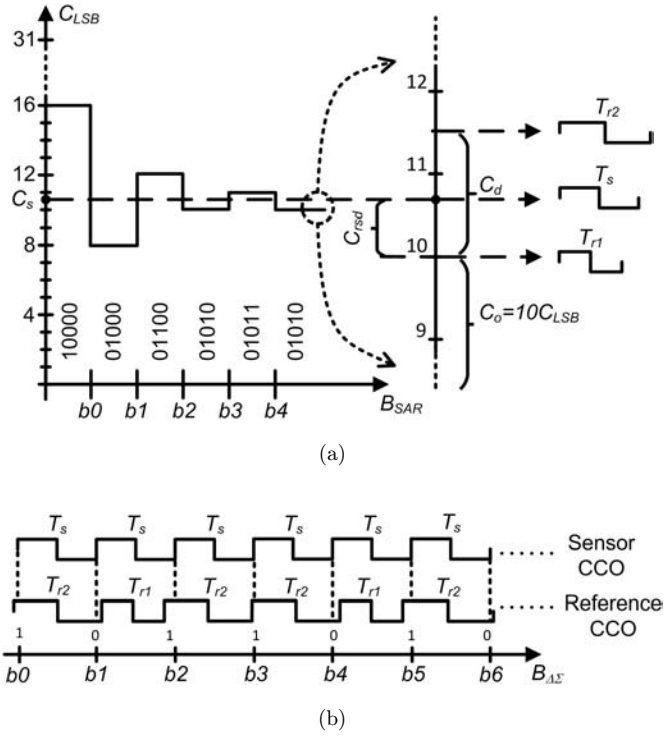


Fig. 4. A complete conversion cycle of the proposed CCO-based TDC: (a) coarse SAR conversion stage, and (b) fine $\Delta\Sigma$ conversion stage.

In the beginning of the fine conversion stage, the digital controller reconfigures the TDC into $\Delta\Sigma$ mode to maximize hardware reuse. During this step, C_d is utilized for signal conversion and T_r switches to either T_{r1} or T_{r2} ($T_{r1} < T_{r2}$) depending on the phase detector output *O_pd* in each cycle. The two CCOs act as time integrators to integrate the phase quantization error. In each $\Delta\Sigma$ conversion cycle, if the phase of the sensor CCO exceeds that of the reference CCO, the period of T_{r2} will be integrated in reference CCO in the next conversion cycle. Otherwise, T_{r1} will be integrated. As the difference of the quantization error between consecutive cycles is integrated in the two CCOs, the phase quantization error is first-order noise-shaped. The output bit stream $B_{\Delta\Sigma}$ can then be combined with B_{SAR} to generate the final digital output. This two-step conversion takes advantage of the fast SAR conversion and the high resolution $\Delta\Sigma$ modulation to achieve improved energy efficiency. The introduction of the SAR stage can be used to cancel the sensor offset as well as to resolve the intrinsic limited sensing range as in a standalone $\Delta\Sigma$ implementation.

2.3. *Sub-threshold digital design*

As the CCO-based TDC is designed to operate under an ultra-low supply voltage, the digital controller should also be optimized to operate in the sub-threshold region to ensure proper system level integration. This subsection first details the design of the customized sub-threshold digital library (optimized at 0.3 V supply) followed by the description of the synthesized SAR/$\Delta\Sigma$ digital controller.

In order to ensure ultra-low voltage operation with improved energy efficiency, the customized sub-threshold standard cell library utilized the inverse-narrow-width (INW) effect. With a fixed supply voltage V_{DD} and transistor length L, the transistor threshold voltage V_T is highly dependent on the transistor width W and can be expressed as[14]

$$V_T = V_{\text{fb}} + \psi_s + \left(\frac{Q_b}{WLC_{\text{ox}}}\right) \cdot \left[1 - \left(\sqrt{1 + \frac{2W_d}{r_j}} - 1\right)\left(\frac{r_j}{L}\right)\right]\left[1 - \frac{F}{W + F}\right], \quad (1)$$

where V_{fb} is the flat-band voltage, Ψ_s is the surface potential, Q_b is the ionized impurity concentration, C_{ox} is the thin gate oxide capacitance, W_d is the depth of the gate-induced depletion region, r_j is junction depth, and F is the fringing factor. Note that V_T is process-dependent and can be optimized with different W as a result of the INW effect. The minimum V_T of a N-type/P-type metal-oxide-semiconductor field effect transistor (NMOS/PMOS) device can be extracted by sweeping W using the minimum L. As demonstrated in Ref. 15, the minimum V_T for NMOS and PMOS using the selected 0.18 μm CMOS process is achieved with a transistor width of 220 nm and 400–590 nm, respectively. Figure 5 demonstrates the propagation delay

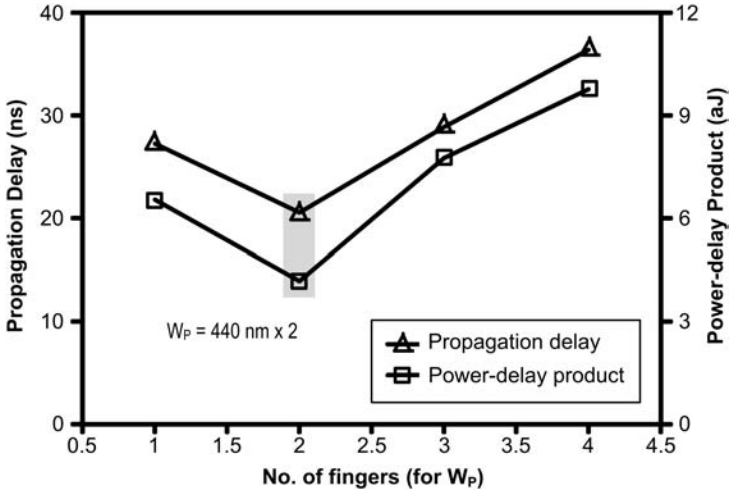


Fig. 5. Propagation delay and PDP versus number of fingers (for W_P) simulated using a FO4 loaded inverter with identical PMOS width (880 nm) and minimum NMOS width (220 nm) at 0.3 V.

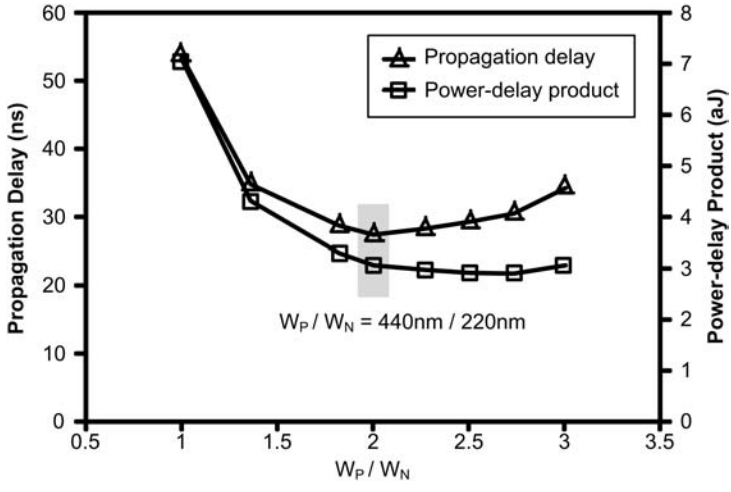


Fig. 6. Propagation delay and PDP versus W_P/W_N ratio (normalized to minimum W_N) simulated using a FO4 loaded inverter applying the INW effect at 0.3 V.

and power-delay product (PDP) of a fan-out-of-4 (FO4) inverter by applying different number of fingers while keeping the total PMOS width (W_P) identical. It can be observed that the PMOS finger width with 440 nm results in a minimum propagation delay and also the PDP. Figure 6 shows the propagation delay and PDP of a FO4 inverter with different W_P/W_N ratios applying the INW effect at 0.3 V. It can be seen that the minimum PDP is obtained with a PMOS width of 440 nm and a NMOS width of 220 nm. By using logical effort, the dimensions of parallel devices as well as stack devices can be determined from the resistance model of the reference inverter. The resistance of each transistor in an n-stacked device is scaled to $1/n$ times to that of a nominal transistor in order to maintain an identical total resistance as the reference inverter. These design guidelines form the basis for individual logic cell designs for the customized sub-threshold digital library. Detailed discussions can be found in Ref. 15.

The FSM of the digital controller is shown in Fig. 7, where m denotes the cycle number during the SAR conversion, and Φ_r and *O_pd* represent the output of the reference CCO and the phase detector, respectively. After initialization, the two CCO integration nodes are reset. Depending on the value of m which indicates whether the system is currently starting up or not, the sensor readout will either perform a one-time SAR conversion or utilize the previously stored B_{SAR} value as an estimate and bypass the SAR conversion altogether followed by the $\Delta\Sigma$ conversion step. To avoid overflow/underflow during the $\Delta\Sigma$ conversion, *Sbitcnt* is utilized for counting the number of consecutive "1" or "0" from *O_pd*, setting up the threshold to trigger the SAR conversion. The value of *Sbitcnt* is selected to ensure that sufficient redundancy is provided between the SAR and $\Delta\Sigma$ conversions.

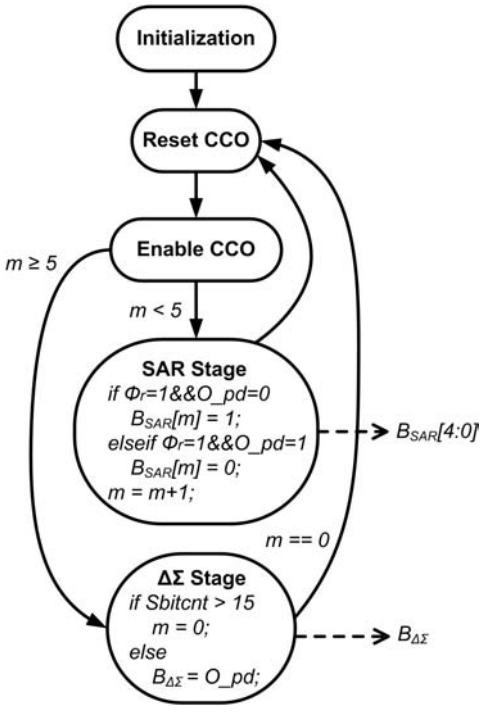


Fig. 7. The finite state machine (FSM) of the SAR/ΔΣ digital controller.

3. Design Considerations

Figure 8 shows the circuit implementation of the CCO-based TDC. The two inverter-based CCOs are constructed using a signal conversion stage followed by a buffer stage. The capacitive sensor C_s and the capacitive array are inserted within the corresponding signal conversion stage. The outputs from the CCOs are compared using a D-flipflop (DFF) and the result is processed by the digital controller for proper conversion operations. Even though the inverter-based circuit can operate at an ultra-low supply voltage for improved energy performance, the lack of cascoding stages can jeopardize its PSRR, which can be a significant error source as the system is directly powered by on-chip solar cells. Other non-ideal effects including the nonlinear switch on- and off-resistance and substantial buffer delay as a result of ultra-low voltage operation can also lead to degradation in the sensing accuracy. This section investigates each of these non-ideal effects to achieve optimized sensor readout performance.

3.1. *On-chip solar cell*

The performance of the fabricated on-chip photodiodes is imperative to the robustness of the sensor readout system. As discussed in Sec. 2.1, we connect four

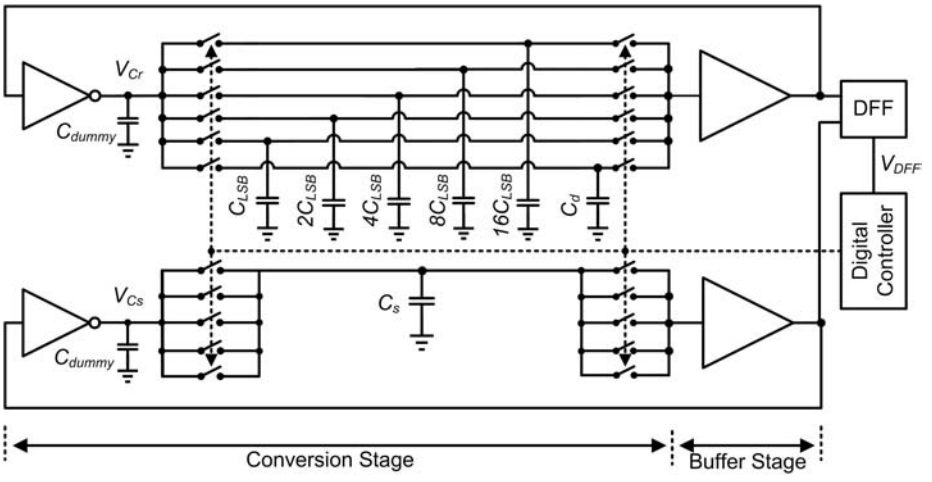


Fig. 8. The circuit implementation of the CCO-based TDC.

types of PN photodiodes (i.e., Psub/DNW, PW/DNW, PW/NW and PW/N+) in parallel in the same substrate. Table 1 summarizes the corresponding estimated short circuit current (I_{sc}) and open circuit voltage (V_{oc}) based on silicon measurement results obtained using the same 0.18 μm CMOS process with a halogen light source.

According to Table 1, the system should operate with a supply voltage less than 324 mV. Figure 9 illustrates the performance of the on-chip solar cell together with the sensor readout circuit, showing an expected operating region from 0.3 V to 0.42 V. With a simulated system average current consumption of 122 nA at 0.3 V, the worst case photodiode area required is estimated to be 0.144 mm^2 at 500 Lux.

As the TDC consumes dynamic power, voltage ripples will appear in the supply voltage affecting the sensor readout performance. Figure 10 shows the relationship between C_{stor} and signal-to-noise-and-distortion ratio (SNDR) of the sensor readout. A C_{stor} value of 250 pF is selected to achieve the optimal performance while minimizing the area overhead.

3.2. *Noise analysis*

In this design, the noise performance can be analyzed by the quantization noise and phase noise during the fine $\Delta\Sigma$ conversion. For the quantization error, we assumed

Table 1. Estimated photodiode performance under different illumination conditions.

Illumination [Lux]	500	5000	20000
I_{sc}/unit area [pA/μm^2]	1.5	14.94	60
V_{oc} [mV]	324	385	422

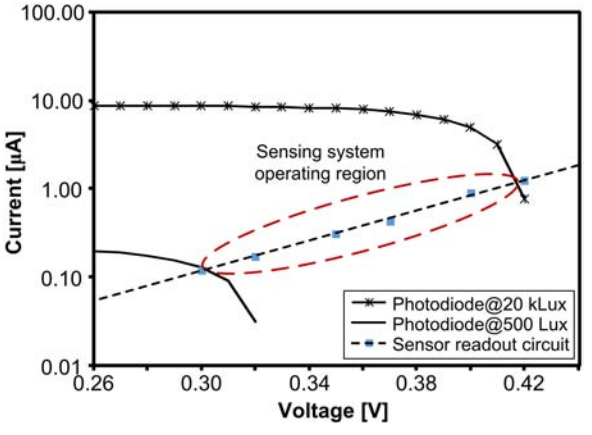


Fig. 9. (Color online) I–V characteristics of the designed on-chip solar cell and the sensor readout circuit.

that it has equal probability in the entire sensor input range. With Δ denoting the quantization step, the mean square quantization error is equal to $\Delta^2/12$. The total quantization noise power in the signal band, $P^2_{Q\_N,\mathrm{rms}}$, can be written as[16]

$$P^2_{Q\_N,\mathrm{rms}} = \frac{\Delta^2}{12}\,\frac{\pi^2}{3}\,\frac{1}{\mathrm{OSR}^3}\,, \tag{2}$$

where OSR is the oversampling ratio. With a full scale sinusoidal input signal applied, the output signal power $P^2_{\mathrm{Sig,rms}}$ can be expressed as

$$P^2_{\mathrm{Sig,rms}} = \frac{1}{T}\int_0^T (\Delta \sin 2\pi ft)^2 dt = \frac{\Delta^2}{2}\,, \tag{3}$$

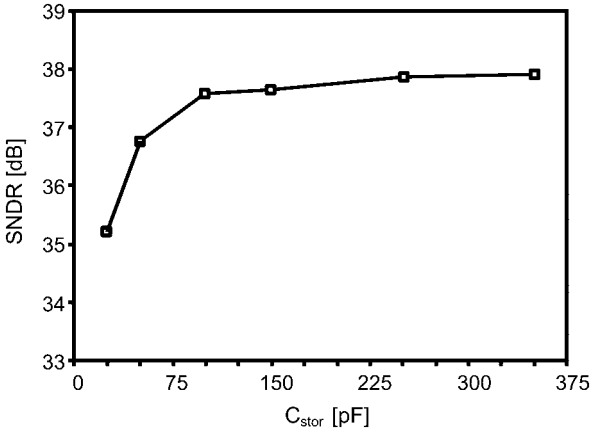


Fig. 10. Simulated SNDR versus C_{stor} for the sensor readout.

where T is the signal period. As a result, the signal-to-quantization-noise ratio (SQNR) can be derived as

$$\mathrm{SQNR[dB]} = 10\log\frac{P^2_{\mathrm{Sig,rms}}}{P^2_{Q\_N,\mathrm{rms}}} = 2.61 + 30\log\mathrm{OSR}\,. \tag{4}$$

In terms of phase noise $L(\Delta f)$, it is mainly introduced by the device noise and power supply/substrate noise and can be described as[17]

$$L(\Delta f) = 10\log\frac{P_{\mathrm{sideband}}(f_0+\Delta f, 1\,\mathrm{Hz})}{P_{\mathrm{carrier}}}\,, \tag{5}$$

where P_{carrier} is the power of the carrier and $P_{\mathrm{sideband}}(f_0+\Delta f, 1\,\mathrm{Hz})$ is the single sideband power at an offset frequency of $f_0+\Delta f$ with a 1 Hz bandwidth. As the output phase noise of the CCO is fed back to the input, $L(\Delta f)$ can be considered as the input referred phase noise P_{P_N}, and its rms noise power after oversampling is

$$P^2_{P\_N,\mathrm{rms}} = \frac{P^2_{P\_N}}{\mathrm{OSR}}\,. \tag{6}$$

As a result, the signal-to-phase-noise ratio (SPNR) is

$$\mathrm{SPNR[dB]} = 10\log\frac{P^2_{\mathrm{Sig,rms}}}{P^2_{P\_N,\mathrm{rms}}} = 20\log\frac{\Delta}{P_{P\_N}} + 10\log\frac{\mathrm{OSR}}{2}\,. \tag{7}$$

From (4) and (7), it can be observed that the SPNR only has a 3 dB increase when doubling the OSR instead of a 9 dB increase in SQNR. As the phase noise is much larger than the quantization noise at low frequency, the corresponding signal-to-noise ratio (SNR) is dominated by the SPNR, and the phase noise ultimately limits the achievable performance of the proposed sensor readout.

3.3. *Switch arrangements*

Due to the finite on- and off-resistance of CMOS switches, the implementation and arrangement of the switches is imperative to improve the sensor readout performance. To reduce the input-dependent switch resistance effect, all the switches are implemented using transmission gates. A total of 32 unit capacitors C_{LSB} (instead of using binary coded ones) are connected in parallel for better matching. Figure 11 shows two different switch arrangements SL1 an SL2 for capacitor selections, with R_p, R_n, and R_{tgp} and R_{tgn} denoting the average resistance of the corresponding transistors, respectively. Without loss of generality, we only consider the charging phase in the following analysis, i.e., $R_n >> R_p$, R_{tgp}, R_{tgn}. The corresponding voltages across the capacitors can be expressed as

$$V_{\mathrm{SL1}}(t) = V_{DD}\left(1 - \frac{R_p}{R_p + R_{\mathrm{tgp}}\|R_{\mathrm{tgn}}}e^{-t/\tau_{\mathrm{SL1}}}\right), \tag{8}$$

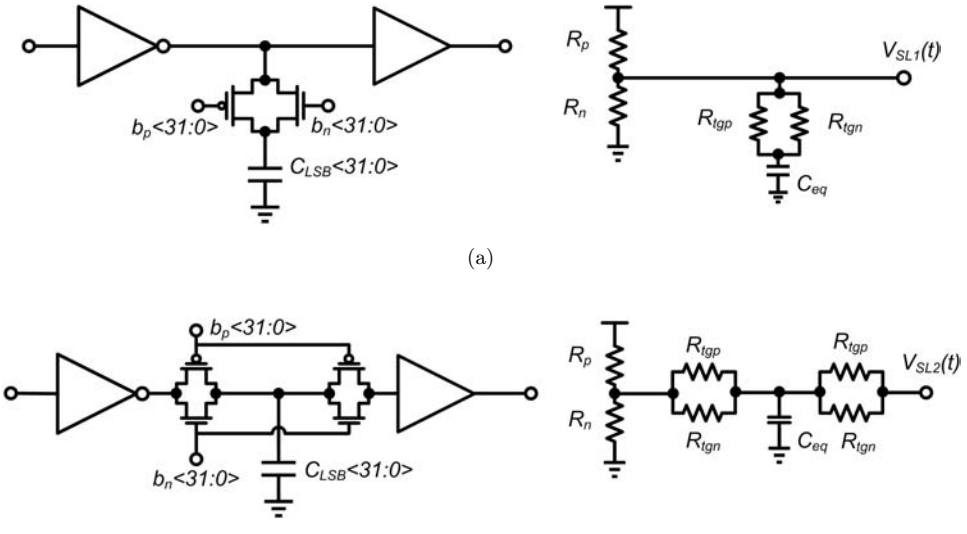


Fig. 11. Switch location using transmission gates: (a) SL1 and (b) SL2.

$$V_{\mathrm{SL2}}(t) = V_{DD}\left(1 - e^{-t/\tau_{\mathrm{SL2}}}\right), \tag{9}$$

where τ_{SL1} and τ_{SL2} represent the corresponding charging time constants with

$$\tau_{\mathrm{SL1}} = \tau_{\mathrm{SL2}} = \tau_{\mathrm{cha}} = (R_p + R_{\mathrm{tgp}} \| R_{\mathrm{tgn}})C\,. \tag{10}$$

Note that the effect of the switch connected to the buffer in Fig. 11(b) is negligible due to the high input impedance. Assuming the trip point of the next stage inverter is $\alpha V_{DD} (0 < \alpha < 1)$, the delays in the charging phase can be expressed as

$$t_{\mathrm{SL1}} = \tau_{\mathrm{cha}} \ln \frac{R_p(1-\alpha)^{-1}}{R_p + R_{\mathrm{tgp}} \| R_{\mathrm{tgn}}}\,, \tag{11}$$

$$t_{\mathrm{SL2}} = \tau_{\mathrm{cha}} \ln (1-\alpha)^{-1}\,. \tag{12}$$

It can be observed that $t_{\mathrm{SL1}} < t_{\mathrm{SL2}}$ for all realistic values of R_p, R_{tgp} and R_{tgn}, leading to a larger capacitance to time gain for SL2 when compared with SL1. As a consequence, SL2 should be chosen for improved signal power under the same power budget. Also, additional second-order effects introduced by R_p, R_{tgp} and R_{tgn} for SL1 can also lead to increased distortion during signal conversion. The nonlinearity introduced by the CCO as a result of different C_{SAR} is characterized by the absolute time delay error expressed as

$$\text{Absolute Time Delay Error } (\%) = \left| \frac{(T_{r2} - T_{r1})|_{C_{\mathrm{SAR}}+C_{\mathrm{LSB}}} - (T_{r2} - T_{r1})|_{C_{\mathrm{SAR}}}}{(T_{r2} - T_{r1})|_{C_{\mathrm{SAR}}}} \right|. \tag{13}$$

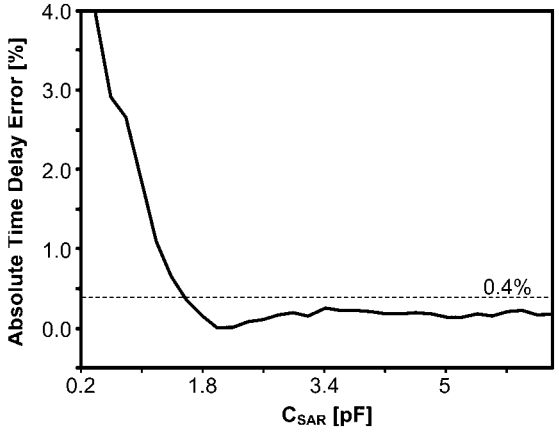


Fig. 12. Design tradeoff between C_{SAR} and the absolute time delay error.

Figure 12 shows the simulation result of the absolute time delay error with different C_{SAR}. It can be observed that a minimum C_{SAR} of 1.5 pF is required to achieve an error of $< 0.4\%$. This is equivalent to a resolution of 8-bit and sets the corresponding minimum sensor input capacitance.

3.4. *Buffer stage propagation delay*

Except from the signal conversion stage, the buffer stage which is implemented using an even number of inverters also generates finite delay that can affect the CCO oscillation frequency (f_{CCO}) and is defined as

$$\frac{1}{f_{\mathrm{CCO}}} = t_C + t_{\mathrm{buf}}, \tag{14}$$

where t_C and t_{buf} denote the total delay in both charging and discharging phases for the signal conversion stage and the buffer stage, respectively. Ideally, t_{buf} should be the intrinsic delay and is signal-independent. But as the input rise/fall time of the buffer stage deviates from the ideal step input, t_{buf} becomes input signal-dependent that can increase the signal distortion at the converter output. Figure 13 illustrates the simulation result of the variation in t_{buf} as the loading capacitance C varies with different C_{dummy} and is defined as

$$t_{\mathrm{buf}} \text{ variation}[\%] = \frac{t_{\mathrm{buf}}|_{C_d=C} - t_{\mathrm{buf}}|_{C_d=0}}{t_C|_{C_d=0}}. \tag{15}$$

It can be seen that the t_{buf} variation becomes significant as C_{dummy} reduces. By using Fig. 13, a minimum C_{dummy} of 1.5 pF is required to achieve an error of $< 0.4\%$ with a corresponding C_{LSB} of 200 fF. C_d is set to 300 fF to introduce redundancy and avoid missing code. Due to the finite setup and hold time of the DFF, a minimum

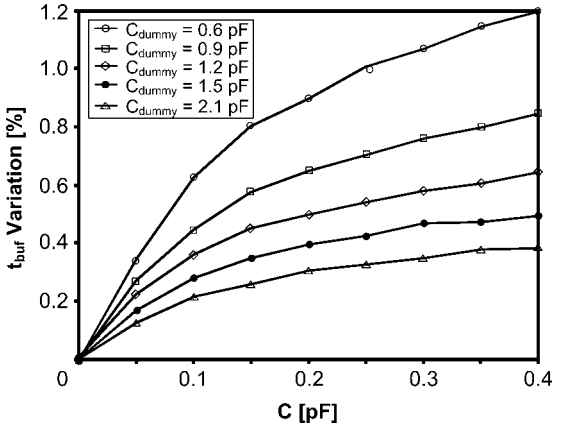


Fig. 13. Simulation result showing the change in t_{buf} as C varies.

timing difference between T_{r1} and T_{r2} should be ensured for accurate signal conversion. Figure 14 shows the effect of C_{dummy} on the timing difference $(T_{r1} - T_{r2})$. For a dummy capacitance of 1.5 pF, the timing difference equals to 120 ns. This defines the DFF setup and hold time requirement during the design stage.

3.5. *Power supply rejection*

During the coarse conversion, C_r will approach C_o and the residue error C_{rsd} is within 200 fF. In order to avoid missing codes, C_d is set to 300 fF to introduce redundancy during the $\Delta\Sigma$ operation. With B_1 denoting the ratio between the number of ones and the total number of bits in the $\Delta\Sigma$ output bit stream, the following relationship between the oscillation frequencies of the sensor CCO and reference CCO can be

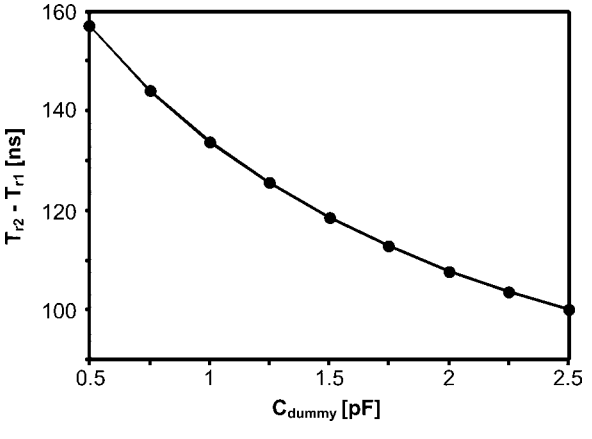


Fig. 14. The difference in timing $(T_{r2} - T_{r1})$ with different C_{dummy}.

obtained:

$$\frac{1-B_1}{f_{\mathrm{CCO}}}\bigg|_{C_r=C_o}+\frac{B_1}{f_{\mathrm{CCO}}}\bigg|_{C_r=C_o+C_d}=\frac{1}{f_{\mathrm{CCO}}}\bigg|_{C_s}. \tag{16}$$

With a C_{dummy} of 1.5 pF and a worst case difference between C_r and C_s of 300 fF, the resultant t_{buf} variation is within 0.5% (as illustrated in Fig. 13). As a result, we can assume that $t_{\mathrm{buf}}|_{Cr=Co}$, $t_{\mathrm{buf}}|_{Cr=Co+Cd}$ and $t_{\mathrm{buf}}|_{Cs}$ approximately equal to each other during the $\Delta\Sigma$ conversion and (8) can be approximated as

$$(1-B_1)\times t_{C=C_o}+B_1\times t_{C=C_o+C_d}=t_{C=C_o+C_{\mathrm{rsd}}}. \tag{17}$$

For any capacitor C, the corresponding time constant during the discharging phase is equal to $(R_n+R_{tg})C$, and the total delay t_C can be expressed as

$$t_C=(R_p+R_n+2R_{\mathrm{tg}})C\ln 2. \tag{18}$$

As the equivalent resistance in (18) is sensitive to the supply voltage variation, t_C is also prone to supply noise, resulting in a supply sensitive CCO output frequency. With a ratiometric readout scheme, the supply sensitive term can be effectively cancelled. By substituting (18) into (17),

$$C_{\mathrm{rsd}}=B_1\times C_d. \tag{19}$$

Theoretically, the power supply noise should be completely cancelled. However, the residues between different t_{buf} and the mismatch in R_p, R_n and between the two CCOs can lead to reduced PSRR. With the use of the coarse SAR conversion, the two CCOs can be better matched during the $\Delta\Sigma$ conversion, improving the PSRR of the capacitive sensor readout. The use of a small C_d can also improve the linearity, and the resolution is mainly limited by the phase noise of the CCOs.[9]

4. Simulation Results

The complete solar-powered capacitive sensor readout system is implemented using a 0.18 μm standard CMOS process with a wide C_s range from 1.5 pF to 6.5 pF. A SAR stage is used during the coarse conversion and an OSR of 128 during the fine $\Delta\Sigma$ conversion. A 0.144 mm^2 solar cell operating under a 500 Lux environment and a 250 pF on-chip filtering capacitor are utilized. The control signals are generated with the digital controller synthesized using the customized sub-threshold standard cell library. Figure 15 shows the timing diagram of the proposed sensor readout system during the SAR and $\Delta\Sigma$ conversion with a 1.5 pF input capacitance. The ripple voltages at the supply are 5 mV and 1 mV during the SAR and $\Delta\Sigma$ conversion, respectively. Due to the increased power consumption during the $\Delta\Sigma$ conversion, a voltage droop of approximately 10 mV appears. The introduced error is resolved by introducing redundancy in the $\Delta\Sigma$ conversion and recovered after calibration.

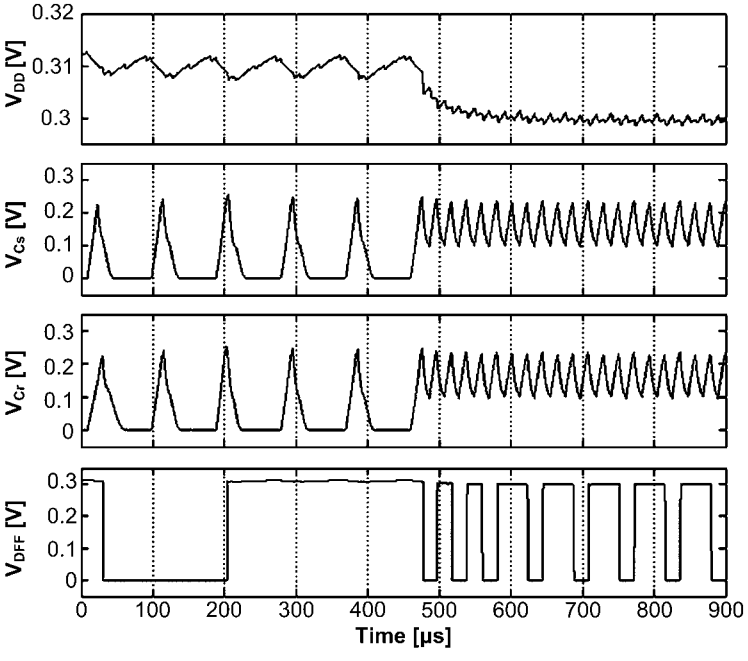


Fig. 15. Timing diagram of the proposed sensor readout with on-chip solar cell.

Figure 16 shows the simulated INL of the proposed capacitive sensor readout at 0.3 V. It can be observed that an INL of $+1.3/-1.4$ LSB can be achieved with C_s ranging from 1.5 pF to 6.5 pF. The source of error is mainly coming from the distortion introduced in the two CCOs. Figure 17 shows the simulated output spectrum with a mean Cs of 3.5 pF and a peak-to-peak variation of 100 fF at 36.8 Hz. The $\Delta\Sigma$ sampling and conversion frequencies are 47.5 kHz and 371 Hz, respectively. The calculated SNDR is 44.7 dB, corresponding to a resolution of 7.1-bit. The degradation in INL with a small C_s is mainly due to two reasons: (i) the CCO integration node impedance mismatch will increase, and (ii) the buffer stage delay variation will increase as the CCO integration node impedance is reduced. This is consistent with

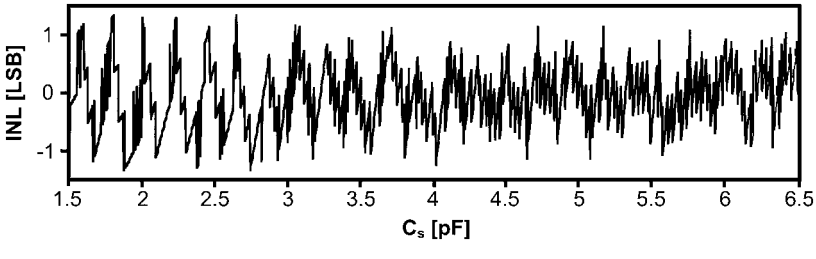


Fig. 16. Simulated INL for the proposed capacitive sensor readout at 0.3 V.

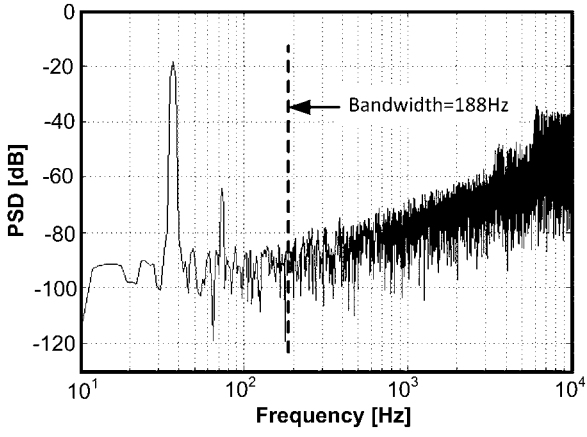


Fig. 17. Simulated output spectrum with $f_{\text{in}} = 36.8\,\text{Hz}$, $C_s = 3.5\,\text{pF}$ and an amplitude of 100 fF at 0.3 V.

the dynamic nonlinearity performance as shown in Fig. 18. Furthermore, as C_s increases, the CCO frequency becomes more insensitive to the change in the input capacitance, leading to a reduction in the $\Delta\Sigma$ quantization step. As a result, the sensor readout is more susceptible to phase noise, degrading the SNR/SNDR. When a 50 Hz noise source with a 1 mV and 2 mV peak-to-peak amplitude is added to the 300 mV power supply, the effective number-of-bits (ENOB) is degraded to 7.04-bit and 6.66-bit, respectively. The use of a large C_{stor} or digital filtering can be utilized in case of increased noise power.

Figure 19 shows the relative percentage TDC error (normalized to the result for $V_{DD} = 0.35\,\text{V}$) with an extended supply voltage ranging from 0.3 V to 0.6 V. The

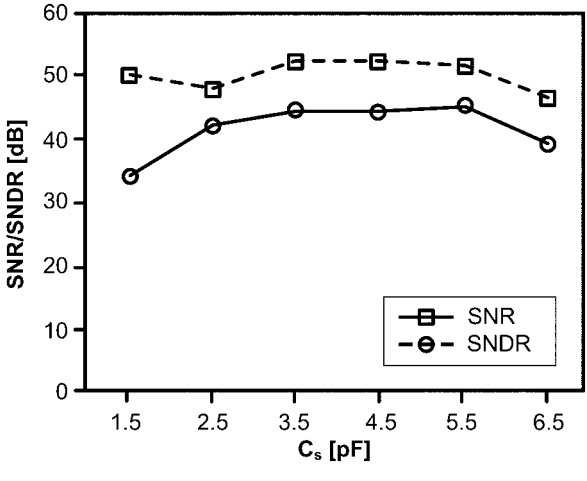


Fig. 18. Simulated SNR/SNDR versus different C_s at 0.3 V.

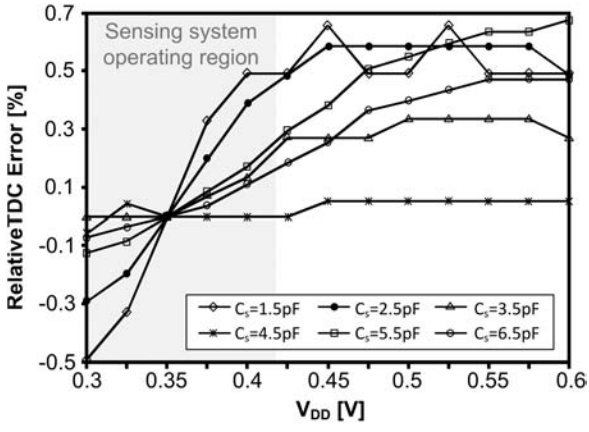


Fig. 19. Relative TDC error at different supply voltages with different C_s.

TDC output is dependent on the supply voltage as expected. The achieved error is within 0.5% from 0.3 V to 0.42 V, corresponding to the sensing system operating region with illumination level from 500 Lux to 20 kLux. Figure 20 shows the energy per conversion of the sensor readout circuit. For the $\Delta\Sigma$ stage, the average power consumption is 40 nW with a sampling frequency f_s of 47.5 kHz and an OSR of 128. By using the FoM as

$$\text{FoM} = \frac{P}{2^{\text{ENOB}} \times 2 \times \text{Bandwidth}} = \frac{P}{2^{\text{ENOB}} \times \dfrac{f_s}{\text{OSR}}}, \tag{20}$$

the proposed capacitive sensor readout circuit achieves a FoM of 0.78 pJ/conv-step. Table 2 shows the performance comparisons with recent sensor readout circuit publications.

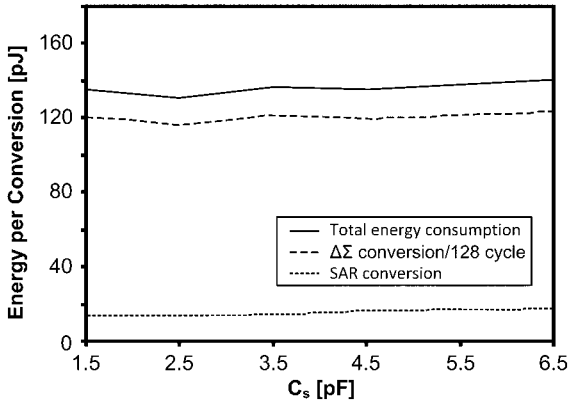


Fig. 20. Energy per conversion of the SAR stage, $\Delta\Sigma$ stage and the complete sensing system.

Table 2. Performance comparison.

	Ref. 8	Ref. 9	Ref. 12	Ref. 13	This Work
Topology	ΔΣ	ΔΣ	SAR	PWM	SAR/ΔΣ
Capacitive(C)/Resistive(R)	R	C	C	C	C
Sensor Range	2 kΩ	5.7–6 pF	50–53 pF	0.5–0.76 pF	1.5–6.5 pF
Supply Voltage (V)	1	0.3	1.4	3	0.3–0.6
ENOB	8.9 bit	6.1 bit	6.8 bit	8 bit	7.1 bit[a]
Power (μW)	124.5	0.27	236.6	84	0.04[a]
Conversion Freq. (Hz)	10M	1k	0.26M	30k	371[a]
PSRR at DC	0.7%	1.2%[b]	—	—	0.67%[c]
FoM (pJ/conv-step)	13.03	3.9	7.9	10	0.78[a]

[a]Simulation result at 300 mV supply with $C_s = 3.5$ pF (ΔΣ only).
[b]Estimated from the corresponding paper.
[c]Worst case over the entire sensing range.

5. Conclusion

A wide input-range of 1.5–6.5 pF fully-digital capacitive sensor readout circuit with on-chip solar cell using a standard 0.18 μm CMOS is reported. The complete system can operate with a supply voltage of as low as 0.3 V (500 Lux indoor environment). System level design/optimization with the on-chip solar cell and the sub-threshold digital controller is discussed in detail. Non-idealities in the readout circuit including the switch resistance and buffer stage propagation delay and their effect on the sensor readout performance are systematically analyzed. Simulation results show that by using the time-based pseudo-differential CCOs and a ratiometric readout scheme, a PSRR within 0.5% from 0.3 V to 0.42 V is achieved (0.67% in the extended range from 0.3 V to 0.6 V). With an average power consumption of 40 nW and a sampling frequency of 47.5 kHz, a FoM of 0.78 pJ/conv-step is achieved.

Acknowledgments

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