A 4.2-mW 77.1-dB SNDR 5-MHz BW DT 2-1 MASH ΔΣ Modulator With Multirate Opamp Sharing

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***Abstract*— This paper presents a discrete time 2-1 MASH Delta-Sigma (ΔΣ) modulator with multirate opamp sharing for analog-to-digital converters, targeting the optimization of power efficiency in active blocks, such as opamps and quantizers. Through the allocation of different settling times to the opamps and by adopting the multirate technique, the power of the shared opamps is utilized more efficiently, and the 4-b successive approximation register quantizer and the data weighted averaging block in the first stage enjoy additional operation time. Moreover, a detailed analysis and related simulations are presented to validate the enhanced opamp power efficiency in the proposed sharing scheme. The 65-nm CMOS experimental chip running at multirate 120/240 MHz achieves a mean signal-to-noise and distortion ratio (SNDR) of 77.1 dB for a 5-MHz bandwidth, consuming 4.2 mW from a 1.2 V supply and occupying 0.066-mm^2 core area. It exhibits a Walden figure of merit (FoM) of 69.7 fJ/conv-step and a Schreier FoM of 167.9 dB based on SNDR.**

***Index Terms*— Analog-to-digital converter (ADC), discrete-time (DT) delta sigma (ΔΣ) modulator, multi-stage noise shaping (MASH), wideband, power-efficient, opamp sharing, multirate, successive approximation register (SAR) quantizer.**

I. Introduction

THE constantly increasing popularity of portable devices in the consumer electronics market, especially personal wireless communication devices or battery-powered medical devices, translates into a growing demand for low-power and low-voltage system building blocks in recent years. Analog-to-digital Converters (ADC) play a significant role in such systems. Delta-sigma (ΔΣ) modulators provide obvious advantages over their Nyquist counterparts regarding relaxed requirements on analog components as well as the preceding anti-aliasing filter. By making use of oversampling and noise shaping properties, ΔΣ modulators transfer most of the signal processing tasks into the digital domain, where the power consumption can be significantly reduced by the continuously scaled-down CMOS technologies. Thereby, when it comes to high resolution wideband applications, ΔΣ modulators are more robust and power-efficient compared to other structures [1].

Due to the low oversampling ratio (OSR) in wideband applications and restricted number of bits of the quantizer, the requirement of high resolution can be satisfied by achieving more aggressive noise shaping in ΔΣ modulators. Single loop ΔΣ modulators are prone to be unstable as the order increases. The out-of-band gain needs to be reduced to stabilize the high-order modulator at the expense of increasing quantization noise as well as the circuit complexity owing to additional coefficient paths [2]. Another alternative way to overcome this stability problem is to cascade several inherently stable low-order single loop modulators, named as Multi-stAge noise SHaping (MASH) [3]–[10] ΔΣ modulators.

However, the perfect matching between analog and digital transfer functions in MASH ΔΣ modulators is highly required to eliminate the quantization noise of the preceding stages, otherwise the noise leakage will deteriorate the overall performance significantly [2]. MASH structures can be implemented through discrete time (DT) or continuous time (CT). Owing to large variations of resistor and capacitor values, the transfer functions are not so precisely defined in CT MASHs [8]–[10] while their DT counterparts are appreciated for robustness as the transfer functions highly rely on capacitor ratios. However, CT solutions allow a better power efficiency.

Although DT implementations impose higher bandwidth and slew rate (SR) requirements for operational amplifiers (opamp), several techniques at system-level have been developed to reduce opamps' power consumption. The double-sampling (DS) approach [5], [6] can boost the effective OSR by reusing all the active blocks of the modulator. As a result, for a given OSR, the sampling frequency can be reduced by a factor of 2 without compromising the resolution, thus greatly relaxing the gain-bandwidth product (GBW) and SR requirements of opamps. However, the noise folding caused by the mismatch between the two required DAC sampling

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capacitors degrades the performance. The employment of passive SC integrators [11], [12] can reduce the analog power consumption a lot by eliminating active power-hungry opamps. Nevertheless, due to the lack of the filter gain and parasitic sensitivity, higher quantization noise exists in the signal band of interest, limiting the achievable resolution. Moreover, these intrinsic properties of passive integrators will further worsen the leakage issue in MASH topologies. Due to the inherent switching activity, the opamp sharing technique [7], [13], [14] can be applied to reduce the number of required opamps in DT $\Delta\Sigma$ modulators, thus reducing power and area consumptions. However, the power efficiency of opamp sharing applied in 2-2 MASH can be improved further in [7].

The main objective of this work is to exploit a more power-efficient opamp sharing scheme for DT MASH $\Delta\Sigma$ modulators, and simultaneously address a stringent timing issue of the multi-bit quantizer and dynamic element matching (DEM) block caused by the horizontal opamp sharing [7]. This work also intends to incorporate SAR quantizers into DT MASH structures by distributing additional time to fit with the long conversion time required by SAR quantizers.

This paper is organized as follows. Section II briefly reviews the prior arts of opamp sharing and describes the proposed opamp sharing technique. Section III covers the system-level design considerations, presents analytical derivations and further performs simulations at transistor-level to validate the improved opamp power efficiency in the proposed topology. Section IV presents the circuit implementations, while Section V provides the measurement results and performance comparisons. Section VI concludes the paper.

II. Opamp Sharing Techniques in DT $\Delta\Sigma$ Modulators

A. Prior Opamp Sharing Arts

Straightforwardly, a horizontal sharing scheme can be applied between adjacent opamps to improve power efficiency in single loop $\Delta\Sigma$ modulators [13], [14]. However, in wide-band low-voltage low-power applications, multi-bit quantizers are often utilized to further suppress the quantization noise and reduce the output swings of the integrators. In such a scheme, DEM needs to be employed to reduce the nonlinearity introduced by multi-bit DACs. With such a horizontal scheme, the multi-bit quantizer and the DEM block must operate during the non-overlapping time of clock phases, which requires a very fast quantizer and DEM block with a low propagation delay [7]. Consequently, it would give rise to stringent power-speed tradeoffs.

To address this issue, as shown in Fig.1, [7] proposed to vertically share opamps between the integrators/adder of two independent loops in the 2-2 MASH. Hence, a half clock period is provided to the first stage's quantizer and DEM block to operate and also the same holds for the second stage's quantizer. Nevertheless, for the MASH system the power of the first integrator often dominates the total power consumption. Moreover, owing to a low OSR utilized in wideband applications, the difference in power consumption between two adjacent opamps is relatively small rather than

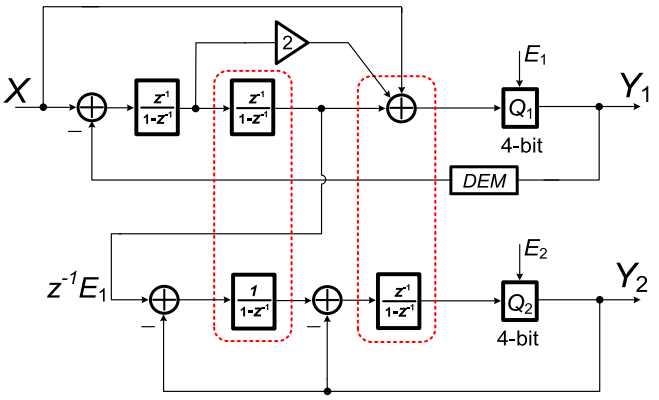

Fig. 1. Block diagram of the 2-2 MASH with vertical sharing proposed in [7].

enormous as in audio-bandwidth applications (a large OSR employed) [2]. Here we present a detailed analysis about the power difference in two adjacent integrators with respect to different OSRs. The on-resistance of the switches and the thermal noise of the opamp both contribute to the thermal noise of the switched-capacitor (SC) integrator. The total input-referred thermal noise of the i^{th} integrator is [2]

$$V^2_{\text{int}_i,ntotal} = \frac{N \cdot KT}{C_{s,i}} \cdot \frac{(2x+7/3)}{(x+1)} \cdot \frac{\pi^{2L}}{OSR^{2L+1}(2L+1)} \quad x = 2R_{on,i}g_{m,i} \quad L = i-1 \tag{1}$$

where $C_{\text{s,i}}$ is the sampling capacitor of the i^{th} integrator, $R_{\text{on,i}}$ denotes on-resistance of the switches in the integration path and $g_{\text{m,i}}$ is the input transistor's transconductance of the i^{th} integrator. Note that N is an integer, which is determined by the specific implementation topology [7]. The thermal noise of the $(i+1)^{\text{th}}$ integrator can be negligible so long as it is ten times less than the thermal noise of the i^{th} integrator. Hence, supposing that the same N and x are chosen for each one, the ratio of the sampling capacitor size required by both adjacent integrators in the same loop is given by,

$$\frac{C_{s,i}}{C_{s,(i+1)}} = \frac{1}{10} \cdot \frac{2i+1}{2(i-1)+1} \cdot \left(\frac{OSR}{\pi}\right)^2 \tag{2}$$

Furthermore, the power consumption of the integrator/opamp is proportional to its loading capacitance [1], which is highly related to its sampling capacitor [15]. Hence, assuming that the same opamp topology is employed for both integrators, the power ratio of them approximately yields to be,

$$\frac{P_i}{P_{i+1}} \approx \frac{1}{10} \cdot \frac{2i+1}{2(i-1)+1} \cdot \left(\frac{OSR}{\pi}\right)^2 \tag{3}$$

As observed in (3), the power difference in two adjacent integrators increases exponentially as the OSR increases.

Also, Table I summarizes the trade-offs between horizontal and vertical opamp sharing schemes applied in DT $\Delta\Sigma$ modulators.

Therefore, in case a low OSR is employed, it cannot exhibit a better opamp power efficiency among MASH architectures without horizontally sharing adjacent opamps of the first stage (especially for the first and second integrators). But the urgent

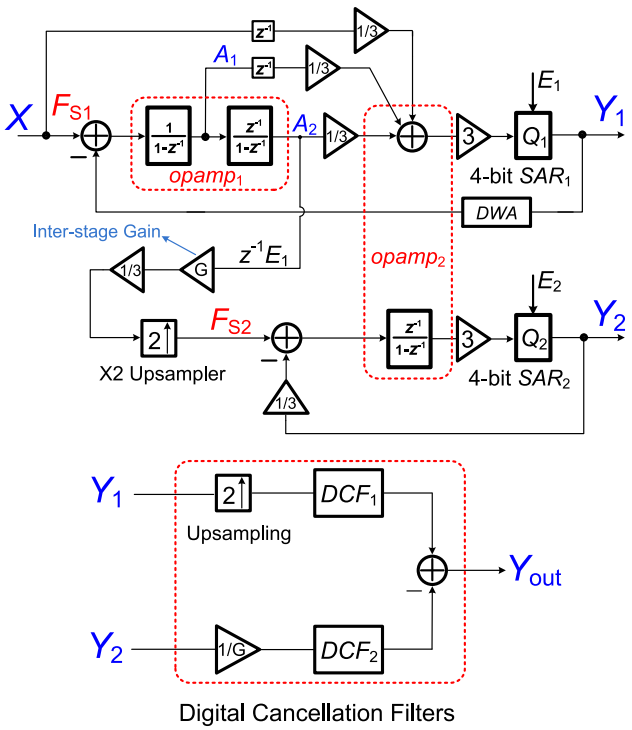

Fig. 2. Block diagram of the proposed DT 2-1 MASH together with the digital cancellation filters.

TABLE I
SUMMARY OF HORIZONTAL AND VERTICAL OPAMP SHARING SCHEMES IN DT ΔΣ MODULATORS

	Horizontal Sharing	Vertical Sharing
Architecture	Single-loop/MASH	MASH
Quantizer Time	Urgent	Normal
Sharing Efficiency	Good	Poor

timing issue of the following blocks (quantizer, etc.) caused by horizontal opamp sharing needs to be addressed.

B. Proposed Opamp Sharing Technique

Fig. 2 depicts the block diagram of the proposed DT 2-1 MASH modulator together with the digital cancellation filters (DCF). The modulator consists of a second-order Cascade of Integrators with weighted Feed-forward Summation (CIFF) and a first-order Cascade of Integrators with Distributed Feedback (CIFB) in the first and second stages [2], respectively. The data weighted averaging (DWA) [16] is employed here to improve the linearity of the first multi-bit DAC. The proposed sharing reduces the number of opamps from 4 to 2 to improve power efficiency, with the horizontally shared opamp between the first and second integrators in the first loop, and the vertically shared one between the adder of the first loop and the third integrator of the second loop.

Fig. 3 illustrates the timing chart for this DT 2-1 MASH operation. Note that the red and blue arrows correspond to signal flow paths in the first and second stages, respectively. First of all, the stringent timing issue of the first quantizer

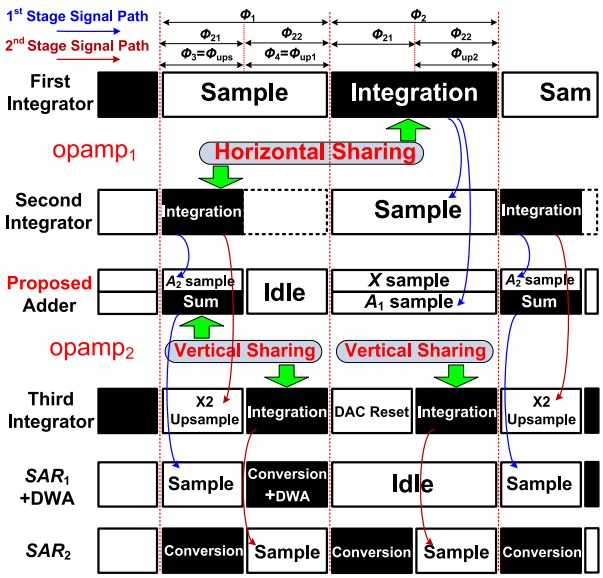

Fig. 3. The timing chart for the proposed DT 2-1 MASH operation.

and DWA block caused by the horizontal sharing is solved by distributing half of the adder's operating time to them. It is noteworthy that the reduction of the adder's settling time by half does not substantially influence the total power consumption since the power of the adder is much smaller than the preceding integrators. In this way, the original operating time of the adder splits into two portions; one for itself, and the other one for the following 4-bit quantizer and DWA block, which accomplishes a better power budget arrangement for both the opamp and the quantizer.

Next, several other blocks must implement corresponding alterations to cater for the reduction of the adder's settling time. First, the second integrator utilizes only a quarter of the clock period to accommodate the summing phase of the adder. Due to the horizontal sharing with the first integrator's opamp, shortening the effective settling time of the second integrator does not bring any power penalty but just makes such sharing more power-efficient. Second, to allow the vertical opamp sharing, the clock frequency driving the third integrator needs to increase by a factor of 2 accordingly. Nevertheless, with such a vertical sharing, doubling the sampling rate of the second stage does not substantially increase on power dissipation. Indeed, by operating in such a multirate mode, the OSR of the second stage will be increased by 2, thereby further boosting the achievable resolution [4]. Moreover, the proposed sharing scheme permits the sharing of the first and second quantizers' references because of the different conversion timing, further improving the reference generating quality while reducing the power and area consumptions.

By employing the feedforward structure in the first loop, the signal will directly go through the feedforward path, leaving only the quantization noise processed by the integrators [17]. Hence, this technique not only mitigates the linearity requirements of integrators/opamps significantly, but also makes it possible to implement a high-gain opamp with low power consumption. Furthermore, the output of

the second integrator can be regarded as the quantization noise of the first loop, thus directly becoming the input of the second loop without the necessity of using an extra DAC. As a result, it reduces the circuit complexity and chip area, especially for the multi-bit quantization. Even though driving the second stage increases the loading capacitance of the second integrator, it will not cause an overall power penalty since this opamp is shared with the first opamp, which is more power-hungry.

With such a feedforward topology, an attenuation factor $1/h_1$ ($h_1 = 3$) [3] introduced in the adder reduces its output swing. This boosts the dynamic range (DR) of the modulator as well as enhances the adder's feedback factor, hence reducing the power consumption further. Nevertheless, to compensate this attenuation and preserve the original transfer functions, the references of the first quantizer are scaled down by 1/3 with $LSB = 2.4\text{V}/(3 * 16) = 50\text{mV}$, a value that would require a careful design of comparators to limit their input-referred offsets if a flash quantizer is employed. This design completely circumvents this problem by using a 4-bit single-comparator SAR in the first stage. The SAR quantizer is not only more power and area efficient, but also free from code-dependent offset mismatch. Moreover, the longer conversion time required by the SAR in the first stage just fits well with the extra time given by the preceding adder. We likewise utilize a scaling factor $1/h_2$ ($h_2 = 3$) in the second stage with also a 4-bit SAR quantizer to reduce the swing of the third integrator and share the same references between both quantizers.

The overall proposed opamp sharing scheme addresses different requests simultaneously, namely: 1) more efficient use of timing for different opamps; 2) solving the stringent timing problem of the first quantizer and DWA block; 3) the employment of an efficient SAR with careful consideration of its timing due to the long conversion time; and eventually 4) employing the multirate solution to allow the vertical opamp sharing and further enhance the achievable resolution.

C. Digital Cancellation Filters

The digital output streams of the first and second stages Y_1 and Y_2, operating with a sampling frequency of F_{S1} and $F_{S2} = 2F_{S1}$ respectively, are expressed in the z-domain,

$$Y_1(z) \approx X(z) + (1 - z^{-1})^2 E_1(z) \tag{4}$$

$$Y_2(z) = G \cdot z^{-1}\left(z^{-2}E_1(z^2)\right) + (1 - z^{-1})E_2(z) \tag{5}$$

Note that $z^{-2}E_1(z^2)$ is the corresponding product, when $z^{-1}E_1(z)$ (the output of the second integrator) is upsampled by a factor of 2 through using the X2 upsampler [18]. Moreover, due to the feedforward and oversampling properties, the signal transfer function (STF) of the first loop approximates unity. As depicted in Fig.2, after upsampling the digital output stream of the first stage by 2 and processing the two output streams through the digital cancellation filters, the final output becomes,

$$\begin{aligned} Y_{\text{out}}(z) &= DCF_1(z)Y_1(z^2) - (1/G)DCF_2(z)Y_2(z) \\ &= DCF_1(z)X(z^2) + (1/G)(1 - z^{-1})DCF_2(z)E_2(z) \\ &\quad + [(1 - z^{-2})^2 DCF_1(z) - z^{-3}DCF_2(z)]E_1(z^2) \end{aligned} \tag{6}$$

where $X(z^2)$, $Y_1(z^2)$ are also corresponding products that are upsampled at $F_{S2} = 2F_{S1}$ [18]. To cancel the quantization noise $E_1(z^2)$, the digital filters are chosen to be,

$$DCF_1(z) = z^{-3} \quad DCF_2(z) = (1 - z^{-2})^2 \tag{7}$$

Assuming the perfect cancellation of $E_1(z^2)$, the final output is given by,

$$Y_{\text{out}}(z) = z^{-3}X(z^2) - (1/G)(1 - z^{-1})(1 - z^{-2})^2 E_2(z) \tag{8}$$

where an inter-stage gain G = 3/2 is inserted between two stages, which can further suppress the quantization noise by 3.5dB.

III. Performance Analysis and Comparison

This section first presents the system-level design considerations for the DT 2-1 MASH with the proposed sharing scheme in Fig.2 and subsequently provides analysis, simulations, and comparisons to validate the improved power efficiency of opamps in the proposed architecture.

A. System-Level Design Considerations

In this prototype design, the overall target ENOB is higher than 12 bits for a 5 MHz input signal bandwidth. First, to achieve the desired signal-to-quantization noise ratio (SQNR), the sampling frequency of the first stage is selected to be 120 MHz, thus leading to a sampling frequency of 240MHz in the second stage. Next, considering the thermal noise constraint, the value of the front-end sampling capacitor is chosen to be 700fF. The capacitor size in the following stages is scaled down since their noise contribution is smaller compared with the front end. Furthermore, as depicted in Fig.2, the digital cancellation filters combine the digital outputs of both stages to eliminate the quantization noise of the first stage, which implies an adequate matching between the analog and digital filters for the desired performance. Due to the multirate operating mode, this matching problem becomes more sensitive [3]. As a result, the design for the first stage in this work requires careful consideration.

In reality, the mismatch issue is mainly caused by the non-ideal effects (finite DC gain and GBW) of the opamps as well as capacitor mismatch in the DT MASH $\Delta\Sigma$ modulators. First of all, the finite DC gain requirement of the opamps employed for every active block (integrators and adder) are determined independently. Fig.4 shows the achieved SQNR in the modulator versus the finite DC gain of opamp for different active blocks. As obviously illustrated, the opamp DC gain requirements for the first and second integrators are similar, while almost the same requirements hold for the adder and the third integrator. As a result, to obtain at least 88dB SQNR, the DC gain requirements of $opamp_1$ and $opamp_2$ are determined to be 55dB and 35dB, respectively. Second, with these finite-gain opamps, the requirement of capacitor mismatch is determined by running 100 times Monte Carlo simulation with Gaussian distributed random mismatch in MATLAB. As indicated in Fig.5, a 0.1% coefficient mismatch results in 2 dB degradation of SQNR in the worst case with a few numbers of occurrences. Since it is possible to achieve

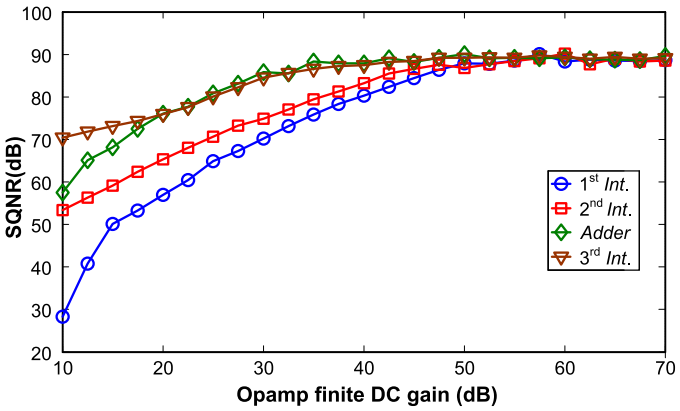

Fig. 4. The SQNR of the modulator versus opamp finite DC gain.

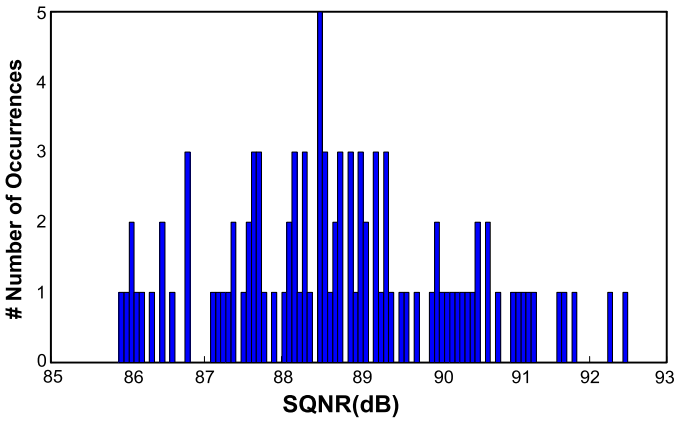

Fig. 5. Monte Carlo simulation with 0.1% capacitor mismatch.

less than 0.1% capacitor mismatch with a careful layout design in the 65nm CMOS process, the matching requirement can be satisfied within the desired resolution with good reliability.

B. Resolution Analysis

As previously illustrated, the multirate solution not only allows the proposed vertical sharing, but also enhances the achievable SQNR further when compared with the single-rate mode. Following (8), the in-band noise (IBN) power (V^2) in the multirate DT 2-1 MASH can be given by,

$$IBN_{MASH} = \left(\frac{1}{G}\right)^2 \frac{\Delta_2^2 \pi^{2L} N^{2L_1}}{12(2L+1)OSR_2^{(2L+1)}} = \left(\frac{1}{G}\right)^2 \frac{\Delta_2^2 \pi^{2L}}{12(2L+1)OSR_1^{(2L+1)} N^{(2L_2+1)}} \quad (9)$$

where L_i and L denote the order of the i^{th} loop and the total order of the system, respectively, Δ_2 represents the quantization step of the second quantizer, OSR_i corresponds to the OSR of the i^{th} loop and N denotes the ratio of the sampling frequency of the second loop to that of the first loop.

As the sampling frequency of the second loop increases by a factor of N ($N > 1$), the IBN power can be further suppressed by,

$$\Delta_{IBN}(dB) = 10(2L_2 + 1)\log_{10} N \quad (10)$$

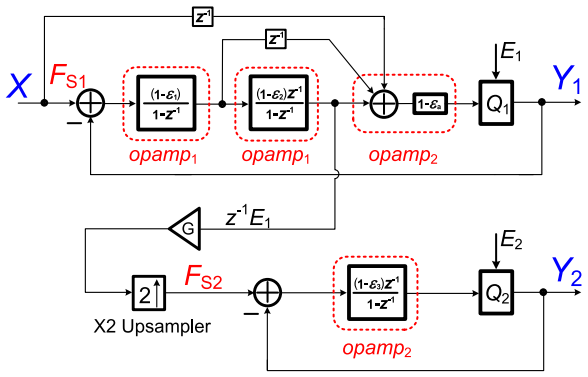

Fig. 6. DT 2-1 MASH with gain errors induced by finite GBW of opamps.

TABLE II
SUMMARY OF EACH OPAMP OUTPUT SWING AND $V_{step,max}$

Active Block	*opamp*	β	V_{pp}(mV)	$V_{step,max}$(mV)
1st *Int.*	$opamp_1$	1/3	312	300
2nd *Int.*	$opamp_1$	1/2	168	200
Adder	$opamp_2$	1/2	720	280
3rd *Int.*	$opamp_2$	2/5	135	350

As observed in (10), higher values of L_2 and N result in a more effective noise shaping. In the proposed architecture, the combination of $L_2 = 1$ and $N = 2$ brings about an additional 9dB quantization noise reduction.

C. Opamp Power Analysis

Next, to verify the enhanced opamp power efficiency in the proposed sharing scheme, the normalized power budget of each independent opamp is derived and compared for the case where the proposed sharing is applicable. Normally, the power consumption of one opamp is mainly determined by the required GBW and SR. The utilization of feedforward topology, multibit quantizers and scaling gains reduce significantly the output swing of the integrators/adder, composed by single-stage opamps (further details shown later). Hence, the maximum step size ($V_{step,max}$) of an opamp's output that can be tolerated without SR limiting is [19]

$$V_{step,max} < SR \cdot \tau \quad \tau = \frac{1}{2\pi \cdot \beta \cdot GBW} \quad (11)$$

By utilizing a specific feedback factor β for each opamp, Table II presents the practical peak-to-peak differential output swing of every opamp (V_{pp}) and calculated $V_{step,max}$. As shown, the V_{pp} of all integrators are similar to their corresponding $V_{step,max}$, while the adder's V_{pp} is much larger than its $V_{step,max}$. Fortunately, the attenuation from the preceding integrators will significantly mitigate the SR requirement of the adder. Thereby, we suppose that the required GBW of each opamp determines its power consumption rather than its SR requirement.

As shown in Fig.6, the finite GBW of opamp exhibits a gain error in the transfer functions of the integrators and the adder [19]. Accordingly, Y_1 and Y_2 in the

z-domain (derived in the Appendix) [20] can be approximately expressed as,

$$Y_1(z) \approx z^{-1}X(z) + (1+\varepsilon_{1st})(1-z^{-1})^2 E_1(z) \tag{12}$$

$$Y_2(z) \approx G \cdot z^{-(N+1)} E_1(z^N) + (1+\varepsilon_{2nd})(1-z^{-1})E_2(z) \tag{13}$$

$$\varepsilon_{1st} = \varepsilon_1 + \varepsilon_2 + \varepsilon_a \quad \varepsilon_{2nd} = \varepsilon_3 \tag{14}$$

where ε_{i} and ε_{a} denote the settling error of the i^{th} integrator and the adder, respectively. It should be noted that the linear settling error of different opamps in the same stage contributes equally to the error in the noise transfer function (NTF), and their sums $\varepsilon_{1\mathrm{st}}$ and $\varepsilon_{2\mathrm{nd}}$ appear as the final gain error of NTF in the corresponding stage. As a result, the E_1 will leak to the final output. After the digital cancellation, the ideal output of the modulator turns into,

$$\begin{aligned} Y_{out}(z) \approx\ & z^{-(N+3)}X(z^N) \\ & -(1/G)(1+\varepsilon_{2nd})(1-z^{-1})(1-z^{-N})^2 E_2(z) \\ & +\varepsilon_{1st} z^{-(N+1)}(1-z^{-N})^2 E_1(z^N) \end{aligned} \tag{15}$$

where the last term corresponds to the E_1 leakage caused by the summing error $\varepsilon_{1\mathrm{st}}$ from the first loop, with a shaping order of $L_1(=2)$. As for $\varepsilon_{2\mathrm{nd}}$, it merely displays a negligible gain error of the original quantization noise E_2. According to (15), the output-referred IBN power (V^2) for E_1 and E_2 can be given by,

$$P_{E_1} = \varepsilon_{1st}^2 \frac{\Delta_1^2 \pi^{2L_1}}{12(2L_1+1)OSR_1^{(2L_1+1)}N} \tag{16}$$

$$P_{E_2} = (1+\varepsilon_{2nd})^2 \left(\frac{1}{G}\right)^2 \frac{\Delta_2^2 \pi^{2L}}{12(2L+1)OSR_1^{(2L+1)}N^{(2L_2+1)}} \tag{17}$$

For each opamp, ignoring the effect of the non-dominant pole, the settling error ε induced by the finite GBW results in,

$$\varepsilon = e^{-k} \quad k = \pi \cdot M \cdot \beta \tag{18}$$

where M denotes the ratio of the opamp's GBW to its corresponding sampling frequency. The larger the k, the smaller the settling error ε will be.

First, as observed in (17), the error $\varepsilon_{2\mathrm{nd}}$ will only slightly affect the ideal resolution as long as it is much smaller than 1. As a result, $k_3 = 3$ is large enough to ignore the effect of $\varepsilon_{2\mathrm{nd}}$ on degrading SQNR (within 0.4dB).

Next, taking the E_1 leakage (the effect of $\varepsilon_{1\mathrm{st}}$) into consideration, and to still preserve the ideal SQNR (within 0.4dB degradation), the following condition must be satisfied,

$$P_{E_1} \le 0.1 \cdot P_{E_2} \tag{19}$$

Since the quantizer bits in both loops are same, by ignoring the effect of $\varepsilon_{2\mathrm{nd}}$ on P_{E2}, the following equation can be obtained,

$$\varepsilon_{1st} \le \left(\frac{1}{G}\right)\left(\frac{\pi}{N \cdot OSR_1}\right)^{L_2} \sqrt{\frac{2L_1+1}{10(2L+1)}} \tag{20}$$

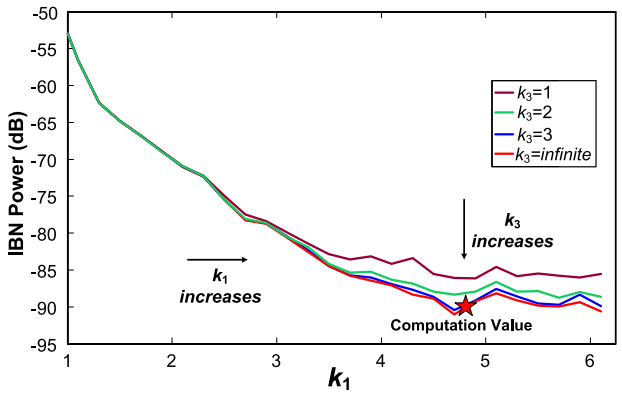

Fig. 7. The total IBN power versus k_1 with different values of k_3.

Supposing that the setting error of each opamp in the first loop is similar ($k_1 = k_2 = k_{\mathrm{a}}$), (20) can be further expressed as,

$$(L_1+1)e^{-k_1} \le \left(\frac{1}{G}\right)\left(\frac{\pi}{N \cdot OSR_1}\right)^{L_2} \sqrt{\frac{2L_1+1}{10(2L+1)}} \tag{21}$$

Rewriting (21), the following criteria can be obtained,

$$k_1 \ge L_2 \ln\left(\frac{N \cdot OSR_1}{\pi}\right) - \ln\left(\sqrt{\frac{2L_1+1}{10(2L+1)}} \cdot \frac{1}{L_1+1} \cdot \frac{1}{G}\right) \tag{22}$$

By substituting $\{N,\ OSR_1,\ L_1,\ L_2,\ L,\ G\} = \{2,\ 12,\ 2,\ 1,\ 3,\ 1.5\}$ in (22), the minimum value of k_1 is obtained to be 4.8 in our case.

Fig.7 shows the total IBN power versus k_1 for different values of k_3, where the simulated values of k_1 and k_3 to obtain the desired resolution correspond well with the above computation. Similarly, we also make derivations for the case of the DT third-order single-loop $\Delta\Sigma$ Modulator with the same CIFF topology to compare to the proposed 2-1 MASH modulator in terms of the opamp power efficiency. For a fair comparison between them, we assume the output swings of the opamps are kept similar in both configurations since a similar output swing guarantees the same opamp structure for every active block (integrators/adder) as well as similar linearity performance. Since the third-order single-loop topology imposes a stability concern, we choose the maximum magnitude of the NTF (H_{inf}) as 2 [2] while keeping the output swings similar to the proposed 2-1 MASH. This increases the in-band quantization noise, and to achieve the same SQNR of 88dB like the proposed 2-1 MASH topology, the OSR needs to increase to 27. Then, by utilizing a specific feedback factor β for each opamp, as shown in Table III, we obtain the GBW requirement for each opamp in both configurations.

Practically, for an opamp with specific topology, combining the given GBW and the corresponding load capacitance C_{L}, the required current drawn by the opamp can be derived. As depicted in Fig.8 (a), since the feedforward architecture and the 4-bit quantizer reduce the output swings, a power-efficient and low-noise telescopic architecture with gain boosting is selected as $opamp_1$ for the first and second integrator to satisfy the high gain requirement. Then, the tail current drawn by this

TABLE III

SPECIFICATIONS OF EACH OPAMP AND THE NORMALIZED CURRENT REQUIRED BY OPAMPS FOR THE PROPOSED 2-1 MASH AND SINGLE LOOP THIRD-ORDER MODULATOR

Configuration	Active Block	*opamp*	k	β	M	F_S(MHz)	GBW(MHz)	C_L(fF)	***Normalized Current***
DT 2-1MASH ΔΣ Modulator	1st *Int.*	$opamp_1$	4.8	1/3	4.6	120	552	720	**7.1**
	2nd *Int.*	$opamp_1$	4.8	1/2	3	240*	720	344	**4.4**
	Adder	$opamp_2$	4.8	1/2	3	240	720	98	**0.8**
	3rd *Int.*	$opamp_2$	3	2/5	2.4	240	576	162	**1**
DT Single-loop Third-order ΔΣ Modulator	1st *Int.*	$opamp_1$	3	1/3	2.9	270	783	320	**4.5**
	2nd *Int.*	$opamp_1$	3	1/2	1.9	270	513	152	**1.4**
	3rd *Int.*	$opamp_2$	3	1/2	1.9	270	513	70	**0.4**
	Adder	$opamp_2$	3	1/3	2.9	270	783	170	**1.4**

*240: Equivalent sampling frequency for *2nd Integrator* due to the reduction of the setting time by half.

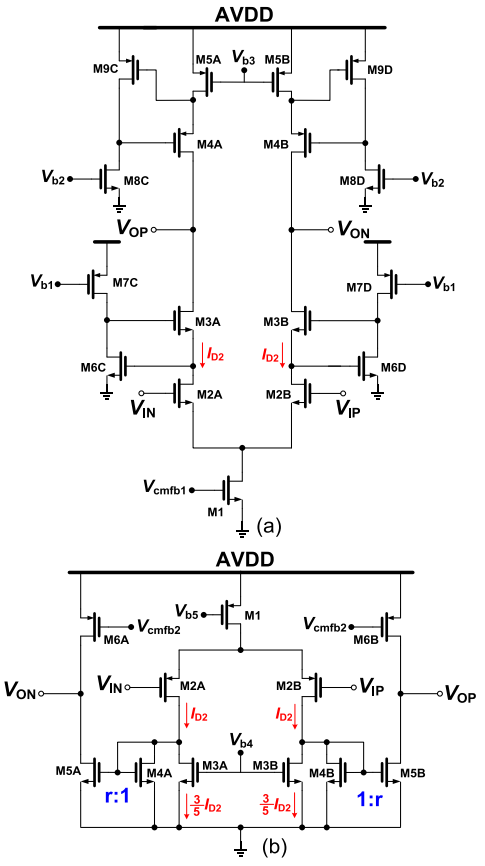

Fig. 8. (a) The topology of the $opamp_1$ for horizontal sharing. (b) The topology of the $opamp_2$ for vertical sharing.

opamp can be expressed as [1],

$$I_{opamp_1} = 2I_{D2} = 2\pi \cdot GBW \cdot V_{ds,sat} \cdot C_L \tag{23}$$

where $V_{ds,sat}$ is the overdrive voltage of the input transistor. Please note that that gain-boosting branches just draw 1/16 of the tail current, which can be negligible. Fig.8 (b) shows that a current mirror opamp with the current starving [1] is implemented as $opamp_2$ which serves as the adder and the third integrator to satisfy the relatively large swing and low-gain requirements. Likewise, with a current mirror gain $r = 5$, the total current consumption of $opamp_2$ yields to be [1],

$$I_{opamp_2} = 6I_{D2} \approx \frac{2\pi \cdot GBW \cdot V_{ds,sat} \cdot C_L}{1.67} \tag{24}$$

Then, combining the foregoing derived GBW requirement, the load capacitance and the specific opamp topology for each active block, Table III presents the normalized current (with respect to the third integrator of 2-1 MASH) required by every active block for both configurations in the last column.

Due to the matching requirement between analog and digital filters, the power of the first two integrators in 2-1 MASH topology is larger when compared with the third-order single-loop modulator. Nevertheless, with the proposed opamp sharing scheme, the total power consumption is almost the same for both architectures. It is noteworthy that horizontal opamp sharing cannot directly be applied between the first and second integrators in the third-order single-loop modulator, otherwise it will give rise to an urgent timing issue for the following blocks, including the third integrator, adder as well as the 4bit quantizer. Moreover, as obviously indicated in Table III, the first integrator is the most power-hungry in both topologies. Owing to the larger $H_{\inf}$ and multirate operation, the sampling frequency of the first integrator in the proposed 2-1 MASH is 2.25 times less when compared with the third-order single loop modulator. This brings considerable advantages to the proposed 2-1 MASH structure over the potential speed limit as the signal bandwidth increases. Considering the timing overhead (including the finite rise, fall and non-overlapping time of clock signals) and parasitic capacitance associated with the input transistor, as its speed requirement approaches technology limit, the power-speed correlation of the first integrator becomes nonlinear, requiring a disproportionately larger power for a desired increase in signal bandwidth [15]. Therefore, the proposed 2-1 MASH topology exhibits higher capability and power-efficiency in the implementation of larger signal bandwidths.

For the proposed multirate 2-1 MASH, the total current consumptions of the first and second integrators are much larger than those of the adder and the third integrator. Moreover, the overall current consumptions of the first and second integrators are relatively comparable, and the same case holds

TABLE IV
CURRENT CONSUMPTION OF OPAMPS AND ACHIEVED SQNR FOR DIFFERENT CONFIGURATIONS OF THE DT 2-1 MASH

Configuration	Active Block	*opamp*	I_{OUT} (uA)	I_{TOT} (uA)	SQNR(dB)
(a) Single-rate DT 2-1MASH F_S=120MHz without opamp sharing	1st *Int.*	$opamp_1$	572	806	79.2
	2nd *Int.*	$opamp_1$	172		
	Adder	$opamp_2$	30		
	3rd *Int.*	$opamp_2$	32		
(b_1) Multirate DT 2-1MASH F_{S1}/F_{S2}=120/240MHz without opamp sharing	1st *Int.*	$opamp_1$	796	1372	88.3
	2nd *Int.*	$opamp_1$	415		
	Adder	$opamp_2$	75		
	3rd *Int.*	$opamp_2$	86		
(b_2) Multirate DT 2-1MASH F_{S1}/F_{S2}=120/240MHz with opamp sharing	1st *Int.*	$opamp_1$	869	967	88.5
	2nd *Int.*				
	Adder	$opamp_2$	98		
	3rd *Int.*				

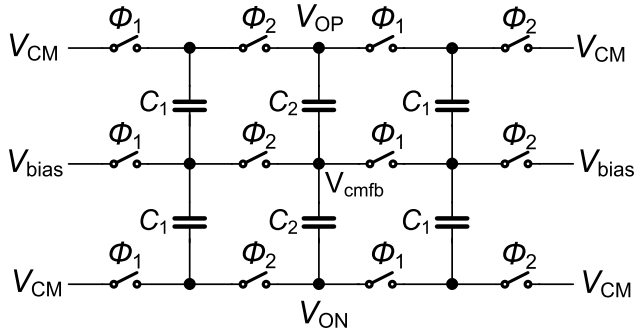

Fig. 9. The DT CMFB configuration for both horizontal and vertical sharing.

for the adder and the third integrator. These observations lead to the conclusion that the proposed sharing technique can effectively improve the opamp power efficiency in the DT MASH modulator.

D. Extraction of Opamp Power and Resolution

Finally, to further validate the above derivations, we perform simulations of transistor-level opamps to extract and compare the current consumption for different configurations: (a) single-rate case, (b_1) multirate case without opamp sharing and (b_2) multirate case with the proposed opamp sharing. The modulator in Fig.2 has been implemented at transistor-level with real opamps and switches in 65nm CMOS, with further details of such DT implementation given in Section IV.

First, considering thermal noise requirements, the capacitive loading for each opamp with a corresponding value is added in the circuit-level simulations. The input sampling capacitors are separated from the DAC capacitors to prevent the signal-dependent leakage into the DAC outputs. Second, as shown in Fig.9, a DT common-mode feedback (CMFB) with symmetric loading [21] is utilized for case (b_2). During every clock phase, the total opamp load capacitance from the CMFB loop is the same. For the case (a) and case (b_1), a simplified DT CMFB is employed. Finally, the minimum current requirement of each opamp in all configurations is found by iteratively decreasing their values until SQNR starts to degrade.

Table IV confirms the simulated minimum current of each opamp as well as the total current consumption for these three configurations. When compared with the single-rate case (a), the SQNR in multirate cases (b_1) and (b_2) is enhanced by 9dB, which matches well with the foregoing analysis. For case (b_1), the normalized current consumption (with respect to the third integrator) for every active block obtained by simulations is 9.26:4.83:0.87:1, which is basically in line with the above derivation (shown in Table III), except for the current consumed by the first integrator that is larger than the calculated value. Nevertheless, it does not affect the enhanced power efficiency of opamps exhibited by the proposed sharing approach. Eventually, the total current consumption of case (b_2) with proposed sharing is 30% lower than that of case (b_1) without opamp sharing.

IV. CIRCUIT IMPLEMENTATION

A. Circuit Level Diagram of the Modulator

Fig. 10 depicts the simplified schematic of the proposed DT 2-1 MASH modulator (single-ended version) with multirate opamp sharing, together with the operating clock phases. To realize the horizontal and vertical sharing scheme, the first stage uses non-delayed and delayed integrators while the second stage employs just one delayed integrator. The first integrator samples the input signal at Φ_1, and conducts the integration during the subsequent Φ_2. Meanwhile, the output of the first integrator is directly sampled by the second integrator in Φ_2 and integrated during Φ_1. The adder is in the summing mode during Φ_3, while the third integrator is active at Φ_{22}. As a result, the horizontal sharing can be applied to the first and second integrator while the adder can vertically share its opamp with the third integrator. All switches with the proper sizes are chosen to ensure their low

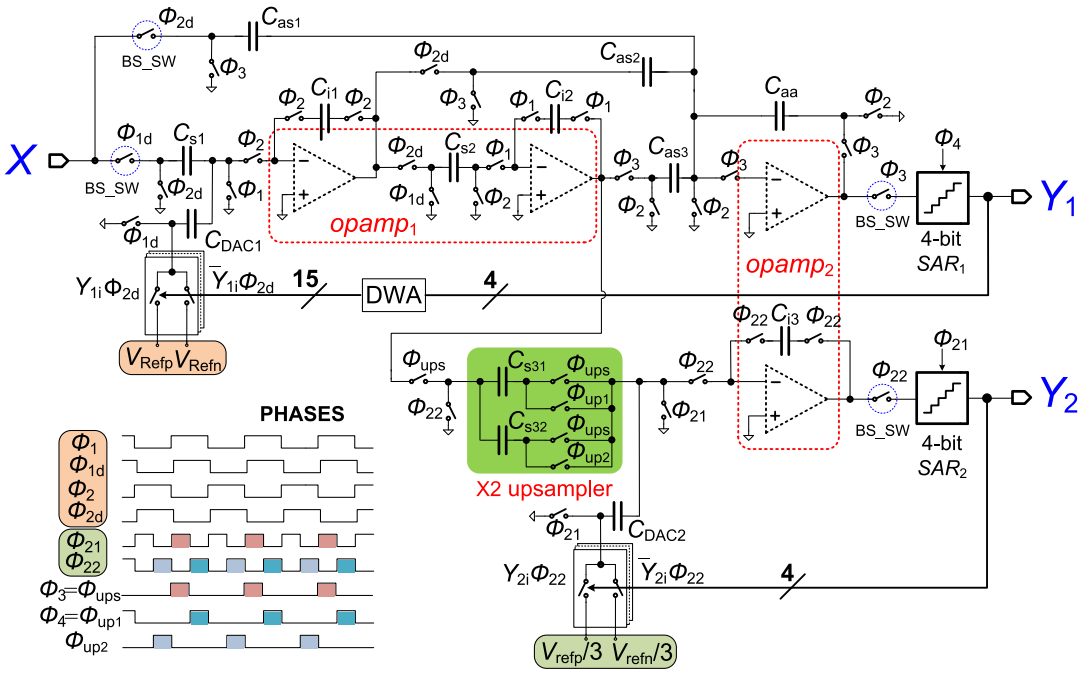

Fig. 10. The implementation of the proposed DT 2-1 MASH with multirate opamp sharing and the operating clock phases.

on-resistance, thus offering enough settling accuracy during the operation time. This modulator employs bottom-plate sampling to reduce the sensitivity to the charge injection and parasitic capacitances. The bootstrapped switches, shown as BS_SW in Fig.10, provides enough sampling linearity for the desired performance in the input sampling network over a wide range of input swing. An X2 upsampler is employed in the sampling front-end of the second stage to interpolate the output of the second integrator by a factor of 2, allowing the multirate operation. During Φ_{ups}, the output of the second integrator is sampled into two equivalent parallel capacitors, C_{s31} and C_{s32}. Subsequently, the samples are successively processed in Φ_{up1} and Φ_{up2} one by one, with two times faster clock of the first stage. Then, upsampling E_1 by a factor of 2 is done.

The two scaling ratios, the inter-stage gain 3/2 and the scaling coefficient 1/3 in series finally combines as 1/2 in the sampling end of the second loop, obtained by a capacitor ratio (accurate enough to avoid the MASH inter-stage error). In order to implement a feedback scaling coefficient of 1/3 and simultaneously define a small value of the feedback capacitor C_{i3} in the third integrator, the references of the DAC in the second stage are scaled by 1/3 while the available minimum unit capacitor is utilized for the second DAC.

B. SAR Quantizer

Synchronous SAR quantizers with a self-timing scheme [22] are employed in both stages of the modulator. As illustrated in Fig.11(a), the self-timing SAR logic consists of a pulse generator, shift registers as well as bit registers. Bootstrapped switches are also applied here to ensure the front-end sampling linearity. To reduce the total capacitance, a split capacitor array DAC is employed as a load of the preceding opamp, which also boosts the settling speed in SARs. Due to the low-resolution and sufficient matching of the fF-level capacitor,

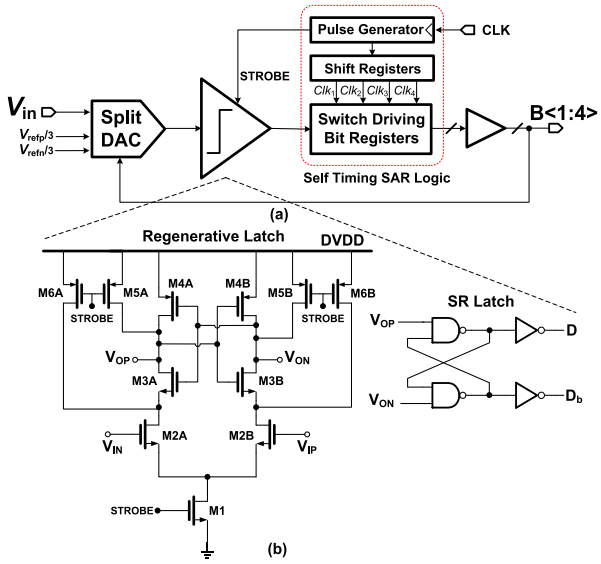

Fig. 11. (a) Block diagram of a 4-bit SAR quantizer with a self-timing scheme. (b) Implementation of the comparator.

this split architecture does not need calibrations for gain error and mismatch. After the sampling, the pulse generator that is a self-trigger inverter chain loop, produces the self-timing strobe signal and activates the shift registers to generate four-phase clocks Clk_1 to Clk_4, switching the bit registers. The pulse generator was tested with process corner variation to guarantee its functional robustness. Unlike the asynchronous scheme, where clock phases for each bit cycle are determined by the preceding bit comparison, this self-timing architecture completely circumvents the possible vanishment of clock phases, caused by the comparator's meta-stability. Thanks to the offset-insensitivity, as depicted in Fig.11(b), the single comparator consists of a regenerative latch and a set-and-reset

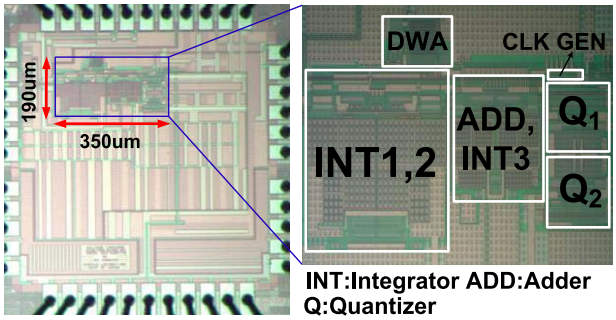

Fig. 12. Chip micrograph.

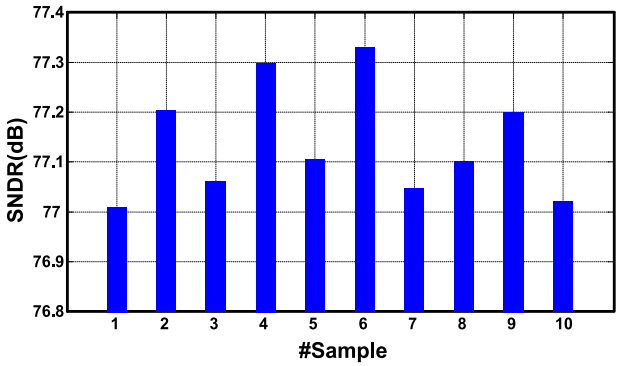

Fig. 13. Measured SNDR over 10 samples with a 690kHz input frequency.

latch without the necessity of employing a preamplifier and auto-zero offset cancellation technique. It results in less power consumption when compared with the flash quantizer.

C. Clock Generator and DWA

The frequency divider divides the high-frequency master clock by 2, generating the low-frequency clock for the first stage. Then, both of them pass through a cross-coupled flip-flop with NAND gates [19] to generate two complementary non-overlapping clock phases as well as their delayed versions, respectively. Φ_{ups}, Φ_{up1} and Φ_{up2} are all produced by combining the corresponding clocks of the first and second stages with NAND gates. The DWA block is employed here to reduce the mismatch errors of the first 4-bit DAC. The binary output from the SAR quantizer is first converted into the thermometer code for the unary feedback. Then, the switching matrix array performs the rotation as the input of the thermometer code with the corresponding index control. Thanks to the technology, the switching matrix array yields a small propagation delay and consumes a little digital power.

V. Experimental Results

The prototype ADC was designed and fabricated in a standard 65nm 1P7M CMOS process, with metal-to-metal (MOM) capacitor option. The chip photograph is shown in Fig.12. It occupies a relatively small active area of 0.066 mm^2. The first and second stage operate at 120MHz and 240MHz, respectively. The digital cancellation filter is implemented off-chip, and an estimated gate count is 300, resulting in less than 100μW digital power, which is negligible compared to the overall power consumption.

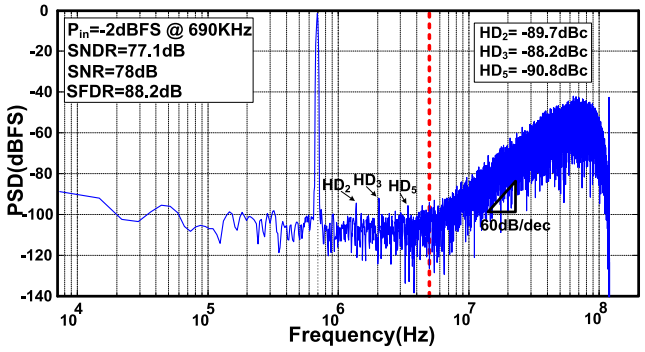

Fig. 14. Measured FFT output spectrum over a 5MHz bandwidth.

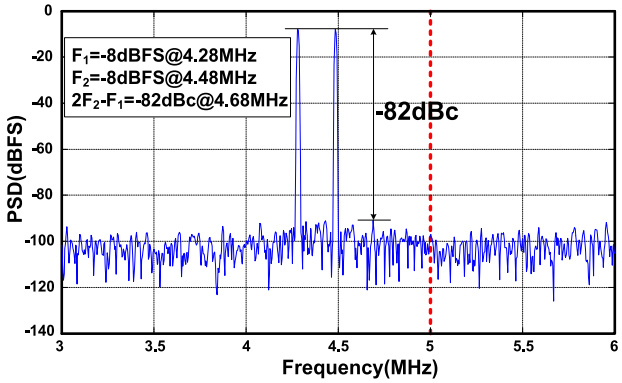

Fig. 15. Measured IMD3 of the $\Delta\Sigma$ modulator output over a 5MHz bandwidth.

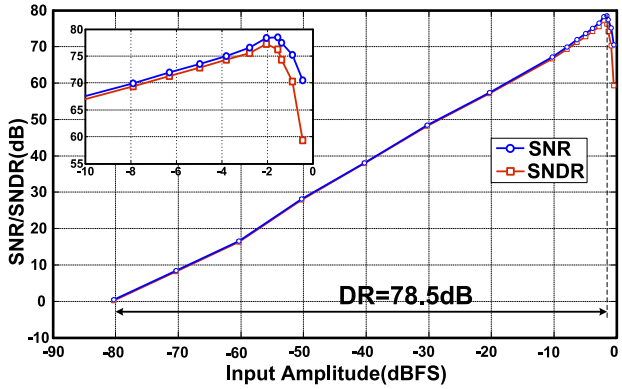

Fig. 16. Measured SNR/SNDR versus input amplitude with a 690kHz input.

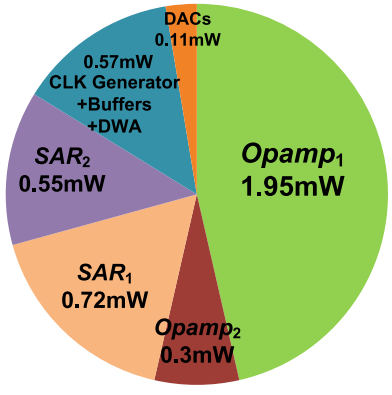

Fig. 17. Modulator power breakdown.

A total of ten chip samples were measured and Fig.13 shows their SNDRs at a 690kHz signal input. The mean SNDR is 77.1dB with a small variation over 10 samples, which

TABLE V
PERFORMANCE SUMMARY AND BENCHMARK WITH THE STATE-OF-THE-ART

	[3]	[7]	[23]	[24]	[25]	[26]	[27]	[28]	[29]	**This Work**
Architecture	DT	DT	DT	DT	CT	CT	CT	CT	CT	**DT**
Technology(nm)	130	130	130	90	28	65	28	28	65	**65**
Supply(V)	1.3/1.4	1.1/1.2	1.2	1.2	0.9/1.8	1	N/A	1.2/1.5	N/A	**1.2**
BW(MHz)	4	5	5	20	5	20	18	50	45	**5**
F_S(MHz)	100/1200	130	80	420	432	2560	640	1800	900	**120/240**
DR(dB)	N/A	78	71.6	N/A	83.9	63	78.1	85	82.5	**78.5**
Peak SNDR(dB)	77	75.7	70.7	70	80.5	61	73.6	74.6	75.3	**77.1**
Power (mW)	13.8	16	8.1	27.9	3.16	7	3.9	78	24.7	**4.2**
Area(mm^2)	0.7	1.6	0.37	1	0.066	0.08	0.08	0.34	0.16	**0.066**
FoM_W* (fJ/conv)	300	320	280	270	36.5	170	27.7	177.7	57.7	**69.7**
***FoM*$_S$** (dB)**	**161.6**	**160.6**	**158.6**	**158.5**	**172.5**	**157.6**	**170.2**	**162.7**	**167.9**	**167.9**

$$^{*}FoM_W = \frac{Power}{2 \cdot BW \cdot 2^{[(SNDR-1.76)/6.02]}} \quad ^{**}FoM_S = SNDR + 10 \cdot \lg(\frac{BW}{Power})$$

verifies that this design is mismatch insensitive. We choose a sample (#8) with a similar SNDR to the mean value to present the following measurement results. Fig. 14 shows the 32K-samples measured output spectrum with −2dBFS input signal at 690kHz. The measured SNDR, SNR and SFDR were 77.1dB, 78dB and 88.2dB, respectively. The achieved 60dB/decade slope of the spectrum validates the desired third-order noise shaping function. Fig.15 depicts a 2-tone test with 4.28MHz and 4.48MHz inputs. The third order inter-modulation distortion (IMD3) is -82dBc with each tone at −8dBFS. Due to the inputs with much higher frequencies in the 2-tone test, the IMD3 is a bit poorer than the HD_3 shown in Fig. 14. Fig. 16 shows the SNR/SNDR versus input amplitudes with a 690kHz input frequency, resulting in the measured DR of 78.5dB. Fig.17 shows the breakdown in power consumption. With a supply voltage of 1.2V for both analog and digital blocks, the total power dissipation is 4.2mW, including 2.6mW analog and 1.6mW digital parts respectively.

Table V summarizes the performance and presents a benchmark with recent state-of-the-art ΔΣ modulators [3], [7], and [23]–[29], which are grouped in DT and CT. For high-resolution data converters, the Schreier FoM_S is more relevant. This design featuring multirate opamp sharing in DT MASH modulator achieves a competitive Schreier FoM_S, especially considering that it is implemented through switch capacitor circuits.

VI. CONCLUSIONS

This paper presented a multirate opamp sharing scheme in the DT MASH modulator for low-power wideband applications. This technique enhances opamps' power efficiency and the overall resolution further through allocating more reasonable settling time based on their various performance requests and capacitive loading. Meanwhile, the stringent timing issue of the first quantizer and DWA caused by the horizontal sharing scheme was correctly addressed, thus allowing the incorporation of a SAR quantizer in the design. The use of a SAR is not only more power and area efficient, but free from the input-referred offset limitations of the quantizer. A DT 2-1 MASH modulator was implemented in 65nm CMOS and tested to verify the effectiveness of the proposed technique. The measurement results show that this modulator achieved the state-of-the-art performance. An SNDR of 77.1dB was achieved in a 5MHz signal BW with 120/240MHz sampling frequency in the first and second stages, respectively, while dissipating a total power of 4.2mW. This results in a Walden FoM of 69.7fJ/conv-step and a Schreier FoM of 167.9dB.

APPENDIX

This appendix provides the detailed derivation of $Y_1(z)$ from the model with the finite GBW of opamps, as shown in Fig.6. $Y_2(z)$ can also be derived similarly. Since the loop filters determine the NTF and STF [2], we can start by deriving the according loop filters. In the first loop, $L_{n1}(z)$ and $L_{s1}(z)$ can be calculated as follows,

$$L_{n1}(z) = \frac{A(z)}{(1-z^{-1})^2} \tag{25}$$

$$A(z) = -(1-\varepsilon_1)(1-\varepsilon_2)(1-\varepsilon_a)z^{-1} - (1-\varepsilon_1)(1-\varepsilon_a)z^{-1}(1-z^{-1}) \tag{26}$$

$$L_{s1}(z) = \frac{B(z)}{(1-z^{-1})^2} \tag{27}$$

$$B(z) = (1-\varepsilon_1)(1-\varepsilon_2)(1-\varepsilon_a)z^{-1} + (1-\varepsilon_1)(1-\varepsilon_a)z^{-1} \times (1-z^{-1}) + (1-\varepsilon_a)z^{-1}(1-z^{-1})^2 \tag{28}$$

First, ignoring the high-order term of ε, $A(z)$ and $B(z)$ can be simplified to,

$$A(z) = -(1-\varepsilon_1-\varepsilon_2-\varepsilon_a)z^{-1} - (1-\varepsilon_1-\varepsilon_a)z^{-1}(1-z^{-1}) \tag{29}$$

$$B(z) = (1-\varepsilon_1-\varepsilon_2-\varepsilon_a)z^{-1} + (1-\varepsilon_1-\varepsilon_a) \times z^{-1}(1-z^{-1}) + (1-\varepsilon_a)z^{-1}(1-z^{-1})^2 \tag{30}$$

Then $NTF_1(z)$ can be given by,

$$NTF_1(z) = \frac{1}{1 - L_{n1}(z)} = \frac{1}{1 - \frac{A(z)}{(1-z^{-1})^2}} = \frac{(1-z^{-1})^2}{C(z)} \quad (31)$$

$$\begin{aligned} C(z) &= (1-z^{-1})^2 - A(z) \\ &= 1 - (2\varepsilon_1 + \varepsilon_2 + 2\varepsilon_a)z^{-1} + (\varepsilon_1 + \varepsilon_a)z^{-2} \end{aligned} \quad (32)$$

Furthermore, (32) can be represented by its Talyor-series expansion around z = 1:

$$\begin{aligned} C(z) = 1 &- (\varepsilon_1 + \varepsilon_2 + \varepsilon_a) + \varepsilon_2(1 - z^{-1}) \\ &+ (\varepsilon_1 + \varepsilon_a)(1 - z^{-1})^2 \end{aligned} \quad (33)$$

As observed in (33), the first and second term are dominant since the highpass filtering shapes the last two terms. Then, $C(z)$ can be approximately expressed as,

$$C(z) \approx 1 - (\varepsilon_1 + \varepsilon_2 + \varepsilon_a) \quad (34)$$

Combining (31) and (34), $NTF_1(z)$ will become,

$$\begin{aligned} NTF_1(z) &\approx \frac{(1-z^{-1})^2}{1 - (\varepsilon_1 + \varepsilon_2 + \varepsilon_a)} \\ &\approx [1 + (\varepsilon_1 + \varepsilon_2 + \varepsilon_a)](1 - z^{-1})^2 \end{aligned} \quad (35)$$

Also, combining (27) and (35), $STF_1(z)$ can be calculated as,

$$\begin{aligned} STF_1(z) &= \frac{L_{s1}(z)}{1 - L_{n1}(z)} \\ &= \frac{B(z)}{(1-z^{-1})^2} \cdot [1 + (\varepsilon_1 + \varepsilon_2 + \varepsilon_a)](1 - z^{-1})^2 \\ &= [1 + (\varepsilon_1 + \varepsilon_2 + \varepsilon_a)] \cdot B(z) \end{aligned} \quad (36)$$

Ignoring the last two terms with high pass filtering of $B(z)$ in (30) within band of interest, then $STF_1(z)$ becomes,

$$STF_1(z) = [1 - (\varepsilon_1 + \varepsilon_2 + \varepsilon_a)^2]z^{-1} \approx z^{-1} \quad (37)$$

As a result, $Y_1(z)$ can be finally approximated by,

$$\begin{aligned} Y_1(z) &\approx z^{-1}X(z) + (1 + \varepsilon_{1st})(1 - z^{-1})^2 E_1(z) \\ \varepsilon_{1st} &= \varepsilon_1 + \varepsilon_2 + \varepsilon_a \end{aligned} \quad (38)$$

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