A Reconfigurable Cross-Connected Wireless-Power Transceiver for Bidirectional Device-to-Device Wireless Charging

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***Abstract*— This paper presents a reconfigurable cross-connected (CC) wireless power transceiver (TRX) operating at 6.78 MHz and implemented for bidirectional device-to-device (D2D) charging with high efficiency and small system volume. We propose, for the first time, a CC topology applied to a differential class-D power amplifier for significant switching loss reduction. Two delay-locked loops (DLLs) for each power NMOS transistor form the reconfigurable controller, realizing the adaptive deadtime control in the transmitter (TX) mode and the off-delay compensation in the receiver (RX) mode, leading to high power conversion efficiency and safe operation. To realize the inductive load for the TX mode in the whole coupling range at the resonant frequency, we use an on-chip tunable capacitor. Furthermore, we also study the power link efficiency in the D2D direct charging system and verify that the near-maximum power link efficiency can be inherently achieved in this scenario. The proposed wireless power TRX, fabricated in a 0.35-μm CMOS process with 5-V devices, measured a peak D2D total efficiency of 77.2% when the output power is 0.7 W. The maximum charging power is 2.74 W with a total efficiency of 62.7% and the maximum transmission distance is 24 mm, both measured.**

***Index Terms*— Adaptive deadtime control, delay-locked loop (DLL), off-delay compensation, reconfigurable cross-connected (CC) wireless power transceiver TRX, tunable capacitor, zero-voltage switching (ZVS) turn-on.**

I. Introduction

In RECENT years, wireless power transfer (WPT) via inductive coupling has become a popular subject for various applications [1]–[3]. It not only provides a convenient power source to power-consuming devices but also contributes to simpler waterproof and dustproof designs by removing their power ports. Recently, the bidirectional WPT (BD-WPT) is gaining more attention [4]–[6], because it enables dynamic and flexible power allocation among different objects.

The BD-WPT systems have been designed for the electric vehicles (EVs) to realize the vehicle-to-grid (V2G) power transfer such that they can supply the energy back to the grid, acting as an emergency power source [4], [5]. In high-power BD-WPT systems, discrete n-type power transistors are commonly used for both the high-side and low-side switches and they operate at low frequencies (tens of kHz) for lower power losses. However, the discrete power transistors are bulky and relatively expensive, which is not favorable for consumer electronics. In addition, level shifters are necessary for driving the high-side n-type power transistors, which increase circuit complexity and demand for special high-voltage process steps.

In [6], a BD-WPT TRX with direct charging operation was applied to realize the device-to-device (D2D) wireless charging for consumer electronics. The high-side power transistors are p-type, reducing the complexity of the driving circuits with no off-chip/large capacitors. All the power transistors, buffers, and control circuits are integrated on-chip. To shrink the system size, it works at a high frequency of 6.78 MHz. However, the switching loss increases proportionally with the switching frequency, thus sacrificing power efficiency. In addition, the timing control in [6] is not ideally optimized, and the power losses caused by the possible shoot-through current also increase with the switching frequency. Therefore, the total BD-WPT efficiency in [6] is relatively low, which also limits the maximum output power due to the thermal issue.

In this paper, to solve the tradeoff between the volume and the power efficiency of the BD-WPT system, we apply a cross-connected (CC) topology, for the first time, to the differential class-D PA [7]. In addition, to ensure the proper operation of the CC differential class-D PA, we propose a dedicated control scheme for the optimization of the switch timing. Based on the CC topology, we design a reconfigurable CC wireless power TRX for the D2D wireless charging. We also analyze the power link efficiency in this paper, where we find that the near-maximum link efficiency can be inherently achieved with two identical coils, without any active control schemes or extra components. With the highly efficient reconfigurable CC wireless power TRX and power link, this paper achieves a high D2D total efficiency.

The structure of this paper is organized as follows. Section II introduces the architecture of the proposed BD-WPT TRX and the operation principle of the CC differential class-D PA.

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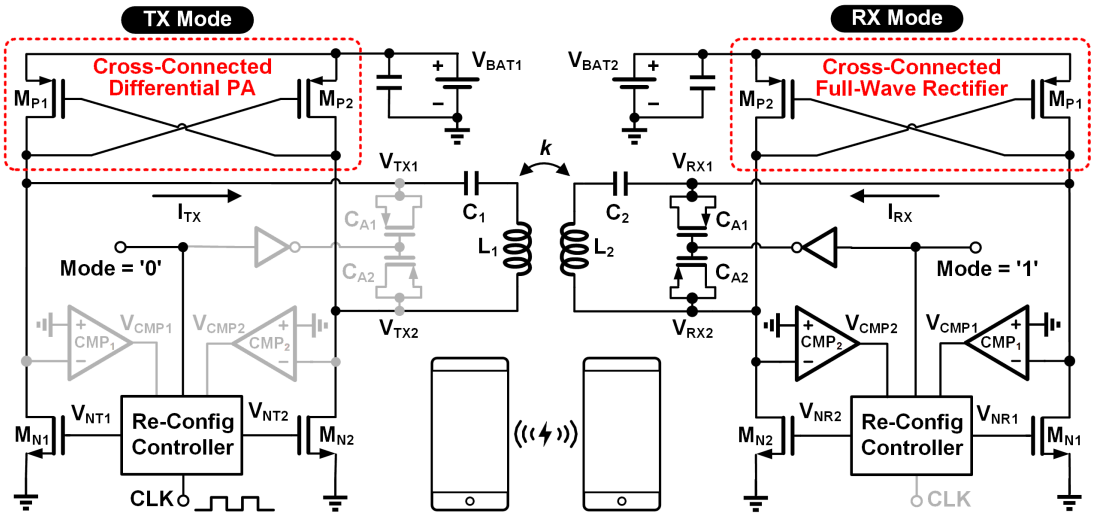

Fig. 1. D2D direct charging system with the proposed CC reconfigurable wireless power transceiver.

Section III shows the circuit implementation of the proposed BD-WPT TRX. Section IV analyzes the wireless power link efficiency. Then, Section V presents the measurement results, and finally, Section VI draws the conclusions.

II. Proposed Reconfigurable CC Wireless Power Transceiver

A. System Architecture

Fig. 1 shows the D2D direct charging system with two proposed reconfigurable CC wireless power TRXs. To charge the battery V_{BAT2} wirelessly, the left TRX is configured to the transmitter (TX) mode, which is a CC differential class-D PA, while the right TRX is configured to the receiver (RX) mode, which is a CC full-wave rectifier. The primary and secondary coils, L_1 and L_2, are series resonant with C_1 and C_2, respectively, for large space freedom. We used the reconfigurable controller in Fig. 1 to provide the optimal switch timing for M_{N1} and M_{N2} and the PMOS capacitors C_{A1} and C_{A2} to obtain an inductive equivalent load for the CC differential class-D PA. The 1-bit mode selection signal *Mode* controls the switch timing selection and the value of C_{A1} and C_{A2}. In this D2D direct charging system, the total efficiency, η_{Total}, can be given by

$$\eta_{Total} = \eta_{PA} \cdot \eta_{Link} \cdot \eta_{RECT} \tag{1}$$

where η_{PA}, η_{Link}, and η_{RECT} are the efficiencies of the CC differential class-D PA, power link, and CC full-wave rectifier, respectively.

With the CC structure, the parasitic gate capacitors of M_{P1} and M_{P2} can be part of the *LC* tank, and thus, most of the gate-drive energy is cycling between each other, ideally with no loss. In other words, the gate of M_{P1} and M_{P2} can swing to "1" when the energy is transferred from the *LC* tank to the gate capacitors and can swing back to "0" when the energy goes back to the *LC* tank. This allows us to use larger power PMOS transistors for smaller conduction loss without inducing switching loss and thus significantly improving the power efficiency. Another advantage of the CC structure in the TX mode is that it no longer needs the buffers and multiplexers in [6] for the driving of power PMOS, saving silicon area and reducing circuit complexity.

We selected the switching frequency of 6.78 MHz, rather than kHz in the EV applications or in the Qi standard, for reducing the sizes of L_1 and L_2, and their series-resonant capacitors, C_1 and C_2. Therefore, the system volume can be much smaller. In addition, L_1 and L_2 can be realized with the printed spiral coils, which provide more flexibility in optimizing the geometry and aspect ratio [8], and are attractive for portable/wearable devices with various shapes and sizes.

To achieve safe charging and obtain a full capacity, constant-current and constant-voltage charging methods are widely used for Li-ion battery charging. However, in the targeted D2D wireless charging application, the charging current can hardly reach the battery maximum current rating. Therefore, the maximum charging current mode (MCCM) in [6] is adopted in this paper. For the pad-to-device charging application, other single-stage regulating rectifier techniques, such as in [9] and [10], can be employed for constant-current and constant-voltage modes, but the charging speed is significantly limited by the low V_{RECT} which demands high RX current.

B. Operation Principle of the CC Differential Class-D PA

Fig. 2(a) shows the schematic of the CC differential class-D PA with the delay-locked loop (DLL)-based reconfigurable controller and its equivalent load impedance Z_{EQ}. C_{P1} on V_{TX1} includes the gate capacitor of M_{P2} and also the junction drain capacitors of M_{P1} and M_{N1}, a similar case for C_{P2}. As mentioned earlier, in the proposed CC structure, M_{P1} and M_{P2} are turned on/off by exchanging the energy with the *LC* tank to reduce the switching loss, which means that C_{P1} and C_{P2} should be charged or discharged by I_{TX}, rather than by the dc potentials (the battery and the ground). Otherwise, large power losses will occur.

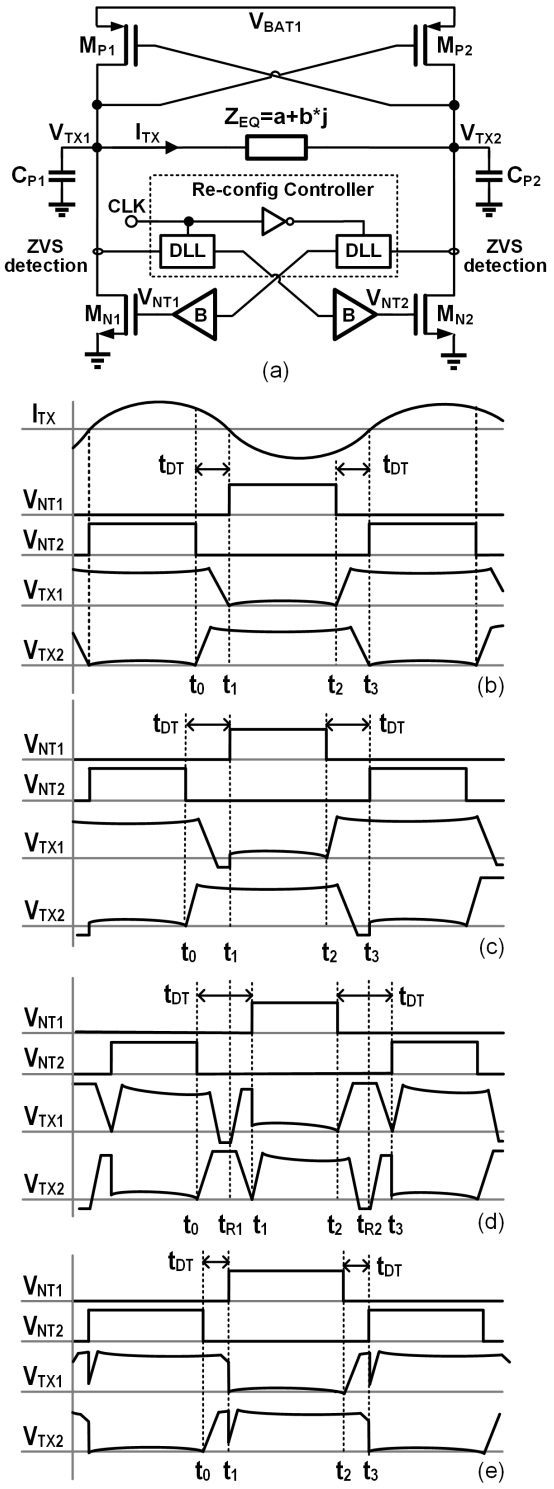

Fig. 2. (a) Schematic of the CC differential class-D PA. Waveforms of the main signals with (b) proper deadtime, (c) slightly larger deadtime, (d) too large deadtime, and (e) smaller deadtime.

Fig. 2(b) shows the desired V–I waveforms. Before t_0, M_{P1} and M_{N2} are on and M_{P2} and M_{N1} are off, and the direction of I_{TX} is from V_{TX1} to V_{TX2}. At t_0, M_{N2} is turned off and I_{TX} is still larger than 0. With both M_{P2} and M_{N2} off, I_{TX} will charge C_{P2} to "1," and thus, M_{P1} will be turned off. With both M_{P1} and M_{N1} off, C_{P1} will be discharged to "0" by I_{TX}, and then, M_{P2} will be turned on at t_1. Here, t_1 is the optimal timing to turn on M_{N1} for two reasons. First, M_{P1} has been turned off before t_1 and no shoot-through current will occur when M_{N1} is turned on. Second, M_{N1} is turned on with zero-voltage switching (ZVS) at t_1, and thus, there is no switching loss at the node of V_{TX1}. The process from t_2 to t_3 is similar, and t_3 is the optimal timing to turn on M_{N2}. The time duration, t_{DT}, from t_0 to t_1 and from t_2 to t_3 in Fig. 2(b), is the proper deadtime between V_{NT1} and V_{NT2}. During t_{DT}, all the power transistors are efficiently turned on/off under ZVS conditions, and both M_{P1} and M_{P2} are driven by the inductor current I_{TX}. Thus, the only switching loss is for driving the power NMOS that usually has a smaller size than that of a power PMOS, and the switching loss is also considerably small. Then, the proposed CC differential class-D PA achieves high power efficiency at high frequency.

Fig. 2(c) shows the case that t_{DT} is slightly larger than the optimal deadtime. In this case, V_{TX1} and V_{TX2} will be discharged to $-V_{thn}$ and the n-type power transistors will operate as diodes for a short time. However, the near-ZVS operation is obtained, and the conduction loss caused by the diode operation is small because during which I_{TX} is near zero. Then, the power efficiency will be only slightly degraded, which is sub-optimum but acceptable.

Fig. 2(d) shows the case where the deadtime is much larger than the optimum. At t_{R1}, I_{TX} changes its direction, then V_{TX1} falsely goes back to "1," and V_{TX2} goes back to "0." Then, when M_{N1} turns on at t_1, M_{P1} is on, and thus, a large shoot-through current and a large switching loss will occur.

Fig. 2(e) shows the occurrence when t_{DT} is too small. From t_0 to t_1, V_{TX2} is charged to "1" by I_{TX}. However, when M_{N1} turns on at t_1, V_{TX1} is still high. Therefore, C_{P1} is discharged by M_{N1} and large switching loss happens. In addition, as the discharging current provided by M_{N1} is large, the sharp falling edge (FE) of V_{TX1} can be coupled to V_{TX2} by the gate-to-drain capacitors of both M_{P1} and M_{P2}. Therefore, a short time interval will appear after t_1 when both M_{P1} and M_{N1} are on, introducing a shoot-through current. Then, this case should also be avoided.

As discussed earlier, the deadtime between V_{NT1} and V_{NT2} has a significant influence on the power efficiency. As the deadtime is taken to charge or discharge C_{P1} and C_{P2}, the proper deadtime is sensitive to the I_{TX} amplitude, the value of V_{BAT1}, and the capacitances of C_{P1} and C_{P2}. Thus, we design the reconfigurable controller to adaptively tune the deadtime.

Two DLLs compose the reconfigurable controller, which do the ZVS detection and control the switching timing accordingly. The tuning of t_{DT} can be realized by tuning the FE or rising edge of V_{NT1} and V_{NT2}. Considering that the off-delay compensation in the RX mode can only be realized by the FE tuning, to reuse the DLLs in the RX mode, we select here the FE tuning. From the waveforms in Fig. 2, we can deduct that the FE of V_{NT2} determines the ZVS turn-on of V_{NT1}. Therefore, the timing of V_{NT2} should be controlled by the left DLL and vice versa, as shown in Fig. 2(a).

Besides the proper deadtime, another necessary condition for the ZVS turn-on of M_{N1} and M_{N2} is to have an inductive load Z_{EQ}. With an inductive load, the output voltage will lead

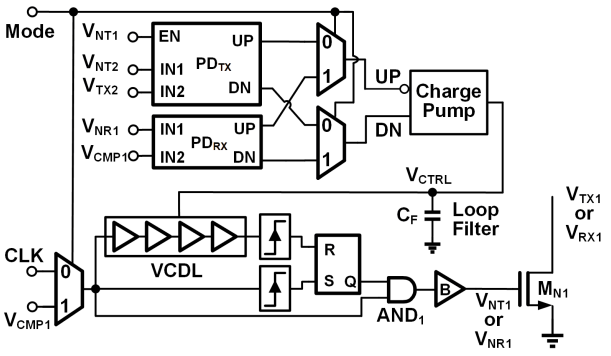

Fig. 3. Half of the DLL-based reconfigurable controller.

to the output current. As shown in Fig. 2(b), the phase of I_{TX} lags behind that of the output voltage $V_{TX1} - V_{TX2}$. If they are in phase, I_{TX} will reverse its direction in the middle of the deadtime, no matter how much t_{DT} is. Then, V_{TX1} and V_{TX2} cannot swing to "1" or "0" at the end of the deadtime. The realization of inductive Z_{EQ} will be introduced next.

III. Circuit Implementation

A. Reconfigurable Controller

We used the reconfigurable controller to determine the deadtime in the TX mode and to compensate the off-delay of M_{N1} and M_{N2} in the RX mode. With the CC topology, the deadtime control in the TX mode is different from the conventional controller, as M_{P1} and M_{P2} are now self-driven, and thus, we can only control the n-type power transistors.

The dynamic deadtime control with an open loop has been explored before [11]–[14]. The ZVS condition can be detected by a comparator [11] and body diode [12], [13], and the power transistors can be turned on only after the detection of ZVS. However, the accuracy of these ZVS operations is low because of the comparator and buffer delays, especially when the switching frequency is high. In addition, V_{TX1} and V_{TX2} may not be discharged to zero when I_{TX} is small, implying that the deadtime control circuits in [11]–[13] are not applicable here. A possible solution is to use a slope-sensing ZVS detector [14] to realize the near-optimum deadtime control even when I_{TX} is small, but the slope-sensing delay is of concern to operate at a high frequency such as 6.78 MHz.

To solve the above-mentioned problems, we built a DLL-based adaptive deadtime control scheme in the reconfigurable controller. Fig. 3 shows half of the controller for deciding the switch timing of M_{N1}, with the other half mirrored. We realized the ZVS detection with logic gates for short delay time by detecting the phase difference between the FE of V_{TX2} and the rising edge of V_{NT2}. Then, the charge pump (CP) will transform the phase difference into the control voltage of the voltage-controlled delay line (VCDL), V_{CTRL}. Thus, the FE of V_{NT1} can be aligned by the delay time of the VCDL, t_{VCDL}. When the feedback loop gets stable, the ZVS operation can be executed no matter what the delay time of the buffer is. In this control loop, we have a dominant pole compensation implemented with the CP integrator, which has a low-frequency dominant pole. On the other hand, the

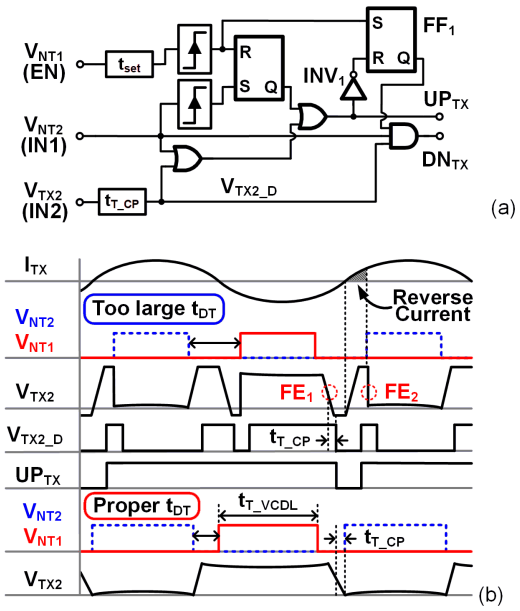

Fig. 4. (a) Schematic of the phase detector PD_{TX} and (b) its timing diagram.

DLL processes the control voltage and immediately converts it into delay. Therefore, the DLL does not add any pole to the loop, as discussed in detail in [15]. The delay directly decides the voltage sampling point, which means that the delay is also immediately converted into voltage. Thus, as long as the loop unity-gain frequency is several times lower than the sampling frequency which is the wireless power transmission frequency, we can linearize and model the loop as a single-pole system.

During the start-up process, t_{VCDL} may be larger than half of the operation period, $T/2$. In the RX mode, M_{N1} and M_{N2} will turn on/off with large I_{RX}, resulting in large di/dt noise. In the TX mode, all the four power transistors will turn on simultaneously for a time duration of $t_{VCDL} - T/2$, resulting in a very large shoot-through current. To protect the power transistors and have a smooth start-up process, we added the logic gate AND_1 in Fig. 3 to limit the duty cycle of V_{NT1} and V_{NR1} to a value smaller than 0.5.

Fig. 4(a) shows the schematic of PD_{TX}, and Fig. 4(b) shows the timing diagrams with too large t_{DT} and proper t_{DT}, where t_{T_VCDL} is the delay time of the VCDL in the TX mode. Due to the finite FE of V_{TX2} and V_{NT2}, there is a phase difference, t_{T_CP}, between V_{TX2} and V_{NT2} when the proper deadtime t_{DT} is achieved, as shown in Fig. 4(b). Therefore, V_{TX2} is compensated with a delay of t_{T_CP} first before the phase difference is detected. However, as explained in Section II, there will be two FEs during the deadtime if the deadtime is too large, FE_1 and FE_2, as shown in Fig. 4(b). PD_{TX} will be misled by FE_2 and generate a DN_{TX} with the pulsewidth of t_{T_CP}, which will increase t_{DT}. To solve this problem, DN_{TX} is locked at "0" by the logic gate INV_1 and the RS flip-flop FF_1 when UP_{TX} ="0," and it will be unlocked in the next half cycle when V_{NT1} is high.

As t_{T_CP} raises from the FE of V_{TX2}, it is vulnerable to process, voltage, temperature, and also the magnitude of I_{TX}. Therefore, it is very hard to obtain the exact value of t_{T_CP}. However, to achieve high efficiency, we do not need

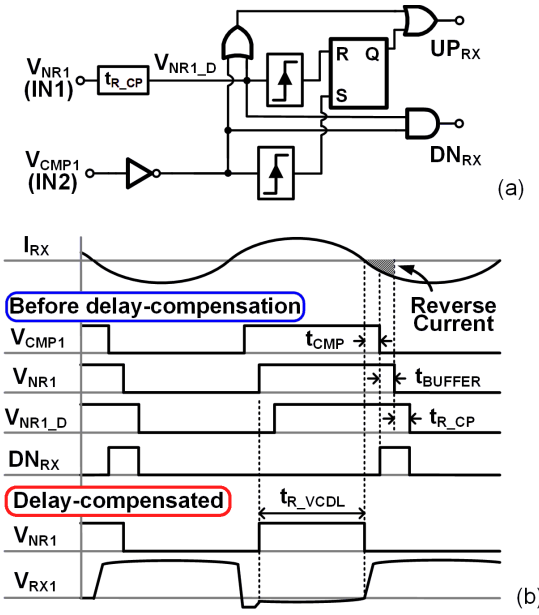

Fig. 5. (a) Schematic of the phase detector PD_{RX} and (b) its timing diagram.

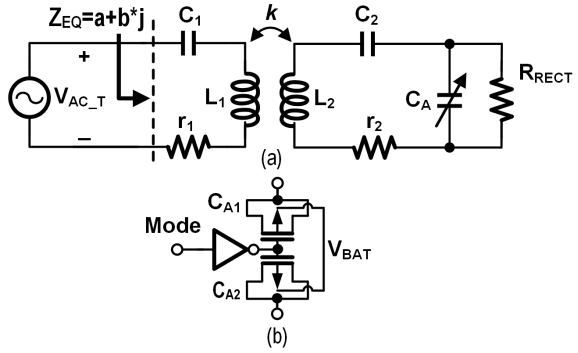

Fig. 6. (a) Proposed solution to provide an inductive Z_{EQ}. (b) Implementation of C_A.

a high compensation accuracy of t_{T_CP}. For example, if t_{T_CP} is slightly over-compensated, the cases shown in Fig. 2(c) will happen, and basically, the power efficiency will not be degraded. In this paper, to reduce the circuit design complexity, we implemented t_{T_CP} with standard delay cells with a delay of 5 ns to 2.5 ns when the battery voltage varies from 2.5 to 4.2 V.

For the RX mode, only the phase detector, PD_{RX}, needs to be designed separately, while all the other circuit blocks are reused. Fig. 5 shows the schematic of PD_{RX} and its timing diagram. Here, V_{CMP1} experiences the comparator delay; therefore, in order to have V_{NR1_D} approximately matched with V_{CMP1}, an artificial delay t_{R_CP} also implemented with an inverter chain has been added to V_{NR1}. t_{R_CP} does not need to exactly match to t_{CMP}, because the conduction time of the rectifier operating with the series-resonant LC tank is relatively long. After that, we compare the phase difference between the FEs of V_{CMP1} and V_{NR1_D} and represent it through the pulsewidth of DN_{RX}. Although other sample-and-hold-based method, such as in [16], can provide high accuracy delay control in the parallel-resonant case, it is quite difficult to apply it in the series-resonant case, as the ac voltages change very fast with a series-resonant tank which is considered as a current source.

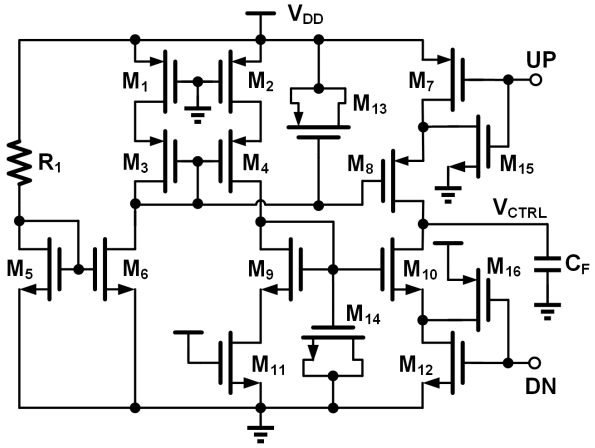

Fig. 7. Schematic of the CP and loop filter.

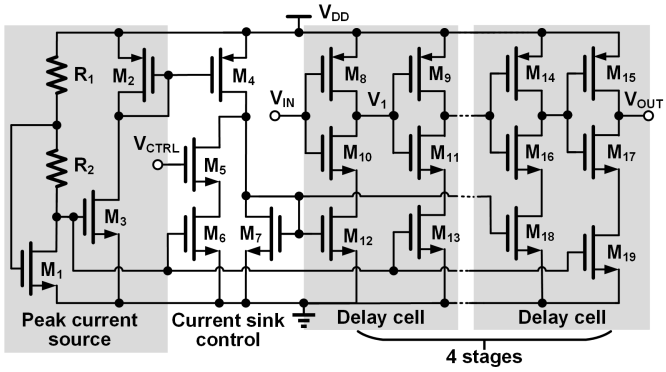

Fig. 8. Schematic of the VCDL.

B. Inductive Load for the CC Differential Class-D PA

An inductive equivalent load impedance is the essential condition for the ZVS operation of the CC differential class-D PA. Here, to realize the inductive load, we connect an on-chip variable capacitor C_A in parallel with R_{RECT}, as shown in Fig. 6(a). The voltage source V_{AC_T} is used to stand for the CC differential class-D PA. R_{RECT} is the input impedance of the rectifier and Z_{EQ} is the equivalent load of PA. C_A introduces a capacitive load to L_2C_2 and the capacitive load is transformed to inductive Z_{EQ} in the whole range of k when operating at the resonant frequency. When ignoring r_1 and r_2, Z_{EQ} can be given by

$$Z_{EQ} = \frac{k^2\omega_{RES}^2 L_1 L_2}{R_{RECT}}\left(1 + j\frac{R_{RECT}}{|Z_{CA}|}\right) \tag{2}$$

where ω_{RES} is the resonant frequency of L_1C_1 and L_2C_2 and $|Z_{CA}|$ is the magnitude of the impedance of C_A. Equation (2) shows that the imaginary part of Z_{EQ} is always larger than 0 only if k is larger than 0. Therefore, the proposed solution is effective in the whole k range. In [17], the inductive load is obtained by operating the PA at the frequency ω_{OP} above the resonant frequency ω_{RES}, without any additional hardware.

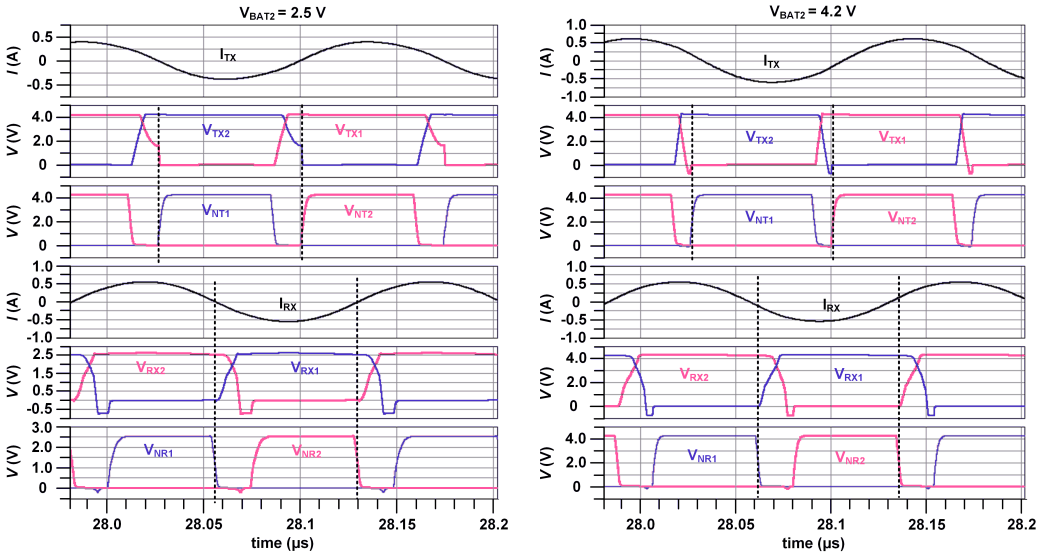

Fig. 9. Simulated waveforms when $k = 0.2$, $V_{BAT1} = 2.5$ V, and $V_{BAT1} = 4.2$ V.

However, it is only in effect when k is smaller than a critical value, k_c. In [18], the parallel LC tank is used to realize the inductive load. This solution is effective in the whole k range. However, it increases the number of off-chip components and system volume. In this paper, C_A is realized with two series-connected PMOS capacitors C_{A1} and C_{A2}, as shown in Fig. 6(b), with the body connected to the battery voltage that is the highest dc voltage in the circuit. Because C_{A1} and C_{A2} are placed in the layout space margins of the power transistors, they do not increase the chip area.

It should be noticed that C_A causes the resonant frequency shift at the secondary side of the power link and reduces the current that goes into the rectifier. In other words, C_A decreases the power factor of the RX side. Therefore, $|Z_{CA}|$ should be several times larger than R_{RECT}. After extensive transistor-level simulations, we select C_A around 300 pF. In the TX mode, C_A is unwanted because it adds capacitive load to Z_{EQ}. Thus, C_A should be tunable. In this design, C_A is composed of two series-connected PMOS capacitors C_{A1} and C_{A2}, as shown in Fig. 6(b), with the body connected to the battery voltage that is the highest dc voltage in the circuit. When the mode selection signal, *Mode*, changes the gate voltage of C_{A1} and C_{A2}, the capacitance can be tuned. In the TX mode, *Mode* = "1" and the capacitance of C_A is about 6 pF.

C. Charge Pump and Loop Filter

Fig. 7 shows the schematic of the CP and the loop filter. Together with the PD, the CP forms a tri-state phase detection circuit. The schematic of the CP is similar to that in [19]. In this design, the battery voltage supplies the CP varying from 2.5 to 4.2 V, causing the bias current provided by R_1 and M_5 to vary from 2.0 to 4.2 μA. Therefore, the CP was carefully designed to work properly within the supply voltage and the bias current range. The pump current varies from 7.2 to 12 μA within the supply voltage range. The MIM capacitor C_F of the loop filter is 8 pF.

D. Voltage-Controlled Delay Line

Fig. 8 shows the schematic of the VCDL. We utilized the analog VCDL for large and continuous delay time. A peaking current source (PCS), a current sink control circuit, and four stages of delay cells compose the VCDL that has V_{IN} as its input. According to Fig. 3, the VCDL input is either *CLK* or the output of the comparators, with only the rising edge of the output voltage of the VCDL used. Therefore, we only control the delay time of the input V_{IN} rising edge. When V_{CTRL} increases and turns on M_5, the current through M_7, M_{12}, and M_{13} decreases and the V_{IN} rising edge delay time increases. Due to the slow FE of V_1, M_9 and M_{11} turn on simultaneously for a long time. To reduce the power consumption, we added M_{13} to limit the current through M_9 and M_{11}. The VCDL is supplied by the battery voltage ranging from 2.5 to 4.2 V. To have the VCDL's delay time less sensitive to the battery voltage variation, we used the PCS to provide a bias current that is proportional to V_{DD} rather than a supply-insensitive current.

E. Simulation Results

Fig. 9 shows the simulated steady-state waveforms of the wireless power TRX at different values of V_{BAT2} with coupling coefficient $k = 0.2$ and $V_{BAT1} = 4.2$ V. On the TX side, we obtained the proper deadtime between V_{NT1} and V_{NT2}. When V_{BAT2} is 2.5 V, V_{TX1} and V_{TX2} are higher than zero but much smaller than 4.2 V when M_{N1} and M_{N2} turn on. Therefore, only small switching loss is introduced, and the efficiency of the CC differential class-D PA remains as high as 96.5%. When V_{BAT2} is 4.2 V, M_{N1} and M_{N2} are turned on with ZVS, and the simulated PA efficiency is 96.6%.

On the RX side, when V_{BAT2} is 2.5 V, M_{N1} and M_{N2} turn off when I_{RX} is around 0 A, so the off-delay is fully compensated. The simulated efficiency of the rectifier is 91.4%, while the main loss comes from the conduction loss due to the low gate

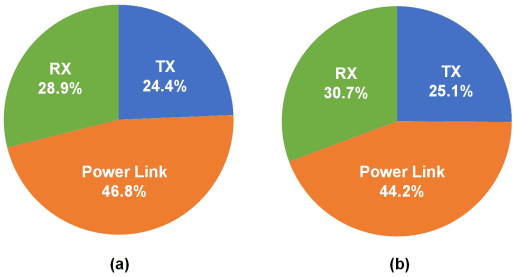

Fig. 10. Simulated power loss breakdown when $k = 0.2$. (a) $V_{BAT1} = V_{BAT2} = 4.2$ V. (b) $V_{BAT1} = V_{BAT2} = 3.7$ V.

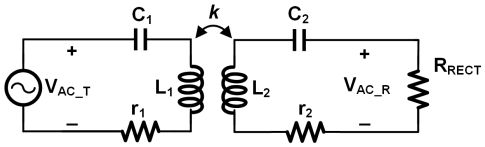

Fig. 11. Equivalent circuit of the D2D direct charging system.

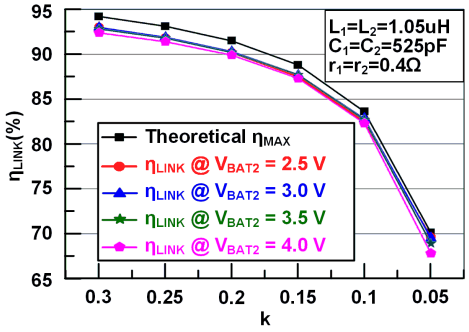

Fig. 12. Simulated power link efficiencies compared with the theoretical maximum link efficiencies.

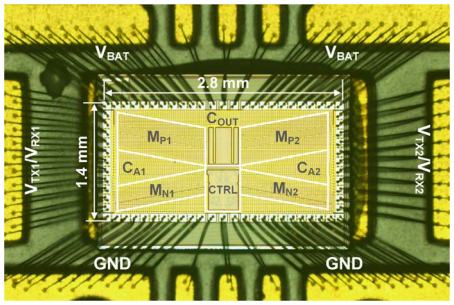

Fig. 13. Die micrograph of the reconfigurable CC wireless power TRX.

drive voltage of 2.5 V. When V_{BAT2} is 4.2 V, the simulated rectifier efficiency increases to 93.8%.

For the total efficiency, simulations under different process corners (including tt, ff, and ss), different temperatures (−40 °C and 150 °C), and different voltages have been carried out. When $V_{BAT1} = V_{BAT2} = 4.2$ V, the worst total efficiency is 79.8%, with 95.1% PA efficiency, 90.1% link efficiency, and 93.2% rectifier efficiency. When $V_{BAT1} = V_{BAT2} = 3.7$ V, the worst total efficiency is 79.2%, with 94.8% PA efficiency, 90.3% link efficiency, and 92.6% rectifier efficiency. The power loss breakdowns are shown in Fig. 10. It shows that the main loss is from the power link.

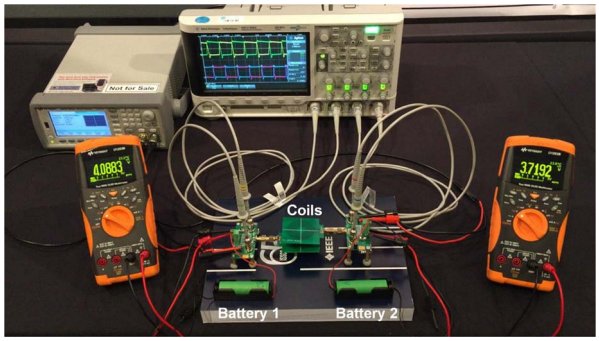

Fig. 14. D2D demonstration setup.

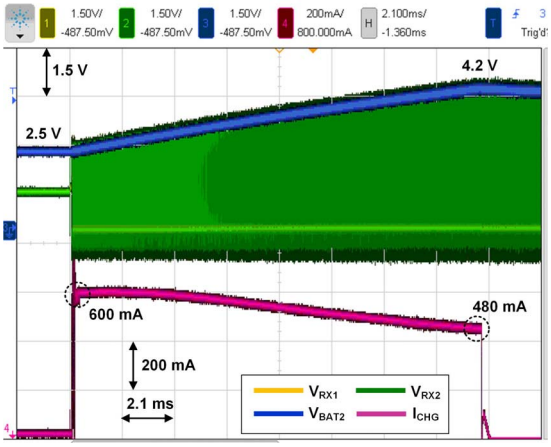

Fig. 15. Measured curve while charging a 4.7-mF capacitor.

IV. Analysis on the Power Link Efficiency

To achieve a high total efficiency, the power link efficiency should also be optimized. However, the peak power link efficiency η_{MAX} can only be obtained at the optimum load [20], R_{OPT}. When $k^2 Q_1 Q_2$ is much larger than 1, R_{OPT} can be given by

$$R_{OPT} \approx k\sqrt{Q_1/Q_2} \cdot \omega_{RES} L_2 \tag{3}$$

where Q_1 and Q_2 are the unloaded quality factor of L_1 and L_2, respectively. From (3), we know that R_{OPT} is proportional to k.

In the D2D direct charging scenario, the load of the rectifier is a battery, where the voltage maintains its value quite constant for a certain duration. The equivalent resistance of the battery varies with k because the charging current is related to k. The D2D direct charging system can be equivalent to the circuit shown in Fig. 11. R_{RECT} is the equivalent input resistance of the rectifier loaded with a battery, which can be expressed by

$$R_{RECT} = \frac{\frac{A}{n}\sqrt{Q_2/Q_1}}{1 - \frac{A}{n} \cdot \frac{1}{kQ_1}} \cdot R_{OPT} \tag{4}$$

with

$$n = \sqrt{L_2/L_1} \tag{5}$$

$$A = V_{AC\_R}/V_{AC\_T}. \tag{6}$$

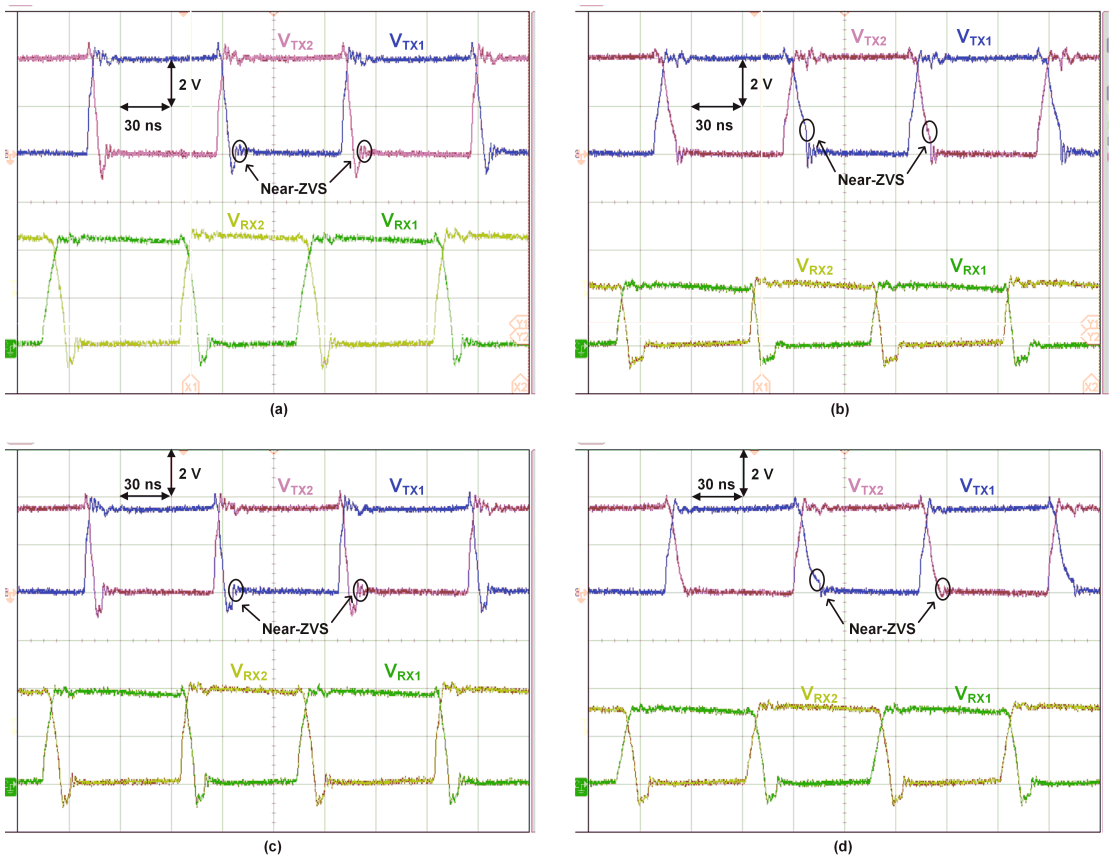

Fig. 16. Measured waveforms of the reconfigurable CC wireless power TRX when transmitting distance $d = 10$ mm. (a) $V_{\mathrm{BAT1}} = 4.2$ V and $V_{\mathrm{BAT2}} = 4.2$ V. (b) $V_{\mathrm{BAT1}} = 4.2$ V and $V_{\mathrm{BAT2}} = 2.8$ V. (c) $V_{\mathrm{BAT1}} = 3.7$ V and $V_{\mathrm{BAT2}} = 3.7$ V. (d) $V_{\mathrm{BAT1}} = 3.7$ V and $V_{\mathrm{BAT2}} = 2.8$ V.

To achieve the peak power link efficiency, R_{RECT} should be equal to R_{OPT}, which means

$$\frac{A}{n} = \frac{kQ_1}{1+\sqrt{k^2Q_1Q_2}}. \tag{7}$$

Considering that $k^2Q_1Q_2$ is much larger than 1, the denominator of (7) is several times larger than 1 and A/n is weakly related to k. For example, if $k^2Q_1Q_2 > 10$, A/n varies in a small range when k varies, leading to

$$\frac{\sqrt{10}}{1+\sqrt{10}} \cdot \sqrt{\frac{Q_1}{Q_2}} < \frac{A}{n} < \sqrt{\frac{Q_1}{Q_2}}. \tag{8}$$

Therefore, when designing the coils, A and n should be co-designed to satisfy (8) and achieve the near-maximum link efficiency.

In our case, we designed two identical PCB coils with an inductance of 1.05 μH and a Q-factor of 111. Generally, the voltage of a Li-ion battery varies from 2.5 to 4.2 V, and we always use a device with higher energy to charge the one with less energy. Therefore, A is within the range of 0.6–1, most of which overlap with (8). We simulated the power link efficiencies with the above-mentioned power link parameters and compared them with η_{MAX}, as shown in Fig 12. We can see that under a wide range of k from 0.05 to 0.3, the simulated power link efficiencies are very close to the theoretical η_{MAX}.

Compared with other papers achieving η_{MAX} with maximum-efficiency point tracking schemes [21], [22], the proposed D2D wireless charging system with identical coils can achieve near-η_{MAX} without any active control circuits or extra components. Considering the phone-to-watch charging case, although the battery capacities are different, the voltage gain A is within the same range, and therefore, the assumptions made earlier are still valid. For the pad-to-phone case, $L_1 > L_2$, and thus, $n < 1$, then easily satisfying (8).

V. Measurement Results

Fig. 13 shows the die micrograph of the proposed reconfigurable CC wireless power TRX. Fabricated in a 0.35-μm CMOS n-well process, it occupies 3.92 mm^2, including the pads. Fig. 14 shows a D2D demonstration system of the proposed wireless power TRX. We used two Li-ion batteries to charge each other wirelessly.

In the measurement, we worked with two wireless power TRXs, one configured in the TX mode and the other in the RX mode. Two identical PCB coils with 4-cm outer diameters form the wireless power link. The measured inductance is 1.05 μH and the unloaded Q-factor is 111 when operating at 6.78 MHz. For the charging curve measurement, a 4.7-mF capacitor emulates the battery for saving measurement time and reducing storage data. For the efficiency measurements, an E-load in constant-voltage mode emulates

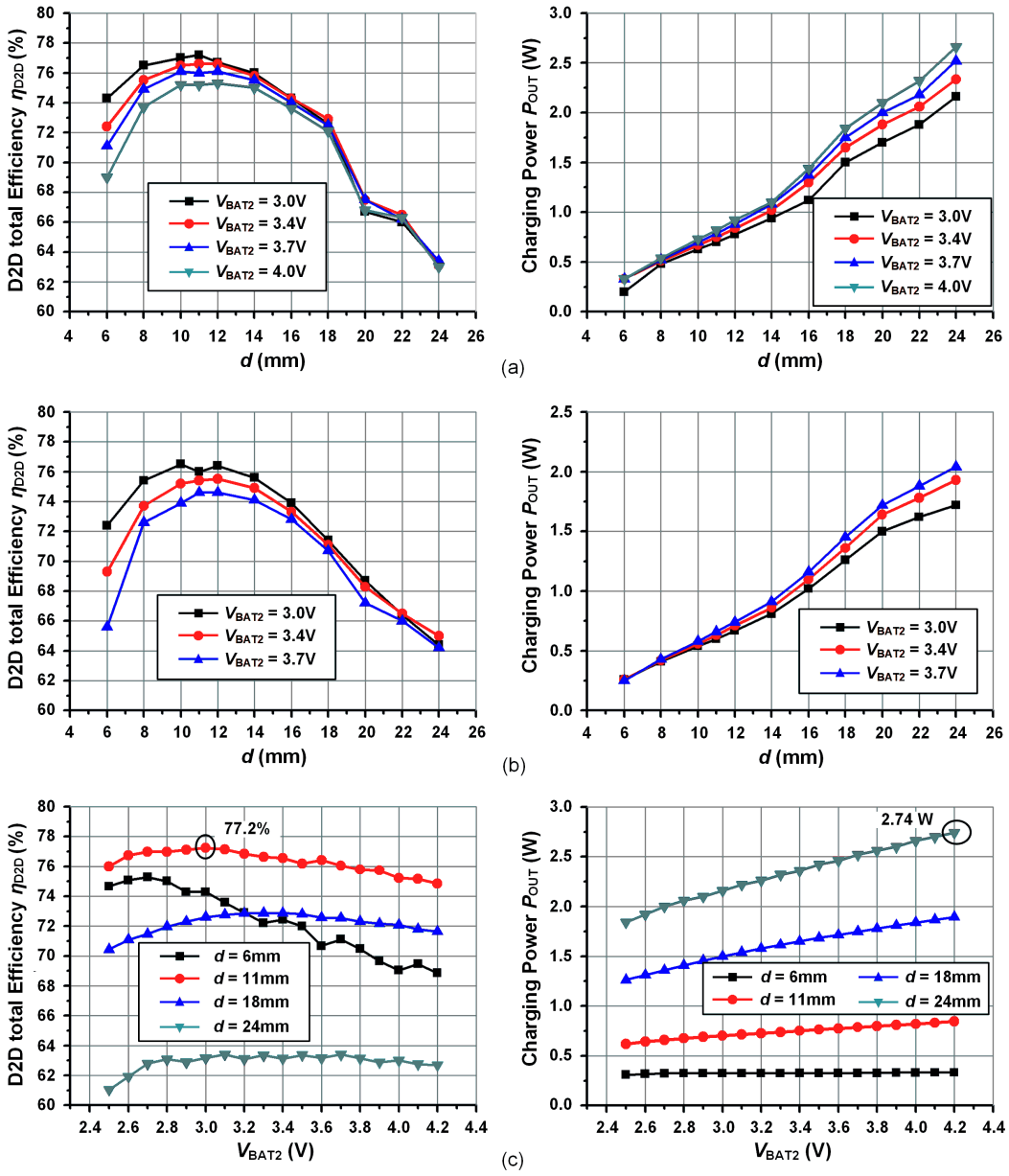

Fig. 17. Measured D2D total efficiencies and charging power with different transmitting distances when (a) $V_{BAT1} = 4.2$ V and (b) $V_{BAT1} = 3.7$ V. (c) Measured D2D total efficiencies and charging power with $V_{BAT1} = 4.2$ V and different values of V_{BAT2}.

a battery. Fig. 15 shows the measured V–I charging curve with a 4.7-mF capacitor when the transmitting distance is 19 mm and $V_{BAT1} = 4.2$ V. When the capacitor voltage charges from 2.5 to 4.2 V, the output charging current changes gradually from 600 to 480 mA.

Fig. 16 shows the measured waveforms of the reconfigurable CC wireless power TRX when the transmitting distance is 10 mm. When $V_{BAT1} = V_{BAT2} = 4.2$ V or $V_{BAT1} = V_{BAT2} = 3.7$ V, V_{TX1} and V_{TX2} drop to about -0.7 V for a short time duration before M_{N1} and M_{N2} are turned on, as shown in Fig. 16(a) and (c), which means that the deadtime between V_{NT1} and V_{NT2} is a little larger than the optimal value. When $V_{BAT2} = 2.8$ V, V_{TX1} andV_{TX2} are slightly larger than 0 V when M_{N1} and M_{N2} are turned on, as shown in Fig. 16(b) and (d), which means that the deadtime between V_{NT1} and V_{NT2} is a little smaller than the optimum value. Therefore, near-ZVS is achieved.

Fig. 17(a) and (b) shows the measured D2D total efficiency and charging output power with transmitting distance d varying from 6 to 24 mm when V_{BAT1} is 4.2 and 3.7 V, respectively. When d increases, the total efficiency rises first and then drops. Meanwhile, the output power P_{OUT} keeps increasing as d increases, which happens because a smaller k leads to a smaller Z_{EQ}. For a well-designed PA with small output impedance, a smaller Z_{EQ} value results in a larger output power. When d is short, the output power is small, and the switching losses of the power transistors dominate the power loss. On the other hand, when d is long, P_{OUT} is large,

TABLE I
COMPARISON WITH PRIOR WORKS

	JSSC [23]	ISSCC [24]	ESSRIRC [21]	ISSCC [6]	This Work
Year	2013	2016	2016	2017	**2018**
WPT Direction	Unidirectional	Unidirectional	Unidirectional	Bi-Directional	**Bi-Directional**
Mode	Pad-to-Device	Pad-to-Device	D2D	Reconf. D2D	**Refconf. D2D**
Process	0.35μm BCD	0.18μm BCD	0.18μm CMOS	0.35μm CMOS	**0.35μm CMOS**
Freq. (MHz)	6.78	0.1-0.3, 6.78	6.78	6.78	**6.78**
$V_{OUT,MAX}$ (V)	5	3.5	4.2	4.2	**4.2**
$P_{OUT,MAX}$ (W)	6	2.5	0.74	1.65	**2.74**
η_{TOTAL} MAX	55%	63%	52.30%	58.60%	**77.20%**
Distances (mm)	NA	NA	19	6	**24**
Area (mm^2)	5.52	5.83	1.2	3.9	**3.92**
Off-Chip Components	5 Diodes 3 Capacitors	1 Inductors 3 Capacitors	2 Inductors 2 Capacitors	1 Capacitor	**1 Capacitor**

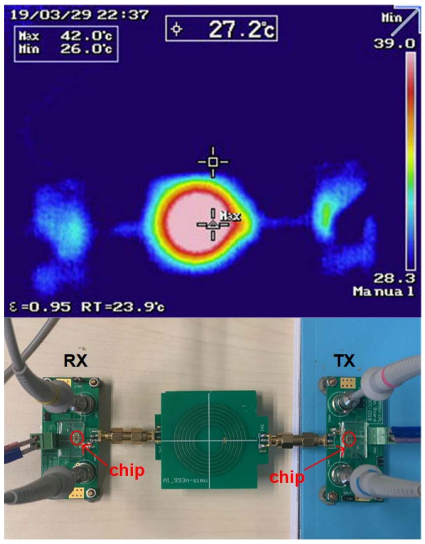

Fig. 18. Measured thermal map of the D2D wireless charging system when $P_{OUT} = 2.74$ W.

and the conduction losses of the power transistors become dominant. Then, the peak D2D total efficiencies exist with d values between 10 and 12 mm in different cases. Fig. 17(c) shows the measured D2D total efficiency and output power when V_{BAT2} varies from 2.5 to 4.2 V. We obtained a peak D2D total efficiency of 77.2% when the transmitting distance $d = 11$ mm and the output power is 0.7 W. The maximum output power is 2.74 W with a total efficiency of 62.7% when $d = 24$ mm and $V_{BAT2} = 4.2$ V.

Fig. 18 shows the measured thermal map of the D2D wireless charging with the maximum output power of 2.74 W and a room temperature of 23.9 °C. According to Fig. 18, the highest temperature is 42 °C and it happens in the coil area. For the two chips, the temperature is only about 33.5 °C, proving the high efficiency of the CC differential class-D PA and CC full-wave rectifier. Table I compares the performances of prior works with the proposed reconfigurable bidirectional wireless power system that measured the highest total efficiency and the longest transmitting distance at 6.78 MHz. In addition, only one off-chip capacitor is necessary, leading to a very compact solution.

VI. CONCLUSION

This paper presented a reconfigurable bidirectional wireless power transceiver with a newly proposed fully CC topology for D2D wireless charging. In addition, a dedicated reconfigurable DLL-based controller has been designed to realize adaptive deadtime for ZVS in the TX mode and near-zero-reverse current in the RX mode. An on-chip tunable capacitor, inserted between the power transistors in the layout, ensured an inductive equivalent load on the TX side for the whole range of the coupling coefficient. We also verified that the wireless power link efficiency in our direct charging D2D system is very close to the theoretical maximum power link efficiency. Finally, by fully enjoying the switching-loss-free feature of the CC topology, we achieved a 77.2% peak total efficiency at 6.78 MHz.

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