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Analysis, Design and Control of an Integrated Three-Level Buck Converter under DCM Operation*

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A three-level buck (TLB) converter has the characteristics of higher voltage conversion efficiency, lower inductor current ripples, output voltage ripples and voltage stresses on switches when compared with the buck converters in continuous conduction mode (CCM). With a TLB converter integrated on a chip, we cannot avoid its discontinuous conduction mode (DCM) operation due to a smaller inductance and load variation. In this paper, we'll present and discuss the analysis, design and control of a TLB converter under DCM operation, implemented in a 65 nm CMOS process. Transistor level simulation results show that when the TLB converter operates at 100 MHz with a 5 nH on-chip inductor, a 10 nF output capacitor and a 10 nF flying capacitor, it can achieve an output conversion range of 0.7–1.2 V from a 2.4 V input supply, with a peak efficiency of 81.5%@120 mW. The output load transient response is 100 mV with 101 ns for undershoot, and 86 mV with 110 ns for overshoot when I_{OUT} = 10–100 mA. The maximum output voltage ripple is less than 19 mV.

Keywords: Three-level buck converter; DCM; modeling; fast transient response; low voltage ripple; voltage mode controller.

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1. Introduction

In recent years, fully-integrated DC–DC converters have gained much attention because of their elimination of bulky and expensive inductors and capacitors and their greatly shrunk PCB footprints.[1] The full-integration is realized by greatly increasing the switching frequency. Reference 2 presents a fully integrated three-level buck converter operating in CCM with 50–200 MHz switching frequency and nanoscale inductance and capacitance. Reference 3 presents a fully integrated three-level buck converter operating in CCM with 37.28 MHz switching frequency. References 1, 4–7 present fully integrated buck converters operating at several hundred MHz. Reference 8 even utilizes switching frequency up to 2 GHz. The three-level buck (TLB) converter has an attractive characteristic of effectively doubling its switching frequency (f_{sw})[2,3,9,10] and halving the voltage level across the inductor, thus reducing the switching ripples and filter elements' size, and also increasing the converter open-loop bandwidth and efficiency.[2] Through appropriate design, its power MOSFETs can just bear half of the voltage stress when compared with those of the two-level buck converter, thus lowering operation voltage and dynamic losses. The TLB converter operating in continuous conduction mode (CCM) has been studied, which yields the same DC and AC transfer functions as the buck converter.[3,9,10] In portable applications especially powered by battery, the system will enter lower power mode or sleep mode, to save the power and prolong the running time of battery.[1] Thus, the fully integrated buck converter will operate in discontinuous conduction mode (DCM) operation due to small inductance and such light load conditions. Reference 3 implements a fully integrated three-level buck converter in DCM, but the DC and AC operation theory and characteristics are missing,[2,3,9,10] which are critical to the small-signal characterization and closed-loop control. Fuzzy logic control without the knowledge of the circuit model has been extensively investigated in application of DC–DC converters.[11,12] However, the AD/DA converter and fuzzy reasoning block make it much more complex, power consuming and of larger size compared with the conventional analog counterpart. In addition, the driving scheme is improved, allowing the use of thin-oxide transistors for the drivers and power MOSFETs, which will reduce the switching loss and also save the chip area and thus reduce the cost. In this paper, the main contributions are

(1) The presentation of the DCM driving signal waveforms by using low-voltage power MOSFETs, followed by the deduction of the CCM/DCM boundary conditions, the DC large signal and AC small signal transfer functions, which are totally different when compared with the conventional buck converter. The AC small signal transfer functions is obtained by the average switch method[13–16];
(2) The design presentation of the voltage mode controller, including the loop type-II compensator, pulse width modulation (PWM) generator, zero current detection, self-driving scheme and level shifter for the TLB converter;

(3) The exhibition of the behavioral simulation results of the TLB converter to verify the DCM analysis, which is important for the DCM closed-loop controller design. Finally, the design of the closed-loop controlled TLB converter and its implementation using ST 65 nm CMOS process. Simulation results verify the analysis, design and control of the TLB converter, in which the performance is comparable with the state-of-the-art works.

2. DCM Operation Principle of the TLB Converter

Figure 1 shows the topology and details of the driving scheme of the TLB converter, where $V_{\rm IN}$, $V_{\rm OUT}$ and $V_{\rm REF}$ are the input, output and reference voltages; C_f and V_{Cf} are the flying capacitor and its voltage. In steady state, $V_{Cf} \approx V_{\rm IN}/2$ if C_f is large enough[3]; L and C are the inductor and filtering capacitor; R is the load resistor; $I_{\rm OUT}$, I_L and I_C are the output, inductor, and capacitor currents, respectively. A capacitive level shifter[17] is applied for the TLB converter. The capacitive level shifter is described in detail in Sec. 7.3. The upper part of Figs. 2(a) and 2(b) show the controller PWM signals and the gate driving signals for the four power MOSFETs with duty ratio $D \leq 0.5$ and $D \geq 0.5$ in DCM. The left column signals in the upper part of Figs. 2(a) and 2(b) are the control signals from the controller and the right column are the gate driving signals, which are generated by the corresponding control signals from the controller passing through the level shifters and drivers. $V_{\rm BOT}$ is of the same voltage level with $V_{\rm PWMbot}$, and $V_{\rm TOP}$ is shifted by $V_{\rm IN}/2$. The flying capacitor supplies the level shifters and drivers in the middle, such that the voltage level is dependent on the switching state of the converter.

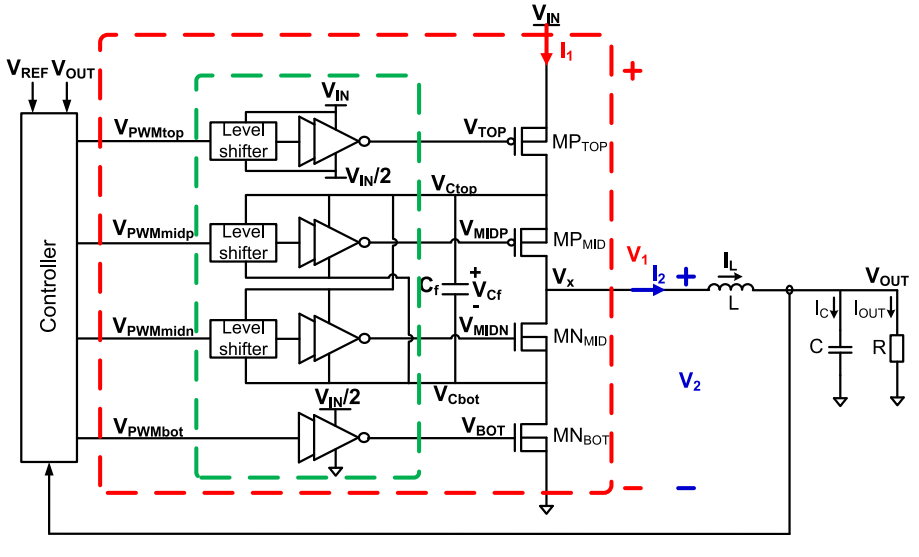
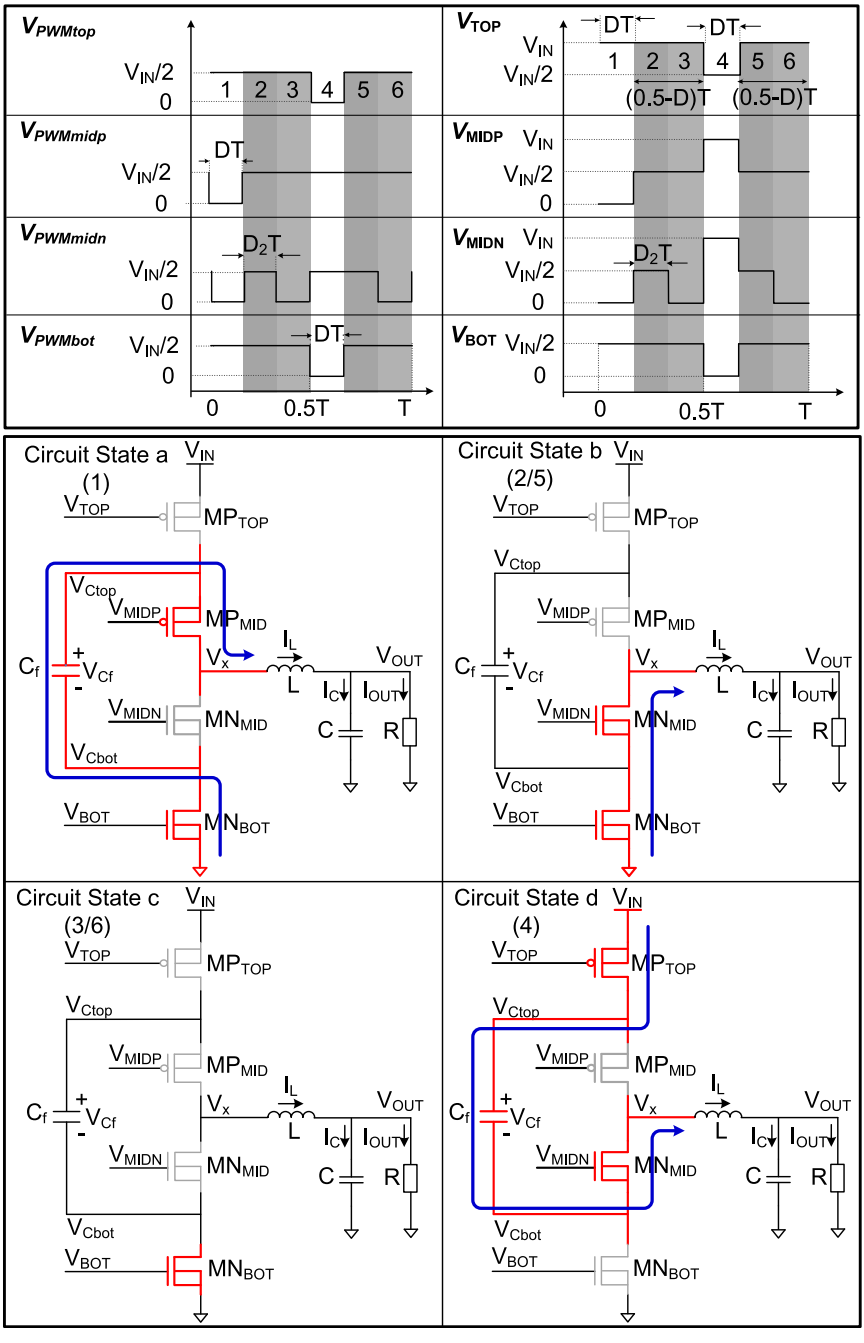
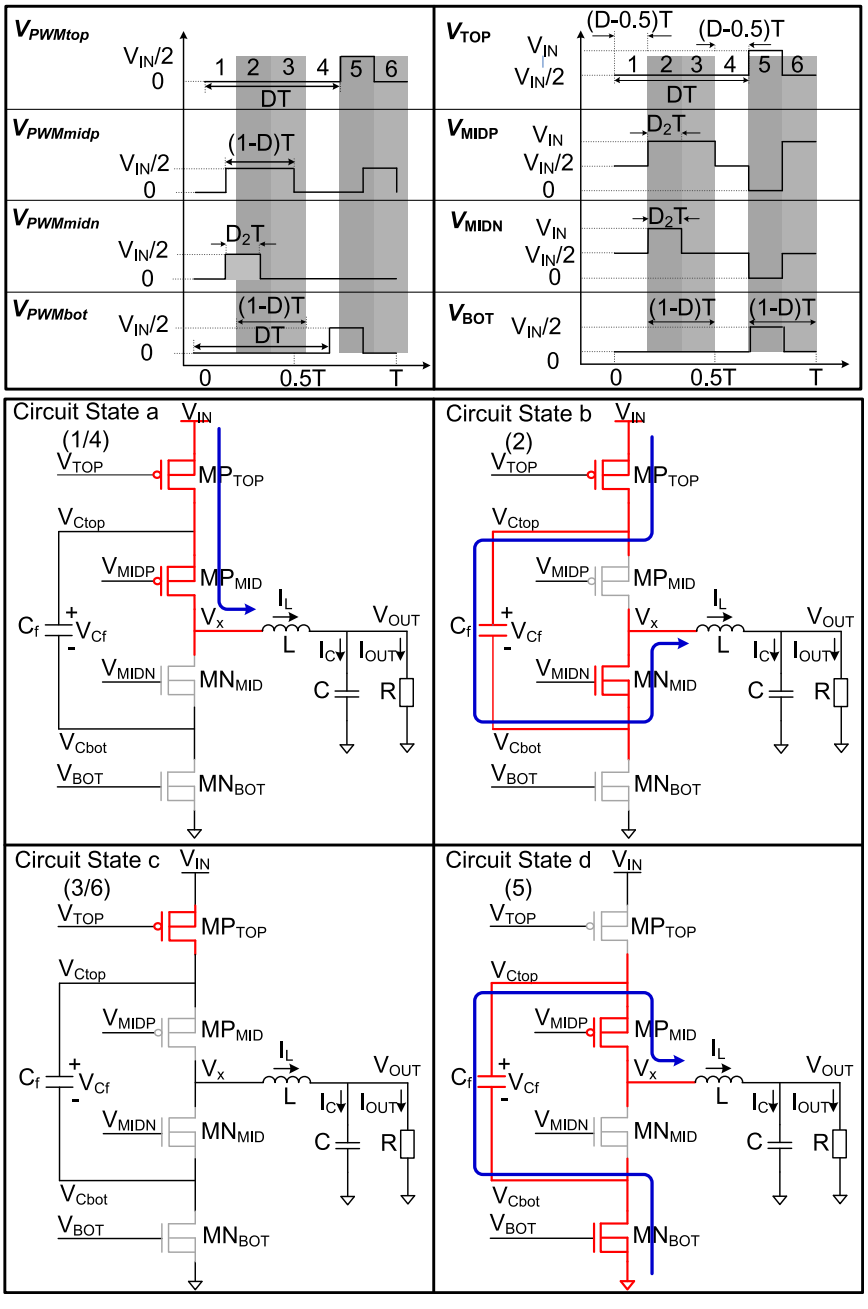


Fig. 1. TLB converter topology and driving scheme.



(a)

Fig. 2. Circuit states of the TLB converter in DCM, (a) duty cycle $D \leq 0.5$ and (b) $D \geq 0.5$.



(b)

Fig. 2. (*Continued*)

As the upper part of Fig. 2(a) shows, for the case $D \leq 0.5$, in switching state 1, V_{TOP} and V_{BOT} is at V_{IN} and $V_{\mathrm{IN}}/2$ level, respectively, and the power MOSFET $\mathrm{MP_{TOP}}$ (PMOS) turns off while $\mathrm{MN_{BOT}}$ (NMOS) turns on, thus $V_{C\mathrm{top}}$ and $V_{C\mathrm{bot}}$ are at $V_{\mathrm{IN}}/2$ and GND level, therefore V_{MIDP} and V_{MIDN} are the same voltage level with V_{PWMmidp} and V_{PWMmidn}, then the power MOSFET $\mathrm{MP_{MID}}$ (PMOS) turns on while $\mathrm{MN_{MID}}$ (NMOS) turns off. The flying capacitor C_f charges the inductor L, as Fig. 2(a) circuit state a shows (the power MOSFET in gray color means in off state). As shown in Fig. 2(a) circuit states a, b and c, $\mathrm{MP_{TOP}}$ and $\mathrm{MN_{BOT}}$ keep in the same circuit state in switching states 1/2/3/5/6. In switching state 2, as Fig. 2(a) circuit state b shows, $\mathrm{MP_{MID}}$ turns off while $\mathrm{MN_{MID}}$ turns on, the inductor L discharges until the inductor current decreases to zero, then the control circuit cuts off the I_L negative current flow path and keeps $I_L = 0$ in switching state 3, as Fig. 2(a) circuit state c shows. In the second half of the switching cycle, $\mathrm{MP_{TOP}}$ turns on while $\mathrm{MN_{BOT}}$ turns off in switching state 4 (Fig. 2(a) circuit state d), so $V_{C\mathrm{top}}$ and $V_{C\mathrm{bot}}$ are at V_{IN} and $V_{\mathrm{IN}}/2$ level, then V_{MIDP} and V_{MIDN} are shifted by $V_{\mathrm{IN}}/2$, thus $\mathrm{MP_{MID}}$ turns off while $\mathrm{MN_{MID}}$ turns on, and the inductor L is charged by V_{IN} through the flying capacitor C_f, as Fig. 2(a) circuit state d illustrates. Switching states 5 and 6 are identical to the switching states 2 and 3, respectively.

A similar analysis approach can be applied for the case $D \geq 0.5$. The difference is that inductor L is charged by V_{IN} and discharged through the flying capacitor. The discharging switching states 2 and 5 (Fig. 2(b) circuit states b and d) are the only different switching states between the first and the second half switching cycle as shown in the upper part of Fig. 2(b). The discharging path is through V_{IN} and the flying capacitor with negative terminal connected to the inductor L in switching state 2 (Fig. 2(b) circuit state b), while only through the flying capacitor C_f with positive terminal connected to the inductor L in switching state 5 (Fig. 2(b) circuit state d). (This difference is to keep the flying capacitor C_f charge balance to keep the capacitor voltage at $V_{\mathrm{IN}}/2$ level, so do the switching states 1 and 4 (Fig. 2(a) circuit states a and d) for $D \leq 0.5$.) The lower part of Fig. 2(b) shows the circuit state and switching state corresponding to the control signal in the upper part of Fig. 2(b).

Table 1. Terminal voltage of the power MOSFETs in the steady-state.

	$D \leq 0.5$						$D \geq 0.5$					
	1	2	3	4	5	6	1	2	3	4	5	6
V_{TOP}	V_{IN}	V_{IN}	V_{IN}	$V_{\mathrm{IN}}/2$	V_{IN}	V_{IN}	$V_{\mathrm{IN}}/2$	$V_{\mathrm{IN}}/2$	$V_{\mathrm{IN}}/2$	$V_{\mathrm{IN}}/2$	V_{IN}	$V_{\mathrm{IN}}/2$
$V_{C\mathrm{top}}$	$V_{\mathrm{IN}}/2$	$V_{\mathrm{IN}}/2$	$V_{\mathrm{IN}}/2$	V_{IN}	$V_{\mathrm{IN}}/2$	$V_{\mathrm{IN}}/2$	V_{IN}	V_{IN}	V_{IN}	V_{IN}	$V_{\mathrm{IN}}/2$	V_{IN}
V_{MIDP}	0	$V_{\mathrm{IN}}/2$	$V_{\mathrm{IN}}/2$	V_{IN}	$V_{\mathrm{IN}}/2$	$V_{\mathrm{IN}}/2$	$V_{\mathrm{IN}}/2$	V_{IN}	V_{IN}	$V_{\mathrm{IN}}/2$	0	V_{IN}
V_X	$V_{\mathrm{IN}}/2$	0	V_{OUT}	$V_{\mathrm{IN}}/2$	0	V_{OUT}	V_{IN}	$V_{\mathrm{IN}}/2$	V_{OUT}	V_{IN}	$V_{\mathrm{IN}}/2$	V_{OUT}
V_{MIDN}	0	$V_{\mathrm{IN}}/2$	0	V_{IN}	$V_{\mathrm{IN}}/2$	0	$V_{\mathrm{IN}}/2$	V_{IN}	$V_{\mathrm{IN}}/2$	$V_{\mathrm{IN}}/2$	0	$V_{\mathrm{IN}}/2$
$V_{C\mathrm{bot}}$	0	0	0	$V_{\mathrm{IN}}/2$	0	0	$V_{\mathrm{IN}}/2$	$V_{\mathrm{IN}}/2$	$V_{\mathrm{IN}}/2$	$V_{\mathrm{IN}}/2$	0	$V_{\mathrm{IN}}/2$
V_{BOT}	$V_{\mathrm{IN}}/2$	$V_{\mathrm{IN}}/2$	$V_{\mathrm{IN}}/2$	0	$V_{\mathrm{IN}}/2$	$V_{\mathrm{IN}}/2$	0	0	0	0	$V_{\mathrm{IN}}/2$	0

Table 1 summarizes the terminal voltages of the four power MOSFETs, where f_{sw} is the switching frequency and $T(1/f_{\text{sw}})$ is the switching period. All of the voltages across them are less than or equal to $V_{\text{IN}}/2$, which avoids the use of high-voltage tolerant power MOSFETs, thus saving area, cost and loss.

3. Boundary Between CCM and DCM of the TLB Converter

It is important to understand the boundary conditions between CCM and DCM of the TLB converter. Assuming that L, C_f and the power MOSFET are ideal, and C_f is large enough so that $V_{Cf} \approx V_{\text{IN}}/2$, Fig. 3 shows the idealized switching node voltage V_X and inductor current I_L waveforms in DCM. For $D \leq 0.5$, in steady state, the inductor current ripple amplitude ΔI_1 in switching state 1 and ΔI_2 in switching state 2 can be expressed as

$$\Delta I_1 = \frac{1}{L}\int_0^{DT} v_L(t)dt = \frac{1}{L}\left(\frac{1}{2}V_{\text{IN}} - V_{\text{OUT}}\right)DT\,, \tag{1}$$

$$\Delta I_2 = \frac{1}{L}V_{\text{OUT}}D_2T\,, \tag{2}$$

where D_2 is the duty cycle in switching states 2 and 5. Output load current $I_{\text{OUT}} = V_{\text{OUT}}/R$, which also equals the average current I_L flowing through inductor L in one switching cycle,

$$I_L = \frac{1}{T}\int_0^{T} i_L(t)dt = \frac{D + D_2}{L}\left(\frac{1}{2}V_{\text{IN}} - V_{\text{OUT}}\right)DT\,. \tag{3}$$

The output load resistance R_B and output load current $I_{\text{OUT}B}$ at the CCM/DCM boundary can be determined when $D + D_2 = 0.5$. With $I_L = I_{\text{OUT}} = \frac{V_{\text{OUT}}}{R}$, Eqs. (1) and (2) and some mathematical manipulation, the boundary output load resistance R_B and current $I_{\text{OUT}B}$ at $D \leq 0.5$ can be obtained as Eqs. (4) and (5). With similar deduction approach, R_B and $I_{\text{OUT}B}$ at $D \geq 0.5$ can be obtained as Eqs. (6) and (7),

$$R_B|_{D\leq 0.5} = \frac{2L}{(0.5 - D)T}\,, \tag{4}$$

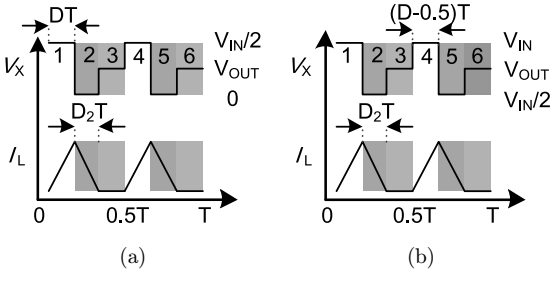


Fig. 3. The idealized steady-state V_X and I_L of the TLB converter in DCM, (a) $D \leq 0.5$ and (b) $D \geq 0.5$.

$$I_{\mathrm{OUT}B}|_{D\le 0.5} = \frac{V_{\mathrm{OUT}}(0.5-D)T}{2L}\,, \tag{5}$$

$$R_B|_{D\ge 0.5} = \frac{2LD}{(1-D)(D-0.5)T}\,, \tag{6}$$

$$I_{\mathrm{OUT}B}|_{D\ge 0.5} = \frac{V_{\mathrm{OUT}}(1-D)(D-0.5)T}{2LD} \tag{7}$$

in which the boundary output load resistance R_B and current $\mathrm{I}_{\mathrm{OUT}B}$ are different from the traditional two-level buck converter.[13] The differences are due to the fact that the V_X of the three-level buck converter switches between 0 and $V_{\mathrm{IN}}/2$ for $D < 0.5$, $V_{\mathrm{IN}}/2$ and V_{IN} for $D > 0.5$, while between 0 and V_{IN} for the two-level buck converter.

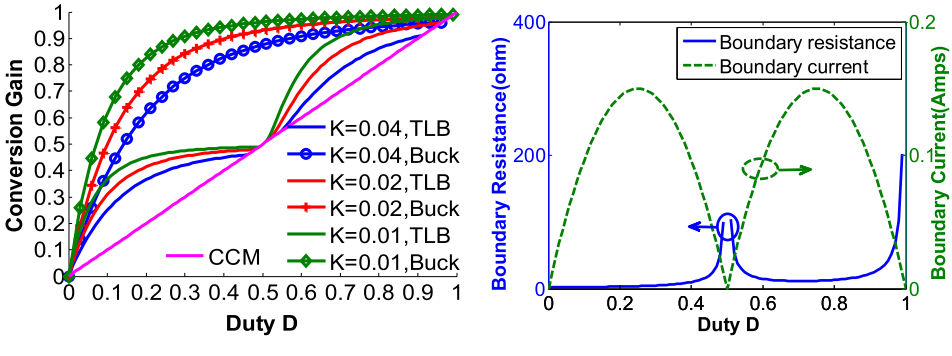
4. DC Characteristics of the TLB Converter in DCM

From Eqs. (1) and (2) together with Eq. (3), after some manipulation, the output voltage V_{OUT} for $D \le 0.5$ and $D \ge 0.5$ can be obtained as Eqs. (8) and (9) show,

$$V_{\mathrm{OUT}} = \frac{\left(\sqrt{D^2+2K}-D\right)D}{2K}V_{\mathrm{IN}}\,, \tag{8}$$

$$V_{\mathrm{OUT}} = \left(\frac{\sqrt{((D-0.5)^2/K-0.5)^2+4(D-0.5)^2/K)}}{2} - \frac{(D-0.5)^2/K-0.5}{2}\right)V_{\mathrm{IN}}\,, \tag{9}$$

where $K = \frac{2L}{RT}$. It is clear that the TLB converter obtained a different V_{OUT} when compared with the traditional two-level buck converter.[13] Figure 4(a) plots the TLB and traditional two-level buck converter DC characteristics (voltage conversion gain $M = V_{\mathrm{OUT}}/V_{\mathrm{IN}}$) in MATLAB environment with $L = 5\,\mathrm{nH}$ and $T = 10\,\mathrm{ns}$



(a) (b)

Fig. 4. (a) Conversion gain M and (b) CCM/DCM boundary R_B and $I_{\mathrm{OUT}B}$ for TLB converter.

($f_{sw} = 100\,\text{MHz}$), for both CCM ($M = D$) and DCM with several different K values, which clearly shows that they have different DCM gain characteristics even though they are same in CCM. Figure 4(b) plots the boundary output load resistance R_B and boundary output load current I_{OUTB} between CCM and DCM for the TLB converter.

5. AC Characteristics of the TLB Converter in DCM

To obtain the AC characteristics, the averaged switching network modeling method[13–16] is applied, identified in the dashed box with terminal quantities as Fig. 1 shows. v_1 equals V_{IN}, and i_1 equals the inductor current when MP_{TOP} turns on and equals to zero otherwise. v_2 equals V_X and i_2 equals the inductor current.[13–16] Figure 5 plots the waveforms of the switching network terminals in one switching cycle. Taking $D \leq 0.5$ for example, averaging the terminal quantities and applying the inductor volt-seconds balance principle,[13–16] it yields,

$$v_1(t) = v_{IN}(t)\,, \tag{10}$$

$$i_1(t) = \frac{1}{R_e}(v_1(t)/2 - v_2(t))\,, \tag{11}$$

$$v_2(t) = v_{OUT}(t)\,, \tag{12}$$

$$i_2(t) = \frac{1}{R_e}\,\frac{0.5v_1(t) - v_2(t)}{v_2(t)}\,v_1(t)\,, \tag{13}$$

where $R_e = \frac{2L}{D^2T}$ is the effective resistor of the average switching network. After perturbation, linearization and some manipulation,[13–16] the parameters of the small signal model of the switching network can be obtained as Fig. 6 illustrates. With a similar deduction approach, the small signal parameters for $D \geq 0.5$ can also be obtained. Table 2 summarizes the results, where $M = \frac{V_2}{V_1} = \frac{V_{OUT}}{V_{IN}}$ represents the voltage conversion gain.

By taking partial derivative of i_1 and i_2 in Eqs. (11) and (13) with respect to V_{OUT}, D and V_{IN}, together with expression $\hat{i}_2 = -\hat{v}_{OUT}/r_2 + j_2\hat{d} + g_2\hat{v}_{IN}$ obtained from

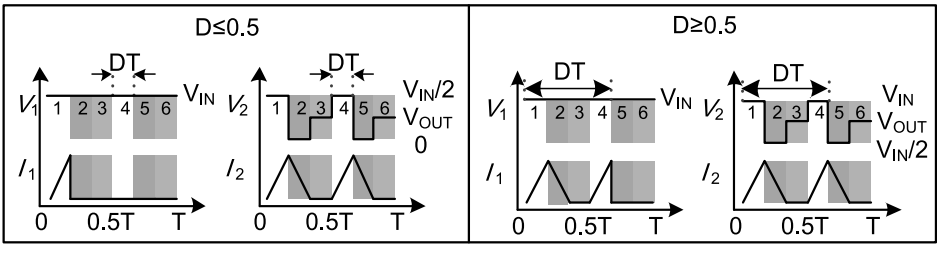


Fig. 5. TLB converter switch network terminal voltage and current waveforms in one switching cycle under DCM.

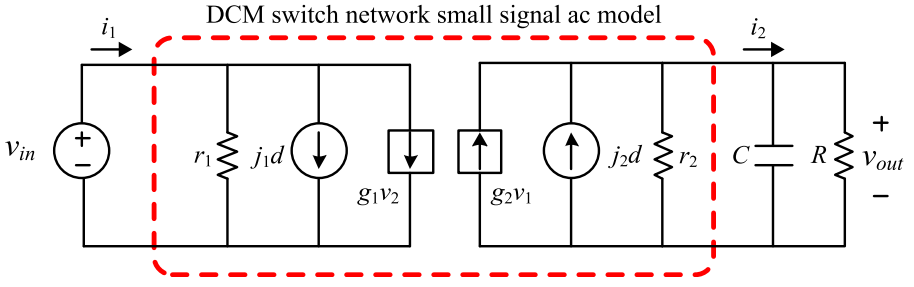


Fig. 6. Low-frequency AC small signal model of the TLB converter.

Table 2. Small signal parameters of TLB converters in DCM.

	g_1	j_1	r_1	g_2	j_2	r_2
$D \le 0.5$	$-\frac{1}{R_e}$	$\frac{V_{\rm IN}(1-2M)}{DR_e}$	$2R_e$	$\frac{1-M}{2MR_e}$	$\frac{V_{\rm IN}(1-2M)}{DMR_e}$	$2M^2R_e$
$D \ge 0.5$	$\frac{M-M^2-\frac{1}{2}}{R_e(M-\frac{1}{2})^2}$	$\frac{2V_{\rm IN}(1-M)M}{DR_e(M-\frac{1}{2})}$	$\frac{2R_e(M-\frac{1}{2})^2}{M^2}$	$\frac{2M-M^2-\frac{1}{2}}{R_e(M-\frac{1}{2})}$	$\frac{2V_{\rm IN}(1-M)}{DR_e(M-\frac{1}{2})}$	$2R_e(M-\frac{1}{2})^2$

Table 3. Comparison of small signal parameters of Buck and TLB converters in DCM.

	Buck	TLB	
	$0 < D < 1$	$0 < D < 0.5$	$0.5 < D < 1$
j_2	$\frac{2V_{\rm IN}(1-M)}{DMR_e}$	$\frac{V_{\rm IN}(1-2M)}{DMR_e}$	$\frac{2V_{\rm IN}(1-M)}{DR_e(M-0.5)}$
r_2	M^2R_e	$2M^2R_e$	$2R_e(M-0.5)^2$

Fig. 6, the parameters r_2, j_2 and g_2 can be found. Finally, from Fig. 6, the TLB converter small signal transfer function $G_{vd}(s)$ is expressed in Eq. (14). As $\hat{v}_{\rm IN} = 0$ for finding $G_{vd}(s)$, g_2 can be neglected.[13] Table 3 compares the DCM small signal model parameters with traditional buck converters, which show different small signal parameters.

$$G_{vd}(s) = \frac{G_{d0}}{1 + s/\omega_p} \tag{14}$$

with $G_{d0} = j_2(R//r_2)$ and $\omega_p = \frac{1}{(R//r_2)C}$.

6. Simulation Results of the TLB Frequency Response

The parameters for simulation are: $V_{\rm IN} = 2.4\,{\rm V}$, $L = 5\,{\rm nH}$, $C = 10\,{\rm nF}$, $C_f = 10\,{\rm nF}$, $f_{\rm sw} = 100\,{\rm MHz}$; $V_{\rm OUT} = 0.72\,{\rm V}$, $R = 10\,\Omega$ for $D \le 0.5$, and $V_{\rm OUT} = 1.5\,{\rm V}$, $R = 20\,\Omega$

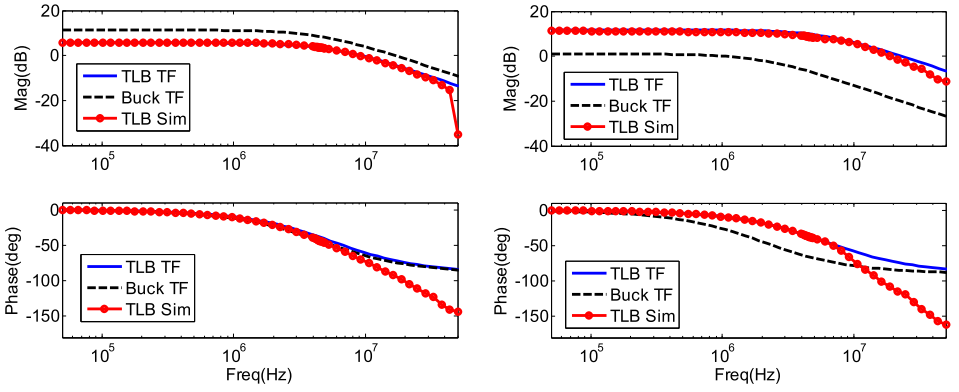


Fig. 7. The simulation frequency response of the TLB converter in DCM, (a) $D \leq 0.5$ and (b) $D \geq 0.5$.

for $D \geq 0.5$. Figure 7 shows the behavioral simulation results of the frequency response of the TLB converter as shown in Fig. 1, compared with the small signal model Eq. (14). The red dot line shows the frequency response behavioral simulation results, which are obtained by applying a small sinusoidal signal over duty cycle D and measuring the corresponding response in the output $V_{\rm OUT}$. The solid blue line is the MATLAB simulation results of Eq. (14). As Fig. 7 shows, the magnitude response matches up to half of $f_{\rm sw}$, while the phase begins to deviate from about one-tenth of $f_{\rm sw}$, which is due to the low-frequency approximation model neglecting the high-frequency pole near $f_{\rm sw}$. But these results are precise enough for closed-loop controller design. The control-to-output transfer function of the traditional buck converter[13] in DCM is also shown in dash black line in Fig. 7. Table 3 and Fig. 7 clearly show that the TLB and buck converters have different DCM transfer functions and characteristics, even though they have the same CCM ones. If one designed the TLB DCM based on the buck DCM one, the DCM closed-loop controller of the TLB converter may yield an unsatisfactory performance. Thus, it is important to analyze the DCM characteristics of the TLB converter.

7. Circuit Implementation

7.1. *Voltage mode controller*

Figure 8 shows the overall block diagram of the closed-loop voltage mode controller for a TLB converter in DCM.[18] The output voltage is scaled down by R_1 and R_2. The scaled feedback voltage $V_{\rm FB}$ is compared with the reference voltage $V_{\rm REF}$ through a Type-II compensator. Then the error voltage is amplified, generating V_e, which is compared with the sawtooth signal $V_{\rm ramp}$. The output control signal V_G is generated from the comparator, which is used to generate the duty cycle control signal. The half cycle delayed duty cycle signals $V_{\rm PWM1}$ and $V_{\rm PWM2}$, along with the zero current

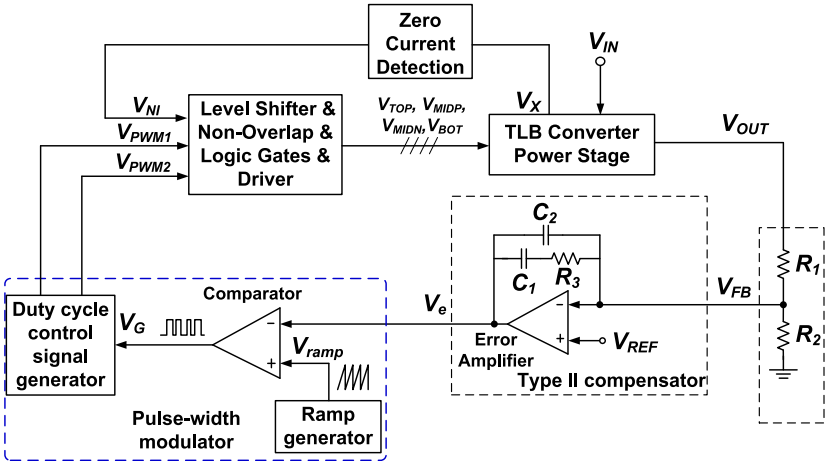


Fig. 8. DCM closed-loop voltage mode controller for a TLB converter.[18]

indication signal V_{NI}, generate the gate control signals driving the power MOSFETs by the level shifter, nonoverlap controller, logic gates and driver circuit block.

7.2. *Loop compensator*

Since the deduced model of the TLB converter in DCM is a single pole system as Eq. (14) shows, a Type-II compensation scheme is applied to compensate the closed-loop of the TLB converter. The first stage of the error amplifier (EA) is a single-ended telescopic cascade amplifier, which provides high DC gain, and the second stage is a common source amplifier, which provides high output voltage swing. The AC simulation results of the error amplifier shows that the DC gain is about 58 dB, cross-over frequency is about 414 MHz and the phase margin is about 73°. This specification is sufficient for the TLB converter loop compensation.

To verify the stability of the closed-loop TLB converter, Fig. 9 shows the bode plot of the Type-II compensator in dashed red line and the loop transfer function of the closed-loop TLB converter in blue line. The cross-over frequency of the closed-loop transfer function of the TLB with compensation is about 11.6, 26 and 31 MHz, and the corresponding phase margin is 65.5°, 62° and 63°, for 10, 72 and 120 mA load current, respectively. Considering the phase deviation as Fig. 7 shows, the actual phase margin is sufficient for the control loop stability.

7.3. *Control circuit implementation*

This section presents the other control circuits in detail, including PWM, zero current detection and self-driving scheme.

The dashed box in Fig. 8 shows the PWM generation block. The duty cycle is generated by comparing the error amplifier output V_e with a sawtooth signal V_{ramp}.

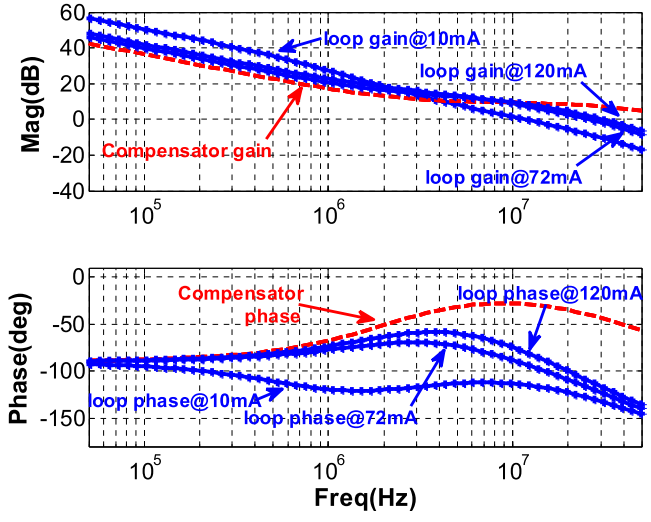


Fig. 9. Bode plot of the Type-II compensator and the loop transfer function of the closed-loop TLB converter transfer function at load current 10, 72 and 120 mA.

The sawtooth signal generator utilizes a so-called single-boundary ramp generator.[1] More details can be found in Ref. 1. The PWM comparator circuit topology is implemented by a source-coupled differential pair with positive feedback to provide a high gain.[19] The frequency of the ramp signal is twice of the switching frequency. The duty cycle control signal for the TLB converter is generated via the output of the PWM comparator V_G. Figure 10 shows the schematic of the duty cycle control signal generator, in which the outputs of the two DFFs, V_{Q1} and V_{Q2}, are rectangular waves with 50% duty cycle and their frequency is half of the ramp signal V_{ramp}. DFF1 is triggered on the rising edge of V_G and DFF2 is effectively triggered on the falling edge of V_G. Thus, V_{Q2} is delayed by the duty cycle width compared with V_{Q1}.

During DCM operation, the power MOSFET MN_{BOT} as shown in Fig. 1 should be turned off when the inductor current decreases to zero, in order to prevent the reverse

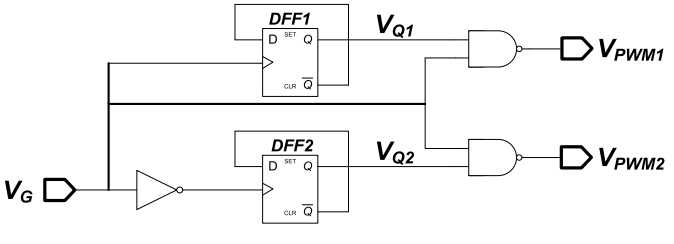


Fig. 10. Duty cycle control signal generator.

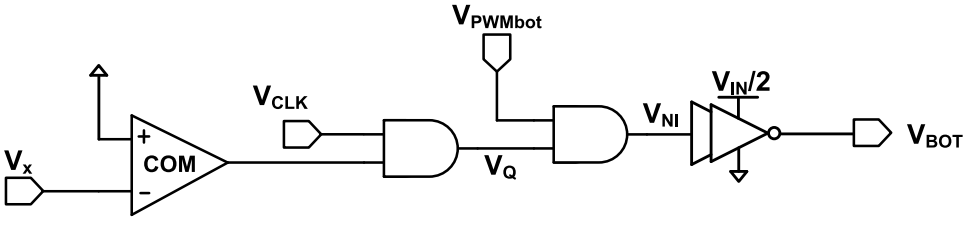


Fig. 11. Zero current detection scheme.

inductor current loss. Figure 11 shows the zero current scheme (zero current detection block in Fig. 8) for the TLB converter. When the inductor current decreases to zero, the voltage on node V_X increases from negative to zero. The comparator output becomes low, and then the V_{BOT} becomes low, turning off the power MOSFET $\mathrm{MN_{BOT}}$ to prevent the inductor current decreasing to negative value. The comparator for DCM control has a certain offset to cope with the propagation delay of the RS flip–flop, AND gate and the driver. The signal V_{CLK} is twice that of the switching frequency. Signal V_{CLK} turns on the $\mathrm{MN_{BOT}}$ at the beginning of every half switching cycle.

One of the main issues to be faced when addressing the microelectronic implementation of a switching power converter is the breakdown voltage (V_{max}) of the thin gate oxide of the power MOSFETs. As a consequence, the thick gate oxide transistors are usually used as power MOSFETs because of their thicker gate dielectric, at the expense of larger channel lengths.[3]

The self-driving scheme, which is shown in dashed green box of Fig. 1, is intended to solve the breakdown issue to allow the use of thin gate oxide transistors. The self-driving scheme comprises of three level shifters and four buffers. The power of top buffer is supplied by V_{IN} and $V_{\mathrm{IN}}/2$, the bottom one is supplied by $V_{\mathrm{IN}}/2$ and GND, the two middle buffers are supplied by the flying capacitor. So that the buffer and the power MOSFETS can be designed with thin oxide MOSFETs, which will save chip area.

Floating level shifters are used to shift the potential of control signals from circuits powered by low voltage power rails to the potential of circuits with floating power and ground rails. In this paper, a capacitive floating level shifter proposed in Ref. 20 is applied for the TLB converter. Figure 12 shows the schematic of the capacitive floating level shifter, which comprises of three parts, a latch holding the level shifted voltage, two coupling capacitors connected with the latched nodes, and two inverters driving the coupling capacitors. This type of capacitive level shifter is simpler, and the chip area, current consumption and propagation delay are also small. However, this capacitive level shifter may fail to operate if not designed properly. The design considerations for the capacitive floating level shifter can be referred to Ref. 17.

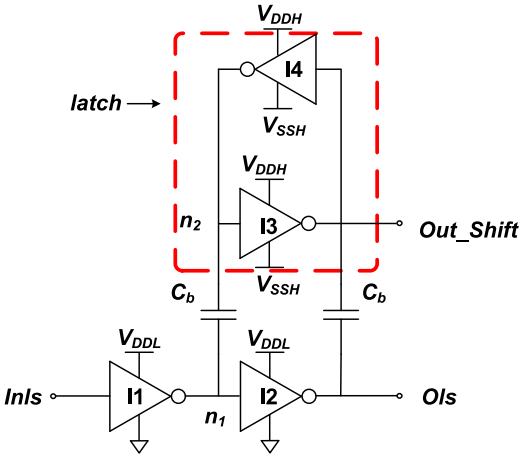


Fig. 12. Capacitive floating level shifter.[17]

8. Simulation Results

The TLB converter is built at transistor level in ST 65 nm CMOS technology. We present and discuss its corresponding simulation results in Cadence environment in this section. Table 4 summarizes the specification and parameters of the TLB converter. Figure 13 shows its operation and gate driving signal waveforms, the output voltage V_{OUT}, the inductor current I_L, the switching node voltage V_X and the gate driving signal of the four power MOSFETs, under a 50 mA output load current. These waveforms are identical to the previous analysis, as Fig. 2 shows.

Figure 14 shows the conversion efficiency and output voltage ripple from a 10–120 mA output load current under different process corners (TT, SS, SF, FF, FS). The maximum efficiency and ripple are 81.5% and 18.1 mV, respectively, at 120 mA load current.

Figure 15 shows the transient response with a load current step from 10 to 100 mA and from 100 to 10 mA. We obtained a result of 100 mV undershoot with 101 ns response time, and 86 mV overshoot with 110 ns response time.

Figure 16 shows the transient response with the same load current step change condition as in Fig. 15, only under different process corners (TT, SS, SF, FF, FS). The maximum undershoot is about 105 mV with 101 ns response time, and the

Table 4. System parameters of TLB converters.

V_{IN} (V)	f_{sw} (MHz)	C_f (nF)	L (nH)
2.4	100	10	5
C (nF)	R_L (Ω)	V_{OUT} (V)	Max. I_{OUT} (mA)
10	150 m	0.72	100

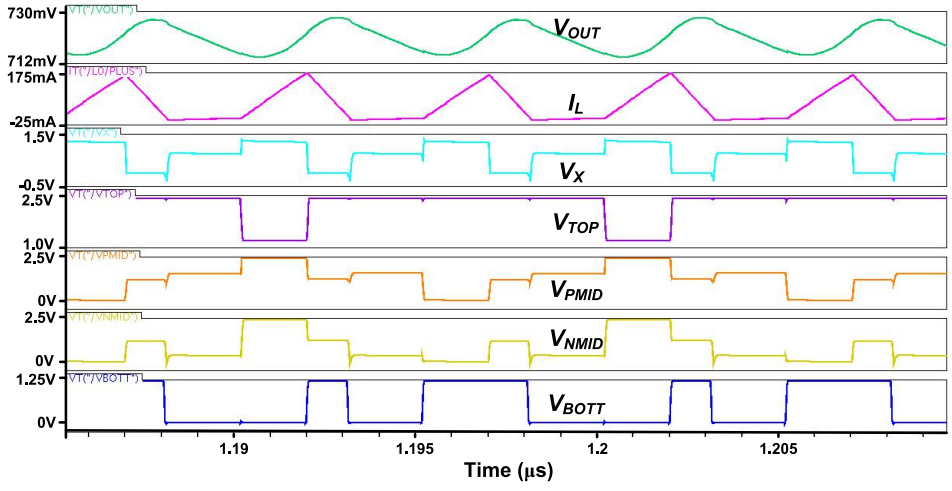


Fig. 13. Waveform of the TLB converter under 50 mA output load current, from top to bottom: output voltage V_{OUT}, inductor current I_L, switching node voltage V_X, power MOSFET $\mathrm{MP_{TOP}}$ gate voltage V_{TOP}, $\mathrm{MP_{MID}}$ gate voltage V_{MIDP}, $\mathrm{MN_{MID}}$ gate voltage V_{MIDN}, $\mathrm{MN_{BOT}}$ gate voltage V_{BOT}.

maximum overshoot is about 92 mV with 115 ns response time. We obtained almost the same load transient response under process variations.

Figure 17 shows the Monte-Carlo simulation results of the transient response with the same load current step change condition as in Fig. 15. The maximum undershoot is about 114 mV with 110 ns response time, and the maximum overshoot is about 110 mV with 150 ns response time. The TLB converter works well under different mismatch circumstances.

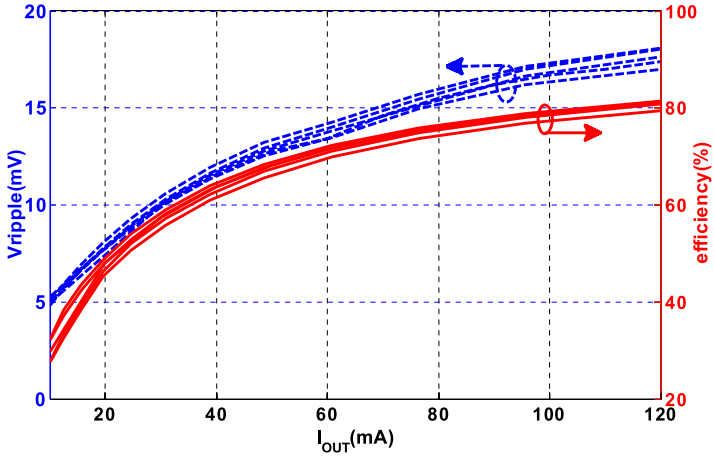


Fig. 14. Conversion efficiency and output voltage ripple versus output current under different corners (TT, SS, SF, FF, FS).

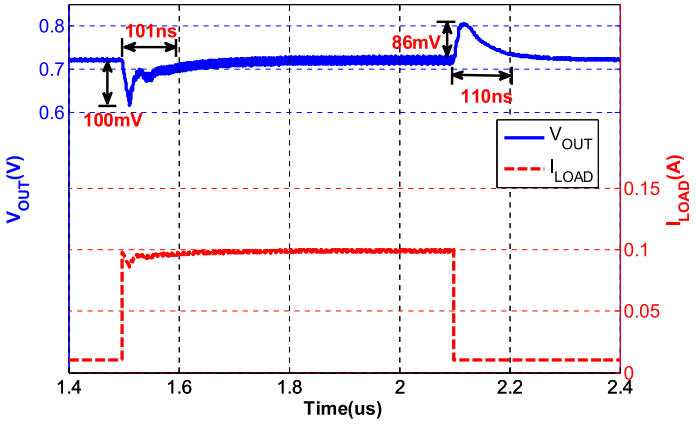


Fig. 15. Transient response of load current step from 10 to 100 mA.

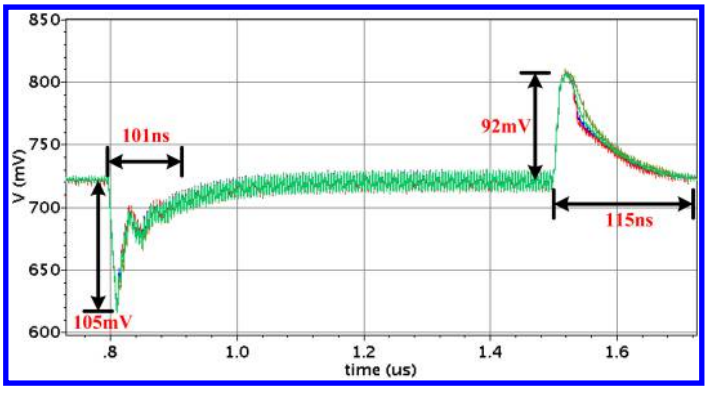


Fig. 16. Transient response of load current step from 10 to 100 mA, different corner simulation results (TT, SS, SF, FF, FS).

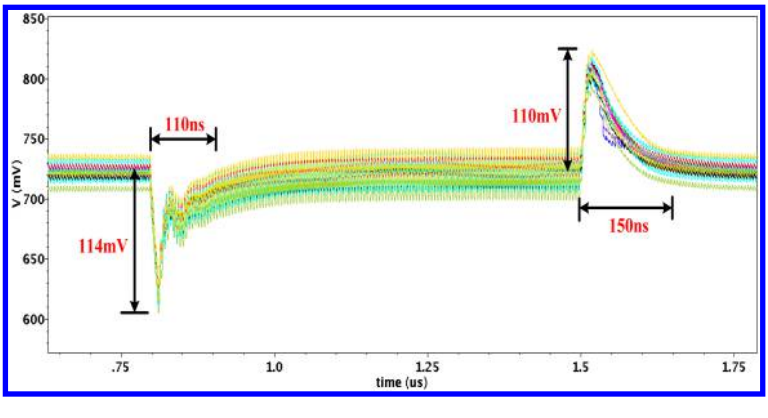


Fig. 17. Transient response of load current step from 10 to 100 mA, Monte-Carlo simulation results.

Table 5. Comparison with prior works of integrated DC–DC buck and TLB converters.

	Ref. 3	Ref. 10	Ref. 1	Ref. 21	Ref. 22	This work
Year	2008	2011	2013	2016	2017	2018
Types & Topology	3 Level Buck	3 Level Buck	Buck	Buck	Buck	3 Level Buck
Operating mode	DCM	CCM	DCM	CCM	CCM	DCM
Process/nm	250	130	130	65	65	65
V_{IN}/V	3.6	2.4	1.2	2–2.2	1.0	2.4
V_{OUT}/V	1	0.4–1.4	0.9	1.2	0.5–0.8	0.7–1.2
Max. I_{OUT}/mA	100	1000	370	700	180	120
P_{OUT}/mW	100	1000	330	840	126	144
f_{sw}/MHz	37.3	50–200	100	500	450	100
Phase	2	4	1	2	1	1
L/nH	26.73	4	5.5	1.54 (2)	1.8	5
C/nF	25.9	10	9.8	1.83	4	10
C_f/nF	5	18	—	—	—	10
Peak efficiency/%	69.7	77	83.2	76.2	76.1	**81.5**
Load transient step (mA)	—	220–370	10–100	200–700	90–180	10–100
V_{OUT} undershoot/ overshoot (mV)	—	80/100*	38/25	83/100	32/42	**100/86**
Settling time under/ over (ns)	—	70*/80*	400*/ 300*	100000*/ 150000*	2000*/ 2000*	**101/110**
Voltage ripple/mV (max)	49.4	150	75*	80	14.5	**18.1**
Level of Integration	bondwire	on-chip spiral	bondwire	on-chip spiral	on-chip spiral	bondwire

Note: *Estimated from the figure presented in corresponding paper.

Table 5 shows the comparison with prior works of the integrated DC–DC buck and the TLB converters. This work obtains 11.8% higher efficiency, 2.7x as small as the output voltage ripple with 5.3x as small as the inductance and 2.7x as small as the output capacitance when compared with the most similar TLB DCM work of Ref. 3. The efficiency, output voltage ripple and transient response are competitive when compared with the state-of-the-art works.

9. Conclusions

This paper first analyzed the DCM operation principle of the TLB converter, including the driving scheme using low-voltage power transistors, the CCM/DCM boundary, plus its DC and AC characteristics. The DCM voltage gain and small signal transfer function are different from the traditional two-level buck converter, even though they have the same CCM. Behavioral and Cadence transistor level simulation results verify the deduced DCM analysis, which is important for the closed-loop controller design of the TLB converter. Then, we discussed the design and control of a TLB converter under DCM operation, which we implemented using an ST 65 nm CMOS process. Transistor level simulation results show that it operates at 100 MHz with a 5 nH inductor, a 10 nF output capacitor and a 10 nF flying capacitor achieving an output conversion range of 0.7 to 1.2 V from a 2.4 V input

supply, with a peak efficiency of 81.5%@120 mW, an output load transient response of 100 mV with 101 ns for undershoot, and 86 mV with 110 ns for overshoot when $I_{\mathrm{OUT}} = 10/100$ mA and a maximum output voltage ripple of less than 19 mV.

Acknowledgments

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