A Multiphase Switched-Capacitor Converter for Fully Integrated AMLED Microdisplay System

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***Abstract*—A fully integrated switched-capacitor (SC) dc–dc converter is designed for powering up an active-matrix light-emitting diode (AMLED) microdisplay system. The stacking-transistor technique with three voltage conversion ratios is utilized to handle the lithium-ion battery range of 2.6–4.2 V and to reduce the switching loss. A 101-phase interleaving scheme is adopted such that, first, output voltage ripple $\Delta V_{\rm O}$ is significantly reduced; second, no external output capacitor is needed; and, third, SC power-cells are physically cascaded to encircle the LED array and drivers to reduce conduction loss. Two test chips were designed in the 0.18-μm 1P6M CMOS technology. The first chip is a test chip comprising the SC converter only. The output voltage is 4.2 V, and the measured maximum $\Delta V_{\rm O}$ is 52 mV. The measured power density is 74.4 mW/mm^2, peak efficiency is 81%, and maximum output power is 258 mW. The second chip is a system chip integrating the SC converter with the AMLED array and drivers using flip-chip packaging. The converter delivers a maximum power of 216 mW with a 78% peak efficiency in the SC mode and a 91% peak efficiency in the linear regulator mode.**

***Index Terms*—Active matrix, active-matrix light-emitting diode (AMLED), battery-connected, dc–dc converter, LED driver, microdisplays (μ-displays), multiphase interleaving, switched-capacitor (SC) converter, voltage regulator.**

I. Introduction

ACTIVE-MATRIX light-emitting diode (AMLED) microdisplays (μ-displays) have attracted great interests from both the industry and the academia. Recent advances in technology allow AMLEDs to have very high efficacy and reliability, making them suitable for flat panel displays of portable devices and for visible light communication [1]. Fig. 1(a) shows a generic LED microdisplay system. The AMLED array is usually fabricated in a gallium-nitride (GaN) process, whereas the column and row controller IC is fabricated in a silicon-based CMOS process. The AMLED array is then integrated on top of the silicon chip using the flip-chip bonding technology. The system power is usually externally supplied by a power management IC [2] that generates a higher voltage from a lithium-ion (Li-ion) battery. The external power supply not only increases component cost and volume, but also increases packaging complexity. Therefore, there is a strong motivation to further integrate the power management unit (PMU) with the controller IC, such that the fully integrated AMLED microdisplay system could be directly connected to the Li-ion battery, as shown in Fig. 1(b).

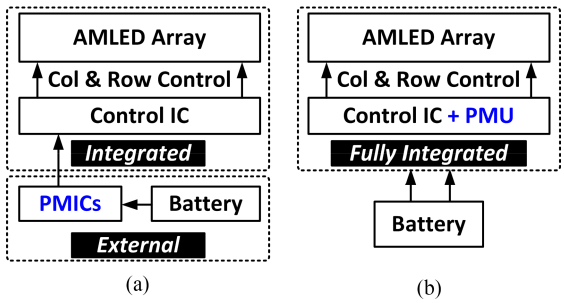

Fig. 1. Structure of AMLED microdisplay system driven by (a) external power management ICs and (b) integrated PMU.

The AMLED array needs a voltage higher than the Li-ion battery voltage, and step-up switched-capacitor (SC) converters (also known as charge pumps) [3]–[6] are good candidates, as capacitors are cheaper and smaller than inductors for low-power applications. In recent years, fully integrated SC converters have been widely reported with improved power density and power efficiency [7]–[10]. Technology scaling offers faster switching frequency, lower parasitic, and higher capacitance density. However, the core transistors have low voltage stress, and these converters are thus limited to low-voltage applications.

The voltage of the popular Li-ion battery ranges from 2.6 to 4.2 V. Thick-oxide I/O devices can withstand such battery voltage, but they have large parasitic gate capacitance and thus large switching loss. Core-transistors with the same turn-ON resistance have much smaller size but have a much lower voltage rating. Cascoding or stacking transistors assisted by auxiliary voltage rails could reduce voltage stress. In [11], an 11/1$\times$ topology was proposed to convert a high voltage (35–40 V) to 3.3 V, using four flying capacitors. In [12] and [13], Dickson ladder topologies were employed, and voltages across the switches were reduced by the series connection of the capacitors. In [14], six thin-oxide transistors were used in a cascode such that the SC converter in

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65-nm CMOS could be directly connected to the battery. In [5], two auxiliary voltage rails (5.5 and 10.5 V) were generated externally to prevent the transistors from breaking down. Each of the above methods requires careful design according to individual voltage specifications.

The pixels of an AMLED array are common-cathode connected to the output of the power converter, and their brightness is very sensitive to the output ripple voltage. Hence, it is also crucial to reduce the output voltage ripple using minimum ON-chip and no OFF-chip capacitors. Multiphase interleaving is an effective method to achieve low-voltage ripples with small load capacitance. SC converters with many phases have been implemented, such as 16 phases in [15], 32 phases in [7] and [16], and 41 phases in [17]. An H-tree structure is usually adopted for the layout floorplan to minimize phase mismatch, but it also limits the number of phases (e.g., larger than 100) that can be used.

To address the above concerns, this article proposes a fully integrated SC converter to power up an AMLED microdisplay. First, thin-oxide transistors are stacked to handle high voltage and reduce switching loss, so high power efficiency is achieved. Three reconfigurable voltage conversion ratios (VCRs) (2×, 3/2×, and 4/3×) are utilized to obtain good efficiencies over wide input- and output-voltage ranges. A power-cell ring structure is used to distribute power to the loads in the center. It consists of 101 interleaving phases with a flexible layout that optimize the usage of the flying/decoupling capacitors and minimize the output voltage ripple. Benefits and design considerations of the ring structure were further investigated in [18].

The remainder of this article is organized as follows. Section II discusses system considerations, including the layout floorplan and voltage stress requirements. Section III proposes an efficiency optimization method and compares the thin- and the thick-oxide transistor structures. Section IV expounds on circuit implementation. Section V presents the measurement results. Section VI concludes this article.

II. System Considerations

A. System Structure and Layout Consideration

Fig. 2(a) shows the system diagram of the microdisplay system. The SC converter provides the supply voltage $V_{\rm O}$ to all the pixel drivers and the common-cathode AMLED array. The turning ON–OFF of each LED pixel is controlled by the pixel driver. The vertical construction of the microdisplay system is shown in Fig. 2(b). The AMLED array with column and row pixels is fabricated using a GaN process and is placed on the top layer. The driver circuit along with the PMU is fabricated using a standard CMOS process and placed on the bottom layer. The pixel size is 40 μm × 40 μm, and the LED on the top chip is connected to the driver on the bottom chip using flip-chip packaging technique; the PMU forms a ring around the driver matrix in the center. The current of each pixel can be independently controlled through digital codes.

The brightness of an LED is very sensitive to the variation of the supply voltage, and the PMU is required to deliver a uniform voltage to all pixels. A multiphase SC converter, consisting of

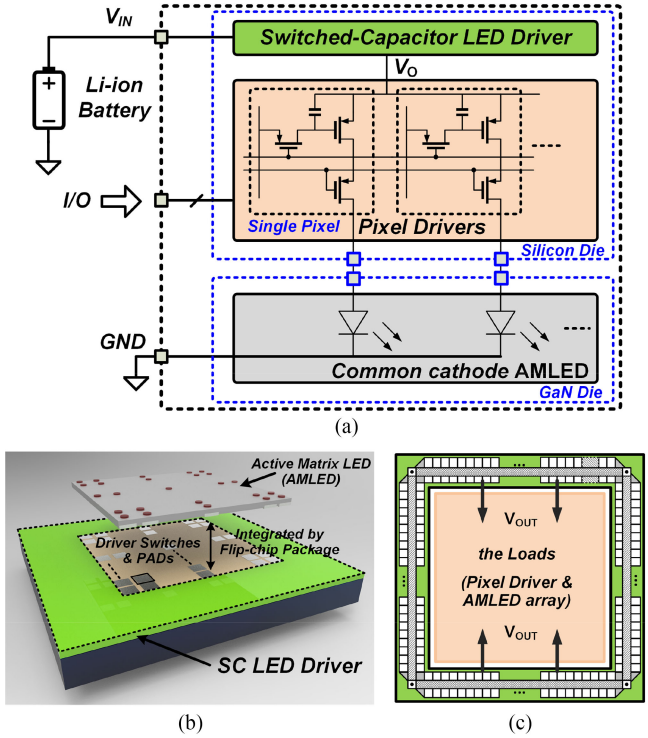


Fig. 2. (a) System diagram of proposed fully integrated AMLED microdisplay system. (b) Vertical construction of AMLED microdisplay system. (c) Central-driver and peripheral-PMU layout of SC converter.

power cells physically cascaded as a ring, encircles the central LED-driver matrix and is thus used as the PMU (see Fig. 2(c)), such that current can be delivered over the shortest path with the lowest resistance from the $V_{\rm OUT}$ bus. Thick power rails are laid in between the drivers to reduce the *IR* drop.

In this work, two test chips have been designed. The first is a test chip used to verify the functionality of the proposed SC converter, and a total of 101 power cells are used to deliver a maximum load current of 60 mA. The maximum current of each power cell is 600 μA. Second is the complete μ-display system that includes the PMU, drivers, and LED pixels. The LED matrix of 64 × 36 pixels (16:9) is encircled by 87 power cells, and a maximum current delivered by each power cell is increased to 690 μA.

B. Multiphase Interleaving and Benefits of Ring Structure

Multiphase interleaving has been widely used in fully integrated SC converters [7], [15]–[19]. Fig. 3 shows the concept and system diagram. Multiphase interleaving is implemented by partitioning the SC converter into multiple small cells, and these power cells are driven by different clocks (ck_1 to ck_n). Adjacent clocks have a 360°/*n* phase shift and *T*/*n* delay, where *T* is the switching clock period, such that the output voltage effectively has a higher frequency and the output voltage ripple can be reduced. An *n*-phase voltage controlled oscillator (VCO) is used to generate these clock signals. To regulate $V_{\rm OUT}$, frequency modulation is used. $V_{\rm OUT}$ is sensed by an error amplifier (EA) to generate the error signal V_C to adjust the switching frequency.

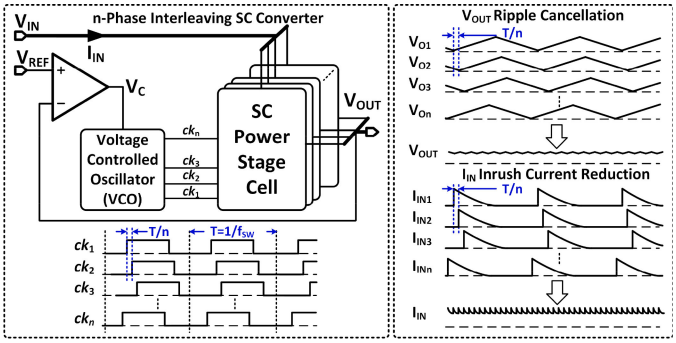


Fig. 3. Concept and system diagram of multiphase interleaving SC converter.

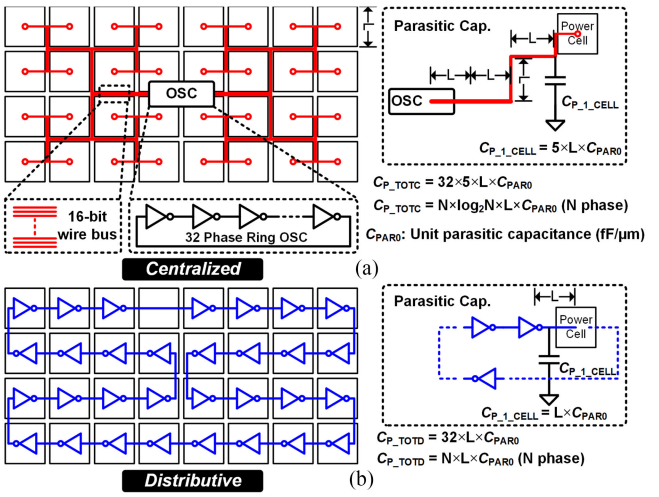


Fig. 4. Comparison between clock generation and distribution, and parasitic capacitance on the routing wires of (a) centralized scheme and (b) distributive scheme.

Besides reducing the output voltage ripple, the input current ($I_{\rm IN}$) ripple is also significantly reduced as the discontinuous input inrush current of a single-phase converter is evenly distributed among many phases for an interleaving converter. Consequently, both the input and output capacitance can be much reduced. As such, more interleaving phases are beneficial and preferred in recent works [17]–[19]. However, generating a large number of clock phases is still challenging.

Two schemes of clock generation and clock distribution are shown in Fig. 4. Fig. 4(a) shows the H-tree structure with centralized clock distribution that is commonly used in large digital circuits and systems. For a multiphase SC converter, each power cell needs one clock path from the central voltage-controlled oscillator (VCO), and N phases will need an N-bit clock bus running through the whole converter, complicating the design. Moreover, to ensure phase matching, the layout of the power cells has to be symmetrical, and the form factor of the PMU is restricted to be rectangular. To distribute the clock phases to each power cell, they have to be routed from the central VCO to the power cells with a parasitic capacitor $C_{P\_1\_\rm CELL} = \log_2 N \times L \times C_{\rm PAR0}$ where N is the phase number and $C_{\rm PAR0}$ is the unit parasitic capacitance in fF/μm. The total parasitic capacitance of all the clock wires that are driven by the VCO is $C_{P\_\rm TOTC} = N \times \log_2 N \times L \times C_{\rm PAR0}$. Hence, power consumption for the clock distribution is large, and the number of clock phases is usually under 50 [7], [15]–[17], [19].

For the distributive scheme of Fig. 4(b) the power cells are designed to be identical, and adjacent power cells generate clock phases that bear a fixed delay with respect to the preceding one. Connecting N such cells (N is an odd number) in a ring forms a ring oscillator. Each power cell supplies power to the power rails that run through the whole converter surrounding the central load. When compared to the H-tree scheme, the distributive clock paths are shorter, so the parasitic capacitance along the clock wire is $C_{P\_\rm TOTD} = N \times L \times C_{\rm PAR0}$, that is much smaller, and power consumption of the VCO is much lower. Meanwhile, the power cells are not restricted to residing on the peripheral of the chip but can run through the components where power is needed, as long as the connected power cells form a ring. The switching frequency of the power ring is affected by the total parasitic capacitance along the clock routing path, and the inverters should be sized accordingly.

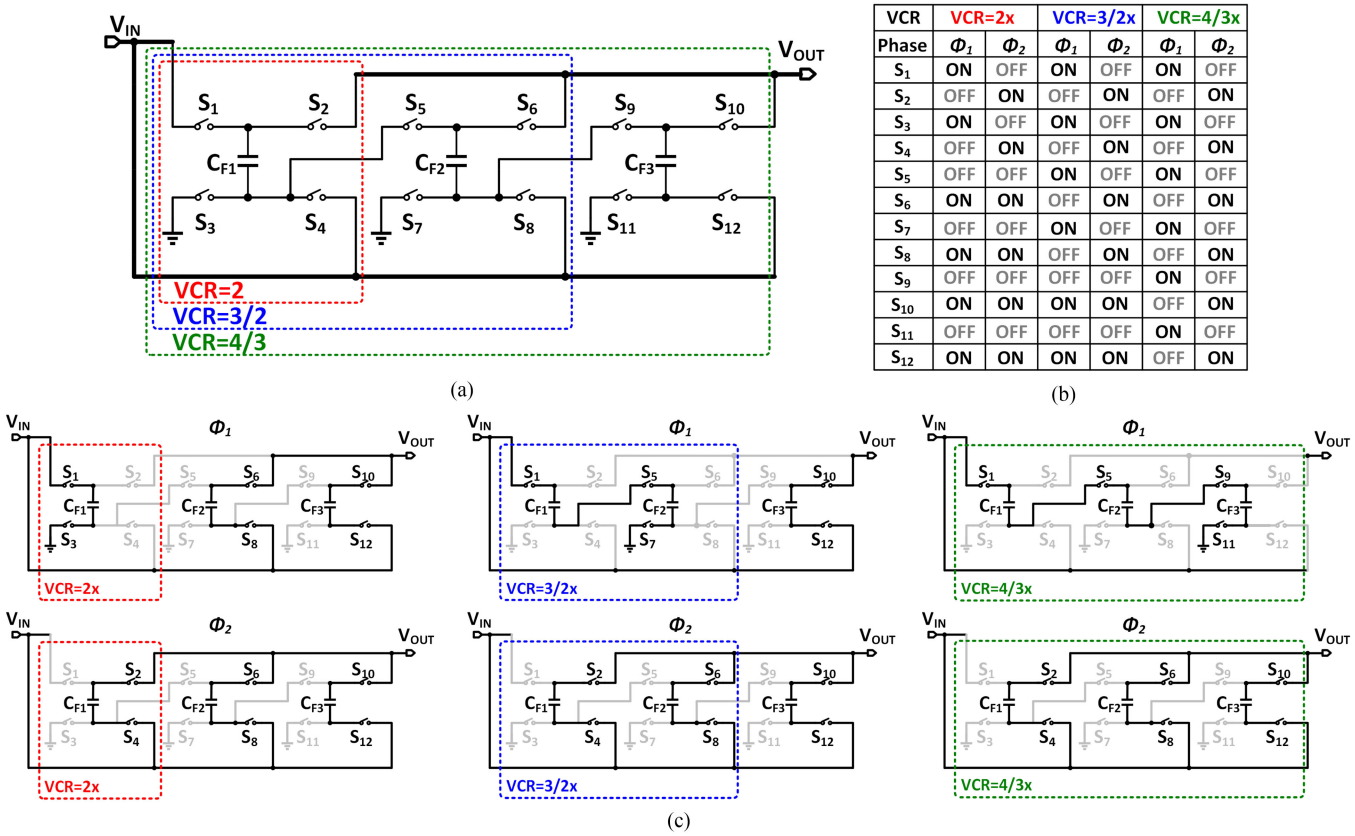
C. Power Stage Design and Voltage Stress Requirements

For an SC converter, the theoretical efficiency is

$$\eta = \frac{V_{\rm OUT}}{M \times V_{\rm IN}} \tag{1}$$

where M is the VCR. This means that higher efficiency is achieved when $V_{\rm OUT}$ is close to the ideal output voltage $MV_{\rm IN}$. Therefore, it is important that the power cells can be reconfigured to many VCRs to cater for a changing input voltage. For example, an Li-ion battery is 4.2 V when fully charged and 2.6 V when completely discharged. For the AMLED application, an output voltage $V_{\rm OUT}$ of 4.2 V is needed to drive the LED pixels and the driver switches. The decision is to use three step-up VCRs (2×, 3/2×, and 4/3×) as a compromise between the number of VCRs, the number of flying capacitors, and the complexity of the switches.

Fig. 5 shows a simplified schematic and operating principle of the reconfigurable SC power stage that consists of 12 switches (S_1 to S_{12}) and three flying capacitors (C_1, C_2, and C_3) to realize three VCRs. The ON–OFF status of each switch is listed in Fig. 5(b). The operating principles of three VCRs are shown in Fig. 5(c). Each mode operates with a two-phase clock. For 2× mode, in Φ_1 the flying capacitor C_{F1} is connected between $V_{\rm IN}$ and ground, and $V_{\rm CF1} = V_{\rm IN}$. In Φ_2, C_{F1} is stacked on top of $V_{\rm IN}$, and in parallel with $V_{\rm OUT}$, thus we have $V_O = V_{\rm IN} + V_{C1} = 2 \times V_{\rm IN}$. Similarly for 3/2× and 4/3× modes, in Φ_1, the flying capacitors are in series between $V_{\rm IN}$ and ground, so $V_{\rm CF1,\,F2} = 1/2 \times V_{\rm IN}$ (3/2 × mode), and $V_{\rm CF1,\,F2,\,F3} = 1/3 \times V_{\rm IN}$ (4/3 × mode). Then in Φ_2, some flying capacitors are stacked on top of $V_{\rm IN}$, so for 3/2× mode, $V_{\rm OUT} = V_{\rm IN} + 1/2 \times V_{\rm IN} = 3/2 \times V_{\rm IN}$; and for 4/3× mode, $V_{\rm OUT} = V_{\rm IN} + 1/3 \times V_{\rm IN} = 4/3 \times V_{\rm IN}$. Unused flying capacitors in 2× and 3/2× modes are connected between $V_{\rm OUT}$ and $V_{\rm IN}$ as decoupling capacitors.



VCR	VCR=2x		VCR=3/2x		VCR=4/3x	
Phase	Φ_1	Φ_2	Φ_1	Φ_2	Φ_1	Φ_2
S_1	ON	OFF	ON	OFF	ON	OFF
S_2	OFF	ON	OFF	ON	OFF	ON
S_3	ON	OFF	ON	OFF	ON	OFF
S_4	OFF	ON	OFF	ON	OFF	ON
S_5	OFF	OFF	ON	OFF	ON	OFF
S_6	ON	ON	OFF	ON	OFF	ON
S_7	OFF	OFF	ON	OFF	ON	OFF
S_8	ON	ON	OFF	ON	OFF	ON
S_9	OFF	OFF	OFF	OFF	ON	OFF
S_{10}	ON	ON	ON	ON	OFF	ON
S_{11}	OFF	OFF	OFF	OFF	ON	OFF
S_{12}	ON	ON	ON	ON	OFF	ON

Fig. 5. (a) Simplified schematic of power stage. (b) ON–OFF status of each switch in three VCRs. (c) Operating principle of three-ratio configurations.

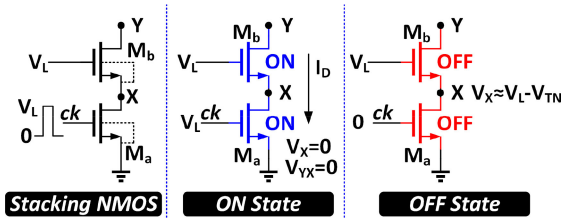


Fig. 6. Operating principles of NMOS stacking transistors.

TABLE I
VOLTAGE RATING REQUIREMENTS OF SWITCHES

VCRs	2×	3/2×	4/3×	Implementation
	V_{DS}	V_{DS}	V_{DS}	
S_1	V_{OUT}-V_{IN}	V_{OUT}-V_{IN}	V_{OUT}-V_{IN}	Thin-oxide NMOS
S_2	V_{OUT}-V_{IN}	V_{OUT}-V_{IN}	V_{OUT}-V_{IN}	Thin-oxide PMOS
S_3	V_{IN}	V_{IN}	V_{IN}	NMOS stacking
S_4	V_{IN}	V_{IN}	V_{IN}	PMOS stacking
S_5	V_{OUT}	V_{OUT}-V_{IN}	V_{OUT}-V_{IN}	Thick-oxide NMOS
S_6	N/A	V_{OUT}-V_{IN}/2	V_{OUT}-V_{IN}/3	PMOS stacking
S_7	V_{IN}	V_{IN}	V_{IN}	NMOS stacking
S_8	N/A	V_{IN}	V_{IN}	PMOS stacking
S_9	V_{OUT}	V_{OUT}	V_{OUT}	Thick-oxide NMOS
S_{10}	N/A	N/A	V_{OUT}-V_{IN}/3	PMOS stacking
S_{11}	V_{IN}	V_{IN}	V_{IN}	NMOS stacking
S_{12}	N/A	N/A	V_{IN}	PMOS stacking

To determine which VCR is to be used, the ratio $V_{\rm OUT} - V_{\rm IN}$ is sensed by comparators. Let $V_{\rm OUT} = 4.2$ V, the VCR assignment is as follows: VCR $= 2\times$ for 2.6 V $< V_{\rm IN} <$ 3.2 V; VCR $= 3/2\times$ for 3.2 V $< V_{\rm IN} <$ 3.6 V; and VCR $= 4/3\times$ for 3.6 V $< V_{\rm IN} <$ 4.2 V. Voltage margins are reserved between adjacent modes to compensate for the $V_{\rm OUT}$ drop caused by the output resistance $R_{\rm OUT}$ of the SC converter. Also, hysteresis windows are implemented to avoid frequent transitions at boundary values.

Thin-oxide transistors have low turn-ON resistance and low switching loss, so they are used in the power stage. These transistors are stacked to withstand high voltage, as shown in Fig. 6. Consider two NMOS transistors M_a and M_b that are cascode-connected, both with maximum operating voltages of 2 V for $V_{\rm DS}$, $V_{\rm GS}$, and $V_{\rm BS}$. In the steady-state, the gate of M_b is biased by a dc voltage V_L. In the ON state, the gate voltage of M_a $V_{\rm GSa}$ is raised to V_L, and M_a and M_b are turned ON, so both $V_{\rm DSa}$ and $V_{\rm DSb}$ are zero. In the OFF state, $V_{\rm GSa}$ is low, as $V_{\rm DSa}$ is restricted to $V_L - V_{\rm THb}$, and hence M_a is protected. Now, $V_{\rm DSb}$ of M_b is $V_Y - (V_L - V_{\rm THb})$. The body of M_a and M_b are connected to their respective sources. In summary, this structure can withstand double of the transistor's normal operating voltage in both states.

Table I summarizes the voltage rating requirements of the switches under each VCR. For S_1 and S_2, their maximum $V_{\rm DS}$ does not exceed 2 V, and thin-oxide transistors can be used. For S_3 to S_{12}, their $V_{\rm DS}$ can be higher than 2 V. NMOS stacking transistors are used to implement S_3, S_7, and S_{11} as they are

TABLE II
SUMMARY OF EQUIVALENT OUTPUT IMPEDANCE OF THREE VCRS

VCRs	K_C	R_{SSL}	K_S	R_{FSL}
2×	1	$\frac{1}{C_F f_{SW}}$	4	$4R_{ON}$
3/2×	$\frac{1}{2}$	$\frac{1}{2C_F f_{SW}}$	$\frac{7}{2}$	$\frac{7}{2}R_{ON}$
4/3×	$\frac{1}{3}$	$\frac{1}{3C_F f_{SW}}$	$\frac{20}{9}$	$\frac{20}{9}R_{ON}$

TABLE III
SWITCHING LOSS CALCULATIONS

Type	NMOS		PMOS	
	Low-V	High-V	Low-V	High-V
L_{MIN} (μm)	0.18	0.7	0.18	0.5
K (1m/ΩV)	0.147	0.138	0.048	0.03
C_{GATE} (fF/L_{MIN})	0.52	0.82	0.62	0.62
W_H/W_L	**0.829×**		**0.889×**	
P_{SW_H}/P_{SW_L}	**2.615×**		**1.778×**	

The last two rows are very conclusive numbers to the analysis part.

connected to ground; PMOS stacking transistors are used to implement S_1, S_4, S_8, S_{12}, S_2, S_6, and S_{10}, as their sources are referenced to $V_{\rm IN}$ and/or $V_{\rm OUT}$; and for S_5 and S_9, as their sources are floating, thick-oxide transistors are used.

Next, we consider the flying capacitors. For VCR $= 2\times$, C_{F1} is charged directly by $V_{\rm IN}$ and a thick-oxide MOS capacitor should be used, whereas C_{F2} and C_{F3} are connected between $V_{\rm IN}$ and $V_{\rm OUT}$. For VCR $=$ 3/2× or 4/3×, V_{C2} and V_{C3} are lower than 2 V due to the series connection, and thin-oxide MOS capacitors are used.

III. ANALYSIS AND OPTIMIZATION OF THE SC CONVERTER

In order to achieve optimal efficiency and power density, a power loss analysis is conducted.

A. Power Loss Analysis

An SC converter can be modeled as an ideal dc voltage source with a finite output resistance $\rm R_{OUT}$ [7], [20], that is composed of $R_{\rm SSL}$ (slow switching limit resistance related to charge redistribution loss) and $R_{\rm FSL}$ (fast switching limit resistance due to finite conductance of switches), given by

$$R_{\rm SSL} = K_C \frac{1}{C_F f_E} \tag{2}$$

$$R_{\rm FSL} = K_S R_{\rm ON} \tag{3}$$

where K_C and K_S are topological factors determined by the charging scenario, C_F is the flying capacitor, $f_{\rm SW}$ is the switching frequency, and $R_{\rm ON}$ is the turn-ON resistance of the switches. A two-phase clock is used. All $R_{\rm ON}$ are designed to be equal, as they conduct the same amount of charge. Table II summarizes K_C and K_S for the three VCRs. The major loss is due to the equivalent *IR* drop of $R_{\rm OUT}$, and from (2) and (3), to reduce $R_{\rm OUT}$ loss, high $f_{\rm SW}$, and large transistor width $W_{\rm SW}$ are needed.

The switching loss and parasitic loss are also significant [7]. The switching loss of the power transistors is given by

$$P_{\rm SW} = V_{\rm SW}^2 f_{\rm SW} C_{\rm GATE} N W_{\rm SW} \tag{4}$$

where $V_{\rm SW}$ is the voltage swing of the driver, $C_{\rm GATE}$ is the capacitance density (in fF/μm, and transistors have minimal channel length), and N is the number of transistors used. To achieve higher power density MOS capacitors are used, and the associated parasitic loss is given by

$$P_{\rm PAR} = \alpha C_F \lambda V_{DD}^2 f_{\rm SW} \tag{5}$$

where α is the percentage of the bottom-plate capacitance (around 5%), and λ is a topology (VCR) dependent factor.

Clearly, switching loss and parasitic loss are proportional to the switching frequency $f_{\rm SW}$ and the transistor width $W_{\rm SW}$, whereas conduction ($R_{\rm OUT}$) loss is inversely proportional to $f_{\rm SW}$ and $W_{\rm SW}$. Hence, there is a tradeoff between these two parameters.

B. Power Loss Reduction by Stacking Transistors

The turn-ON resistance $R_{\rm ON}$ of a MOS transistor is given by

$$R_{\rm ON} = \frac{L_{\rm MIN}}{K V_{\rm OD} W_{\rm SW}} \tag{6}$$

where K is a process parameter, $V_{\rm OD}$ is the overdrive voltage of the gate, and $L_{\rm MIN}$ is the minimum channel length. A power switch can be implemented using one thick-oxide transistor or two stacking thin-oxide transistors. If the two implementations have the same $R_{\rm ON}$, then for each type of transistor

$$R_{\rm ON\_L} = \frac{1}{2} R_{\rm ON\_H}. \tag{7}$$

Considering (6) and (7) together, the size ratio of the thick-oxide transistor to thin-oxide transistor is

$$\frac{W_{\rm SW\_H}}{W_{\rm SW\_L}} = \frac{L_H}{2L_L} \frac{K_L V_{\rm OD\_L}}{K_H V_{\rm OD\_H}}. \tag{8}$$

Now, the switching loss is given by

$$P_{\rm SW} = V_{\rm SW}^2 f_{\rm SW} C_{\rm GATE} W_{\rm SW}. \tag{9}$$

Hence, the ratio of their switching losses is

$$\frac{P_{\rm SW\_H}}{P_{\rm SW\_L}} = \frac{V_{\rm SW\_H}^2 C_{\rm GATE\_H} W_{\rm SW\_H}}{2V_{\rm SW\_L}^2 C_{\rm GATE\_L} W_{\rm SW\_L}}. \tag{10}$$

In this design, the lengths are $L_H = 0.5\,\mu$m for NMOS, $L_H = 0.7\,\mu$m for PMOS, and $L_L = 0.18\,\mu$m. The overdrive voltages are $V_{\rm OD\_H} = 3$ V and $V_{\rm OD\_L} = 1.2$ V. Other parameters are extracted from the process and listed in Table III. The results show that after using low-voltage transistors, switching loss reduction of 2.615× and 1.778× could be achieved for the NMOS and PMOS switches, respectively.

C. Efficiency Optimization

The total power loss can be obtained by summing (2)–(5)

$$\begin{aligned} P_{\rm LOSS} &= P_{\rm SSL} + P_{\rm FSL} + P_{\rm SW} + P_{\rm PAR} \\ &= R_{\rm SSL} I_O^2 + R_{\rm FSL} I_O^2 + V_{\rm SW}^2 f_{\rm SW} C_{\rm GATE} N W_{\rm SW} \\ &\quad + \alpha C_F f_{\rm SW} \lambda V_{DD}^2. \end{aligned} \tag{11}$$

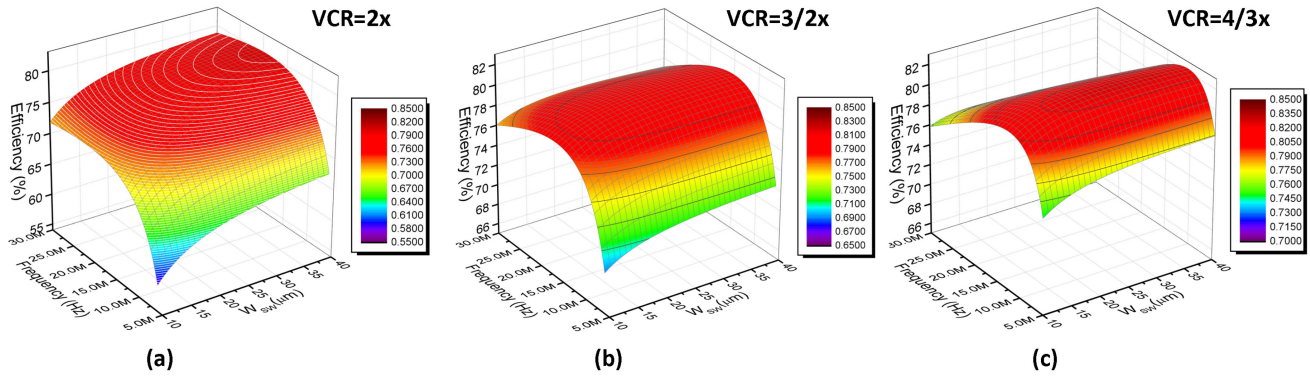


Fig. 7. Simulated efficiency with respect to switching frequency $f_{\rm SW}$ and width of power transistor width $W_{\rm SW}$.

The overall efficiency can thus be obtained as

$$\eta\left(f_{\rm SW}, W_{\rm SW}\right) = \frac{P_O}{P_O + P_{\rm LOSS}}. \tag{12}$$

For different power transistors, the respective parameters $V_{\rm SW}$, $C_{\rm GATE}$, and N are used, and the $W_{\rm SW}$ of the thick-oxide transistors are normalized to the $W_{\rm SW}$ of the thin-oxide transistors.

The maximum loading of one power cell I_O and the flying capacitor value C_F are designed according to the total load and the area of the load. The resultant design should have adequate interleaving phases but not too many power cells. In this design, I_O is set at 600 μA. Equation (11) shows that most of the parameters are determined by the CMOS process and the VCR topologies, and only $f_{\rm SW}$ and $W_{\rm SW}$ are determined by the circuit designer.

Efficiency calculation and simulation were conducted using MATLAB, and to obtain the peak efficiency of each VCR, $f_{\rm SW}$ and $W_{\rm SW}$ were swept from 10 to 30 MHz and from 10 to 40 μm, respectively. The results are shown in the three-dimensional curves of Fig. 7. For the 4/3$\times$ mode (see Fig. 7(c)), the peak efficiency is 82.5% when $f_{\rm SW}$ is 11.3 MHz and $W_{\rm SW}$ is 27.5 μm. For the 3/2$\times$ mode (see Fig. 7(b)), the peak efficiency is 80.5% when $f_{\rm SW}$ is 15.7 MHz and $W_{\rm SW}$ is 33.94 μm. The optimal $f_{\rm SW}$ for the 3/2$\times$ mode is higher than the optimal $f_{\rm SW}$ of the 4/3$\times$ mode because fewer transistors are used; as switching loss is lower, larger transistors can be used.

For the 2$\times$ mode, the peak efficiency is 80% when $f_{\rm SW} = 19$ MHz and $W_{\rm SW} = 40$ μm. This mode uses the lowest number of transistors, and switching and parasitic losses are significantly lower than the other two modes; hence, both $f_{\rm SW}$ and $W_{\rm SW}$ can be larger. However, Table II shows that K_C and K_S are much larger than those in the other modes, and $R_{\rm OUT}$ loss limits the peak efficiency to 80%. In practice, the 2$\times$ mode is used when $V_{\rm IN}$ is lower than 3.2 V, and (1) dictates that the efficiency is limited by the regulated voltage and is $\sim$70%. But the relatively low efficiency is not a concern as it is rather rare for $V_{\rm IN}$ to be as low as 3.2 V. Taking all factors into consideration, the final transistor size is chosen to be 30 μm and the middle value between the 4/3$\times$ mode and 3/2$\times$ mode. With $W_{\rm SW} = 30$ μm, when switching at 15 MHz in the 4/3$\times$ mode, the switching losses of the high- and low-voltage transistors are 35.2 and 20.1 mW, respectively. Hence, when delivering the full power of 258 mW, the improvement in efficiency is 5.85%.

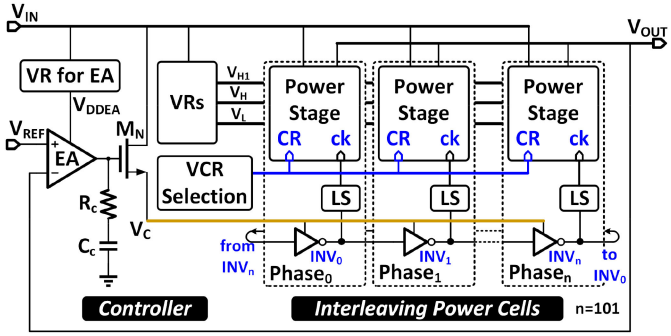


Fig. 8. System diagram of proposed SC dc–dc converter.

IV. Circuit Implementation

A. System Architecture

Fig. 8 shows the system architecture of the proposed SC converter. It consists of a controller and a ring of power cells. In the controller, the VCR selection block senses $V_{\rm REF}/V_{\rm IN}$ and then issues the proper VCR selection bits to the power cells. The supply voltages for the drivers of the stacking transistors of the power stage are internally regulated and the supply voltage for the EA is also preregulated by a voltage regulator. In the first test chip, 101 phases are implemented. In the second test chip, the phase number was adjusted to 87 according to the AMLED loading requirement.

The output voltage is regulated through using frequency modulation. Each power cell generates its own clock-phase by its *in-situ* VCO, and an odd number of clock-phases are connected as a ring structure. The frequency of the VCO is controlled by the EA's output voltage V_C. To ensure supplying adequate current for the ring oscillator and to avoid having a low-frequency pole at the V_C node, an NMOS source follower is inserted. The number of power cells can be adjusted according to the loading

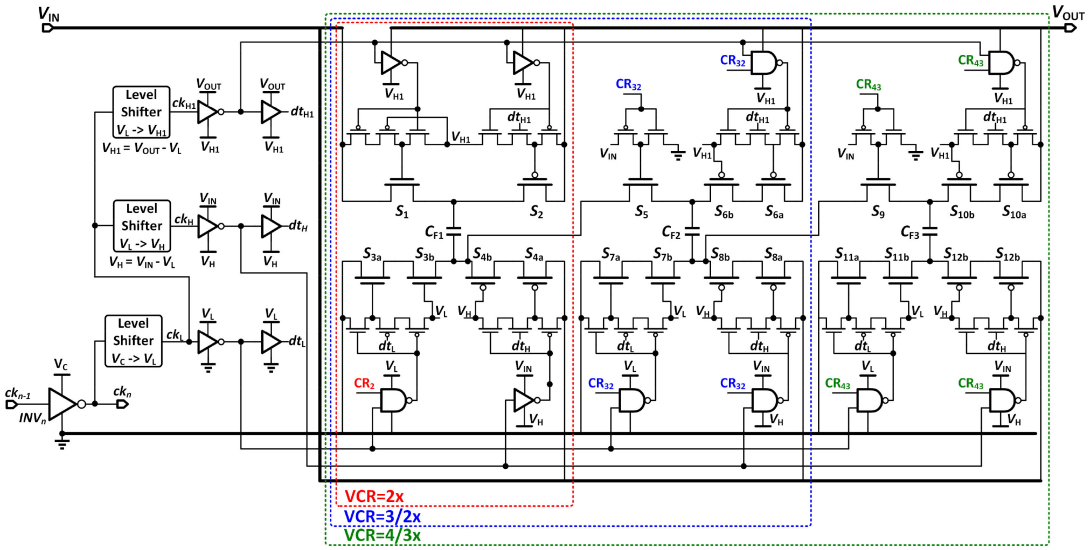


Fig. 9. Transistor level schematic of one power cell (phase-n).

requirement. The first chip consists of only the SC converter with 101 power cells, and each power cell can deliver a maximum current of 600 μA to support a full load of 60 mA. The second chip consists of both the LED driver matrix and the SC converter. There are 87 power cells that encircle the driver matrix, and the maximum current of each power cell is increased to 690 μA.

B. Power Stage With Stacking Transistors

Fig. 9 shows the transistor level schematic of one power cell. The power cell consists of 12 transistors (S_1–S_{12}) and three flying capacitors (C_{F1}–C_{F3}). Three selection bits (CR_{12}, CR_{23}, and CR_{34}) are used to configure the VCR to 2×, 3/2×, and 4/3×.

The flying capacitors (C_{F1}, C_{F2}, and C_{F3}) are realized by on-chip MIM and MOS capacitors, achieving a total capacitance density of around 10 fF/μm^2 with thin-oxide MOS capacitors (C_{F2} and C_{F3}), and 7 fF/μm^2 with thick-oxide MOS capacitors (C_{F1}). Each flying capacitor is 33 pF. Since C_{F2} and C_{F3} are thin-oxide MOS capacitors, to limit their voltage stress, they cannot work in parallel with C_{F1} in 2× mode. To increase the utilization of on-chip capacitors, C_{F2} or C_{F3} are connected between $V_{\rm OUT}$ and $V_{\rm IN}$ to serve as decoupling capacitors when not taking part in charge/power transfer.

Table I shows how the power switches are implemented. The switches $S_{3–4}$, $S_{6–8}$, and $S_{10–12}$ are implemented with stacking transistors. The gates of the transistors S_{xb} ($x = 3$–4, 6–8, 10–12) are connected to a fixed bias voltage. The bias voltages (V_L, $V_H = V_{\rm IN} - V_L$, and $V_{H1} = V_{\rm OUT} - V_L$) are generated from internal voltage regulators. The digital logic operates in the voltage domains (0, V_L), (V_H, $V_{\rm IN}$), and (V_{H1}, $V_{\rm OUT}$) powered by internal voltage supplies as well. For NMOS transistors, their body terminals are connected to their sources and isolated from the p-substrate with deep N-well. S_5 and S_9 are thick-oxide transistors.

The inverter INV_n of the VCO uses the clock phase ck_{n-1} from the previous stage to generate an additional interleaving clock phase ck_n (built inside INV_n) to drive the current power cell. The clock phase ck_n is level-shifted to generate three clocks (ck_L, ck_H, and ck$_{H1}$) in three different voltage domains, followed by buffering drivers. To eliminate shoot-through current, the switches are driven by three-transitor (3T) based NAND gate with the sandwiched transistors driven by dead-time signals (dt_L, dt_H, and dt_{H1}) from the delay cells.

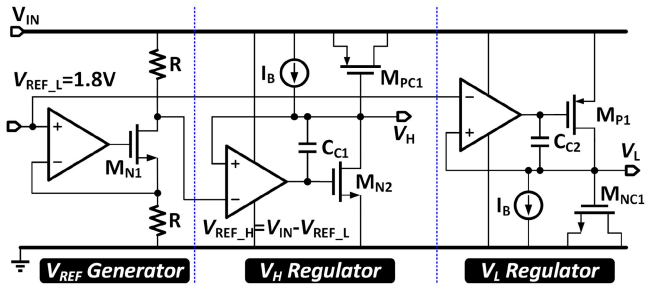


Fig. 10. Schematic of voltage regulators for internal voltage rails.

Fig. 10 shows the implementation of the voltage regulators used to generate the voltages for biasing. A PMOS voltage regulator is used to generate V_L (=1.8V). For V_H, the reference voltage $V_{\rm REF\_H}$ ($= V_{\rm IN} - V_{\rm REF\_L}$) is generated by the voltage-to-current block. The NMOS voltage regulator is used to generate $V_H (= V_{\rm IN} - V_{\rm REF\_L})$ that sinks the current. Dummy loads I_B and compensation capacitors (C_{C1} and C_{C2}) are used to ensure stability. For V_{H1}, the schematic is the same as V_H, but the reference voltage is $V_{\rm REF\_H1} (= V_{\rm OUT} - V_{\rm REF\_L})$.

C. Clock Distribution and Level Shifting

The clock phases are distributed to the whole silicon chip. To ensure that the VCO can generate the required maximum switching frequency, the wiring parasitic capacitance between adjacent inverters has to be accurately estimated as it increases the total delay of the ring oscillator. From the post-layout simulation, the

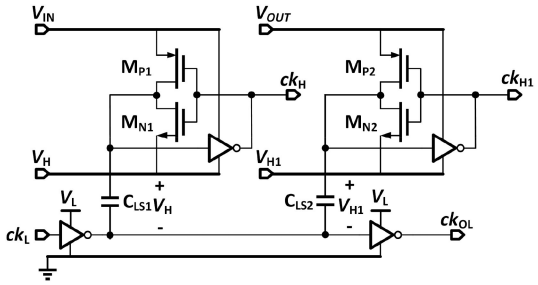


Fig. 11. Circuit implementation of clocked level-shifters.

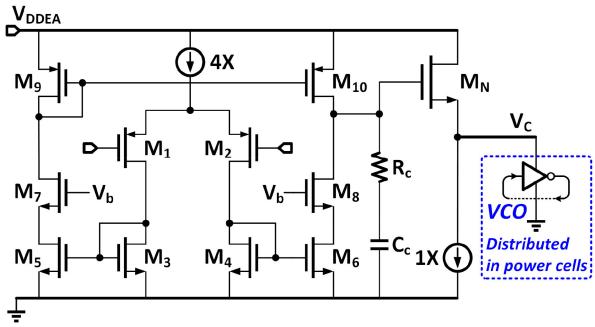


Fig. 12. Circuit implementation of EA.

value is around 0.1 fF/μm when the minimum width of 0.28 μm is used. Higher layer metals were used to reduce the parasitic. Accordingly, the inverters were properly sized to have sufficient driving ability. Simulation results were eventually verified by measurement results.

To reduce the power consumption, clocked level-shifters are used [14], and they are located close to the power cells to minimize timing variations. Fig. 11 shows an example of the clock shifting from the (0, V_L) domain to the ($V_{\rm H}$, $V_{\rm IN}$) and ($V_{\rm H1}$, $V_{\rm OUT}$) domains. The bottom plate of the coupling capacitor $C_{\rm LS}$ is driven by the input clock ck_L, thus coupling ck_L to the high-side voltage domain ck_H and ck_{H1}. M_{N1} and M_{P1} serve as pull-down and pull-up resistors, respectively, to control the dc capacitor voltage of $C_{\rm LS}$. As there is no dc current through these two voltage domains, clocked level-shifters can switch faster with lower power than the conventional current-starving level-shifters.

D. Regulation Controller

Fig. 12 shows the schematic of the EA. It consists of a one-stage current-mirror amplifier with dc gain enhanced by using cascode transistors M_7 and M_8. Driving capability is increased by using an NMOS source follower as the output stage to drive the VCO. As the output node V_C has low impedance, the corresponding pole is pushed higher than the unity-gain frequency. The dominant pole is placed at the gate of the source follower. A type-II compensator consisting of $R_C = 38$ kΩ and $C_C = 22$ pF is used to generate a pole-zero pair to cancel the output pole and extend the bandwidth of the system. To increase

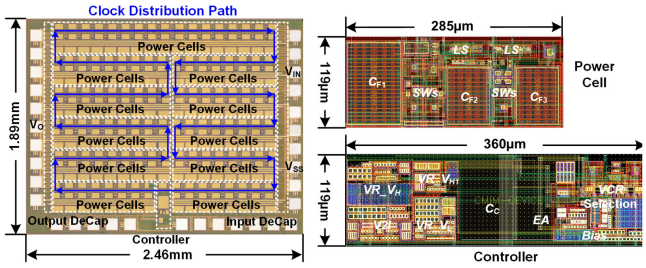


Fig. 13. Chip microphoto of first test chip solely with an SC converter.

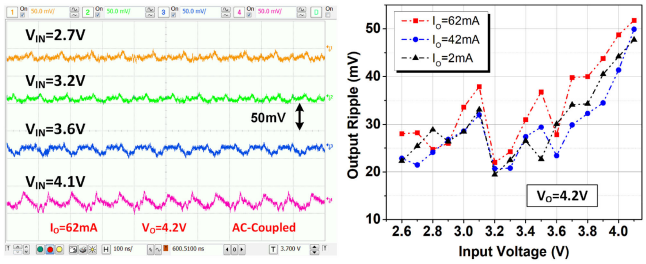


Fig. 14. Measured output voltage ripple under different loading and input voltages.

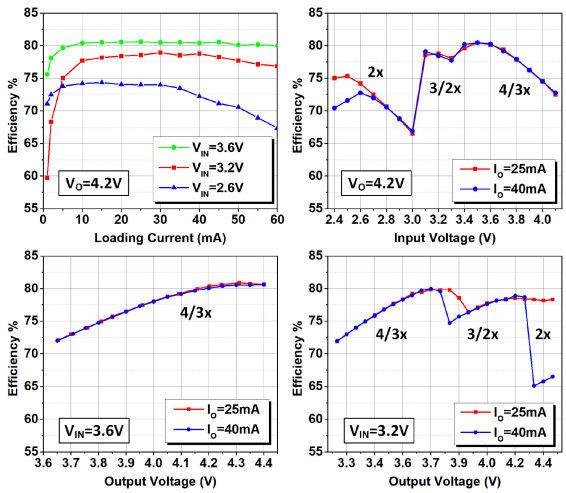


Fig. 15. Measured efficiency of the proposed SC converter versus loading currents, output voltages, and input voltages.

the voltage headroom of M_N and to eliminate the body effect, the body of M_N is isolated by deep N-well and connected to M_N's source terminal.

V. Measurement Results

Two test chips were designed in this work, and both were fabricated in 0.18-μm 1P6M CMOS processes. The first chip consists of only the SC converter for verifying functionality and performance. The micrograph is shown in Fig. 13, and the chip measures an area of 1.89 mm $\times$ 2.46 mm including all testing pads (the active area is 1.72 mm $\times$ 2.02 mm). The power cells

TABLE IV
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART SC CONVERTERS

Work	ISSCC`18 [21]	ISSCC`16 [22]	JSSC`15 [23]	JSSC`10 [15]	VLSIC'09 [14]	This work	
						1st Test Chip	2nd Test Chip
Technology	65 nm Bulk	0.35 μm HV Bulk	28 nm FDSOI	32 nm Bulk	130 nm Bulk	**0.18 μm Bulk**	**0.18 μm Bulk**
Topology	Step-Up & Down	Step-Up & Down	Step-Up SC	Step-Up SC	Step-Up SC	**Step-Up SC**	**Step-Up SC**
Cap. Type	MOS MIM	MIM	MOS, MOM	Poly MOM	MIM	**MOS, MIM**	**MOS, MIM**
Ideal VCRs	11 buck 13 boost	8 buck 9 boost	5/2, 2/1, 3/2	2/1	2/1	**2, 3/2, 4/3**	**3/2, 4/3, 1**
# of VCR	24	17	3	1	1	**3**	**3**
# of C_{fly}	20	4	4	1	1	**3**	**3**
# of Interleaving Phases	2	1	4	32	16	**101**	**87**
V_{IN}	0.22-2.4 V	2-13 V	1 V	1-1.2 V	1-1.2 V	**2.6-4.2 V**	**2.7-4.2 V**
V_{OUT}	0.85-1.2 V	5 V	1.2-2.4 V	1.3-2 V	1.8 V	**3.5-4.3 V**	**3.6 V**
$P_{OUT,\,MAX}$	34 mW	10 mW	2.7 mW	7.5 mW	4.8 mW	**258 mW**	**216 mW**
η_{peak}	83.2%	81.5%	88%	64%	82%	**82%**	**78% (SC Mode)**
Active Area	2.42 mm^2	6.8 mm^2	0.114 mm^2	0.0067 mm^2	2.25 mm^2	**3.47 mm^2**	**3.07 mm^2**
Power Density @ η_{peak}	10.2 mW/mm^2	1.47 mW/mm2	4.9 mW/mm^2	500 mW/mm^2	0.67 mW/mm^2	**54.5 mW/mm^2**	**52.8 mW/mm^2**
Internal C_{OUT}	0	600 pF[#]	300 pF	0	400 pF	**200 pF**	**248 pF**
Regulated	Yes	Yes	No	No	Yes	**Yes**	**Yes**
ΔV_O%	7.5%	N/A	N/A	N/A	0.5%	**1.23%**	**1.38%**

[#]extracted from paper.
FDSOI: Fully depleted silicon on insulator.

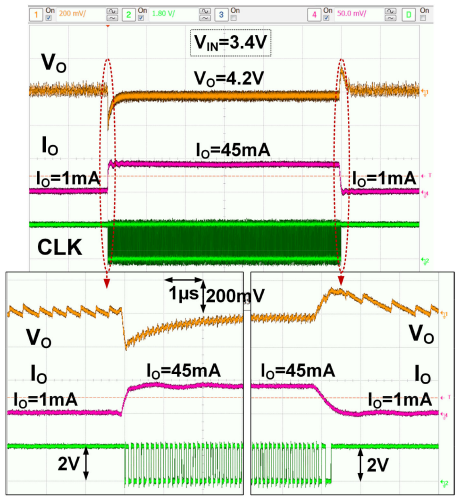


Fig. 16. Measured waveforms of transient response.

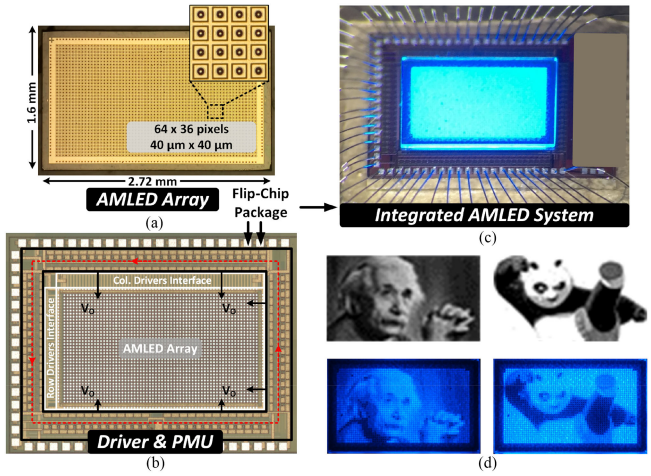


Fig. 17. Chip photos of (a) AMLED array, (b) drivers and the PMU, (c) integrated AMLED microdisplay system, and (d) examples of display images.

in this SC converter are serpentine-packed but connected head to tail as a ring.

Fig. 14 shows the measured output voltage ripples ΔV_O of the SC converter under different input voltages and loading conditions. With no external output decoupling capacitor, the maximum ΔV_O was 52 mV, which is only 1.23% of the output voltage. Fig. 15 shows the measured efficiencies at different load currents and input voltages. The peak efficiency was 81% when the loading current was 45 mA at the input voltage of 3.6 V. Note that the efficiency increased when $V_O/V_{\rm IN}$ was close to the ideal VCR. For the $2\times$ mode, thick-oxide MOS capacitor was used to handle higher voltage stress, resulting in higher output resistance and lower efficiency than other VCRs. This is not a big issue as most of the time the Li-ion battery voltage will be above 3.2 V, and the average efficiency is mostly decided by the $4/3\times$ mode and the $3/2\times$ mode.

Fig. 16 shows the measured transient responses with the loading current switching from 1 to 45 mA with rise and fall times of 100 ns. The overshoot and undershoot of the output voltage $\Delta V_{\rm OUT}$ were lower than 200 mV and the recovery time t_R was under 3 μs. Both over- and undershoot voltages were smaller than 5% of the output voltage $V_{\rm OUT}$ with zero external C_L. The transient responses were fast enough for the LED display system.

The second chip has the PMU integrated with the AMLED drivers, as shown in Fig. 17 [21]. The AMLED array was fabricated using a GaN process and measured 1.6 mm $\times$ 2.72 mm (see Fig. 17(a)), whereas the silicon drivers and the PMU

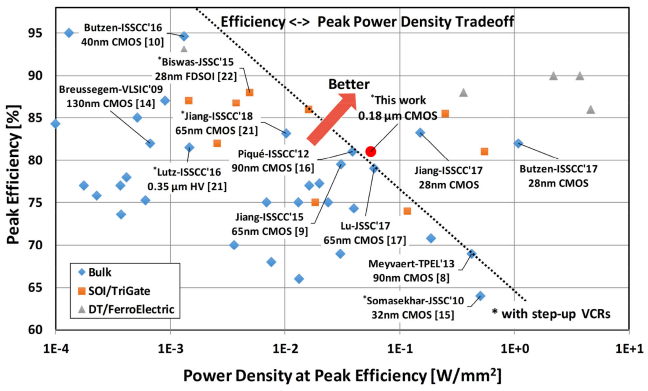


Fig. 18. Comparison of state-of-the-art fully integrated SC converters showing peak efficiency versus power density at peak efficiency [25].

together measure 2.8 mm $\times$ 3.7 mm, with the PMU forming the outer ring (see Fig. 17(b)). The AMLED array was flip-chip bonded to the silicon chip. The digital I/O pins controlling the display were wire-bonded directly to the PCB. Fig. 17(d) shows two examples of the display images. With a 4-b gray-scale control, images can be clearly rendered. For the second test chip, the regulated output voltage was 3.6 V, so a step-up SC converter with 3/2$\times$ and 4/3$\times$ modes cascaded a step-down linear regulator were utilized to cover Li-ion battery voltage range. When working in the SC converter mode, the converter achieved 78% peak efficiency in 3/2$\times$ mode ($V_{\rm IN} = 2.7$ V and $V_O = 3.6$ V). When working in the linear regulator mode, the converter achieved 91% peak efficiency at $V_{\rm IN} = 3.7$ V and $V_O = 3.6$ V. The maximum deliverable power of the converter was 216 mW.

The proposed SC converter is compared with state-of-the-art designs in Table IV. By using stacking transistors and performing design optimization, our SC converter achieved higher peak power density while maintaining similar peak efficiency when compared to [22] and [23]. The work of [16] has higher power density but much lower efficiency. The work of [24] used an advanced technology to achieve higher efficiency, but the power density is much lower. By using the distributive clock scheme, our converter has more interleaving phases and low output voltage ripple while delivering more current than that in [15]. From Fig. 18, when compared with state-of-the-art fully integrated SC converters, our work shows a better tradeoff between peak efficiency and peak power density with a lower cost than most of the works using bulk CMOS and SOI/TriGate processes.

VI. Conclusion

A fully integrated SC dc–dc converter is proposed in this article to power up an AMLED microdisplay. Multiphase interleaving scheme is adopted such that the output voltage ripple is significantly reduced, and no external output capacitor is needed. The power cells are cascaded to encircle the LED array. The stacking technique with three voltage conversion ratios is utilized to handle the wide input voltage range of an Li-ion battery (2.6 V–4.2 V) and reduce the switching loss. Good efficiency is achieved without using an advanced process or sacrificing output current density.

The first test chip of the SC converter had 101 interleaving-phases and the output voltage ripple ΔV_O was measured to be 1.23% of the output voltage. It achieved a maximum power density of 74.4 mW/mm^2, a peak efficiency of 81%, and delivered a maximum power of 258 mW. The second test chip integrated the SC converter with the AMLED drivers to power the microdisplay by using only an Li-ion battery with no external component.

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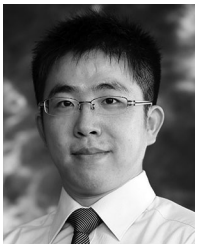

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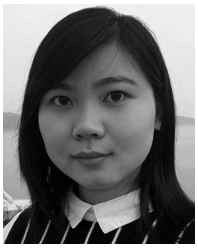
He was a Visiting Scholar with the State Key Laboratory of AMSV, University of Macau, Macau, China, in 2015, and a Post-Doctoral Fellow with HKUST, in 2017. In 2018, he joined Kilby Labs Silicon Valley, Texas Instruments, Santa Clara, CA, USA, as an Analog Design Engineer. His research interests include power management IC design, especially in switched-capacitor power converter design.

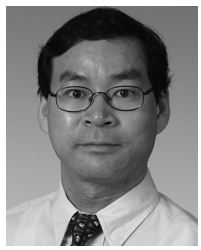
Dr. Jiang was a recipient of the Analog Devices, Inc., Outstanding Student Designer Award in 2015, the IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award 2016–2017, and the ASP-DAC University LSI Design Contest Special Feature Award in 2018.



Xun Liu (S'12–M'19) received the B.Eng. degree in electronic and information engineering from Zhejiang University, Hangzhou, China in 2011, and the Ph.D. degree in electronic and computer engineering from The Hong Kong University of Science and Technology (HKUST), Hong Kong, in 2017.

She was a Postdoctoral Fellow with HKUST, in 2017, after graduation, and an Engineering Intern with the Department of Power Management IC, Qualcomm Technologies, Inc., San Diego, CA, USA, in 2017. In 2018, she rejoined Qualcomm, Santa Clara, CA, USA, where she is currently a Senior Analog Designer. Her research interests include power management IC and analog IC design, especially in high-frequency dc–dc converters, three-level buck converters, and power amplifier supply modulators design.

Dr. Liu was a corecipient of the ASP-DAC University LSI Design Contest Special Feature Award in 2018.



Wing-Hung Ki (S'86–M'91) received the B.Sc. degree from the University of California, San Diego, CA, USA, in 1984, the M.Sc. degree from the California Institute of Technology, Pasadena, CA, USA, in 1985, and the Ph.D. degree from the University of California, Los Angeles, CA, USA, in 1995, all in electrical engineering.

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Prof. Ki was an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 2004 to 2005 and from 2012 to 2013, and an International Technical Program Committee Member of the IEEE International Solid-State Circuits Conference from 2010 to 2014. He has been an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS since 2016, and the IEEE JOURNAL OF SOLID-STATE CIRCUITS since 2018.

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Dr. Mok was the recipient of the Henry G. Acres Medal and the W. S. Wilson Medal from the University of Toronto, and the Teaching Excellence Appreciation Award three times from The Hong Kong University of Science and Technology. He was also a corecipient of the Best Student Paper Award, twice, in the 2002 and 2009 IEEE Custom Integrated Circuits Conference. He was a member of the International Technical Program Committees of the IEEE International Solid-State Circuits Conference from 2005 to 2010 and from 2015 to 2016. He was a Distinguished Lecturer of the IEEE Solid-State Circuits Society from 2009 to 2010. He was an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 2006 to 2011, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I from 2007 to 2009, and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 2005 to 2007 and from 2012 to 2015. He has been an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I since 2016.

Yan Lu (S'12–M'14–SM'17) received the Ph.D. degree in electronic and computer engineering from the Hong Kong University of Science and Technology, Hong Kong, in 2013.

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Dr. Lu is a TPC member of ISSCC and CICC, and was a Guest Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I in 2019 and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 2018 to 2019. He was a recipient/corecipient of the 2018 Macao Science and Technology Award (second prize, with the first prize vacancy), the IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award 2013–2014, the IEEE CAS Society Outstanding Young Author Award 2017, ISSCC 2017 Takuo Sugano Award for Outstanding Far-East Paper, and the PwrSoC Workshop 2018 Best Student Poster Award First Place (as an advisor).