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Global digital controller for multi-channel micro-stimulator with 5-wire interface featuring on-the-fly power-supply modulation and tissue impedance monitoring

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ABSTRACT

This paper reports a global digital controller for multi-channel high density micro-stimulator applications. By centralizing the essential functions including stimulation timing controls, tissue-electrode impedance (TEI) monitoring and power supply modulation in the global digital controller (GDC), digital blocks in the local electrode driver channels (LEDCs) can be greatly simplified, resulting in compact electrode drivers suitable for high density intracellular stimulations. Based on the proposed column-parallel row-scanning (CPRS) stimulator topology, the 5-wire global control ensures customized per channel stimulation with minimal interfacing overhead. A 4-column GDC stimulator prototype is fabricated in a 0.18 μm CMOS process. It features flexible stimulation with a power consumption of 18 μW/column while enabling global power-supply modulation and real-time TEI monitoring for improved stimulation efficiency and safety.

1. Introduction

Multichannel microstimulator is the main apparatus required for establishing a link between an artificial sensor and a high-density nerve array such as the retina and the cortex [1]. A stimulator triggers neurons by artificially modulating excitatory postsynaptic potential through sourcing and sinking charge packets into and from the axon hillock region of neurons. Recently, electrical stimulation of high-density electrode array emerges as an important engineering interest, engendered by technological advances appeared in nanofabrication of electrode array and deep-submicron high-density current driver circuits [2]. A micro-stimulator drives an external load impedance that can be approximated by a resistor (R_a) and a capacitor (C_{dl}), which are determined by the materials and geometries. The access resistance (R_a) arises from the hydrolyte at the tissue-electrode interface, while the double layer capacitance (C_{dl}) represents the charge-transfer contributed by ionic redox reaction in the Helmholtz layer adjacent to the metallic surface of the electrode [3]. The Faradaic resistance which lies in parallel with C_{dl} is large enough to keep the irreversible chemical reactions (which are physiologically harmful) inside the safety window.

With the ever-expanding applications of electrical stimulators, ranging from unraveling the blueprint of the neural network to the cure of various deceases originating from defects in the nervous system, various micro-stimulator systems have been proposed [4,5]. The recent development of high-density stimulation applications such as retinal prosthesis [6] and intracellular micro-electrode array (MEA) monitoring (~10,000 electrodes [2]) brings about increasing demands for multi-channel micro-stimulators (MCMS) systems. As the number of driving channels increases, the managing architecture of a MCMS has to be more delicately designed to efficiently supervise the timing, duration, polarity, and spatial patterns of electrical stimulations under power and area constraints. Various efforts have been made to achieve different aspects of GDC system optimization, including global-local stimulation data packet transmission protocol [7], programmable scanning pattern control [8], flexible waveform generation [9], compliance-voltage-aware power-supply control [10,11] and TEI monitoring [12].

Sivaprakasam et al. [7] sought for an efficient data transmission protocol by optimizing the packet error rate and the required bandwidth. However, their 60-channel stimulator is highly customized and the dedicated serial data bus and parallel 8-to-1 multiplexed-waveform-generator architecture can be a major bottleneck in high-density stimulator designs. In [9], a GDC which can generate programmable current waveforms with a time resolution of 4 μs was designed for a 1024-channel stimulator. Despite its capability of generating effective step-down stimulation waveforms [13] which can reduce the required

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compliance voltage by 10%−15%, every LEDC requires a dedicated digital controller with a power and area overhead of ~10 μA at 1 MHz and 21%, respectively, which inevitably burdens the LEDC design and limits the stimulation density.

In high-density stimulation, it is important to minimize the resistive heat loss across the current drivers to regulate the tissue temperature increment to be under 4.5 °C [14]. In order to prevent overheating as a result of the voltage drop across the current drivers, many existing MCMSes [10,11,15] employed DC-DC converters to adaptively regulate the power supply and dynamically track the compliance voltage of the electrodes. Nevertheless, the scalability issue of the previously reported GDC remains unsolved as a result of the requirement for dedicated regulation circuits per stimulation channel [10] and a split supply configuration [13] which ultimately limits the stimulation resolution. To improve this situation, the GDC in [11] employs a time-multiplexed charge packet delivery scheme with multiple electrode drivers sharing a buck-boost DC-DC converter. However, the number of concurrently driven channels is still limited by the number of the time slots that can be allocated within a stimulation time frame. Apart from that, the requirement of a large number of interfacing wires (16 in [6], 26 in [9], and 31 in [16]) as a result of the intensive usage of multiplexing switches and sophisticated bus protocol also significantly increases the LEDC complexity. To further ensure the safety of MCMS, the GDC should ensure the tissue-electrode interface quality while preventing residual charge accumulation. This can be indirectly inferred by measuring the tissue-electrode impedance [12] by incorporating an impedance monitoring circuit in the stimulator system [17].

This paper presents a GDC architecture that is suitable for MCMS with a high-density MEA. The GDC can control a large variety of MEAs with varying geometries and channels by using a very lightweight LEDC controller which is comprised of only a set of shift registers. Particularly, the control signals are synchronized by the GDC in a row-wise manner through the proposed column-parallel row-scanning (CPRS) stimulator topology, relieving the LEDC from dedicated clock counters for complex timing control. In addition, on-the-fly dynamic power supply modulation and in-situ TEI monitoring for improved stimulation efficiency and safety can also be achieved. Each LEDC can be custom controlled by using only a 5-wire interface. The fabricated 4-column GDC prototype in 0.18 μm CMOS successfully demonstrates stimulation data distribution, flexible stimulation timing control, switching-mode power supply (SMPS) control and TEI safety monitoring, while consuming only 18 μW per column.

The rest of the paper is organized as follows. Section 2 discusses about the architectural considerations that underlies the proposed GDC. Section 3 explains the operating principles of the GDC. Experimental results are presented in Section 4. Section 5 concludes the paper.

2. Architectural considerations of the proposed GDC

In this section, we investigate the architectural considerations for MCMS driving a variable-size MEA, including the communication protocol, stimulation timing control method, power supply configuration, and impedance monitoring circuit. The GDC should distribute the data packets containing the stimulation waveform profiles (e.g. current amplitude) for every LEDC. As the attached MEA size increases, the required data flit size also increases. The **Stimulation Data Packet Transmission (Stim Data Pkt Tx)** block distributes the stimulation profiles (current amplitude) to each LEDCs. Fig. 1(a-c) illustrates three different data bus protocols: 1) parallel; 2) cluster; and 3) serial. The serial bus architecture is shown in Fig. 1(c). As all the LEDCs retrieve their data packets funneled through the serial bus, the packet dropout rate can be increased [7]. A solution is to utilize the fully parallel data bus architecture as shown in Fig. 1(a). The constant flit size packets are distributed to LEDCs simultaneously, leading to a reduced packet dropout rate but at the expense of the requirement for a local LEDC decoder. To achieve both a small LEDC size and a good data error tolerance, the cluster bus protocol where each cluster is accessed separately can be utilized, as shown in Fig. 1(b). In the CPRS topology, the LEDCs contained in a row are assigned with an identical address, thus the required bandwidth for address data transmission can be reduced by $1/N_{col}$, where N_{col} is the number of LEDCs in a row. Yet, the data error rate can be kept much lower than that of the serial data protocol as each cluster data packet can be independently distributed. In this work, we exploit the row-wise clustering MEA architecture and propose the CPRS topology (which is based on the cluster bus protocol) to achieve an efficient GDC implementation for high density MCMS.

To control the stimulation pattern on a high-density electrode array, multiple instances of timers should be operated coherently. The timing control protocol employed by the **Channel Controller** determines where the timers are located (e.g. centralized or distributed), and how the timers are shared and synchronized among LEDCs. Fig. 1(d–f) depicts the timer instances in three different timing control protocols: 1) local autonomous; 2) parallel; and 3) cluster. The GDC controls both the polarity and timing control of stimulation waveform of multiple LEDCs, which can be accomplished using the local distributed autonomous control method (Fig. 1(d)), the centralized parallel method (Fig. 1(e)), and the centralized cluster method (Fig. 1(f)). The stimulation timing sequence of the LEDCs in the MCMS, which is applicable to all the control methods to determine the scanning pattern. With the local distributed autonomous timer control [6,11], each LEDC contains a set of timing controllers and related building blocks to generate the local polarity and charge cancellation signals. Even though highly customized LEDC functions can be realized, the requirement for the control overhead in individual stimulation channels can limit the LEDC size. By centralizing the stimulation waveform generation in the GDC as shown in Fig. 1(e), the LEDC area overhead and the data packet size can be much reduced. This scheme is demonstrated in [9], where the GDC generates the initiation and termination signals for each LEDCs. Nevertheless, the multiple instances of concurrently running timing control circuits can increase the LEDC synchronization complexity and possibly lead to deadlock or livelock states. Also, independent sets of routing wires are required for every LEDC, increasing the probability of crosstalk and hence the packet dropout rate. In this work, the centralized cluster method which takes advantage of the row-wise clustering in the propose CPRS topology is utilized, as shown in Fig. 1(f). The waveform control timer in the GDC is shared among different stimulation rows through time multiplexing, which can balance the tradeoffs between the implementation complexity, LEDC size and stimulation frequency. Also, it can significantly reduce the number of global control wires while minimizing signal interference.

In MCMS, the power management circuit should improve the stimulation efficiency and reduce the heat energy loss so as to increase the number of simultaneously driven electrodes without violating the power and safety constraints (e.g. [10,11,15]). According to how energy is delivered between the power source and electrodes, there are three classes of power supply modulation methodologies for reducing the power loss across the current controlling transistors, namely: 1) fixed voltage (FV); 2) dynamic voltage scaling (DVS); and 3) direct voltage forming (DVF). In the FV supply based stimulator topology, current drivers pull energy from the fixed voltage regulator. The conduction loss across the current drivers can induce excessive heat, especially when the supply voltage is much higher than the electrode voltage. To reduce the power loss of the FV supply based stimulators, DVS supply based stimulators adaptively vary the supply voltage levels according to the compliance voltage required for successful biphasic stimulations (e.g. current amplitude, pulse duration, and electrode types). For DVF supply based stimulators [10,11], the power loss across the current controlling transistors can be completely remove by applying voltage waveforms directly derived from the instantaneous electrode voltage for driving a specific electrode. Yet, existing DVF supply based stimulators cannot be applied in high density MCMS designs due to the excessive overhead induced by dedicated

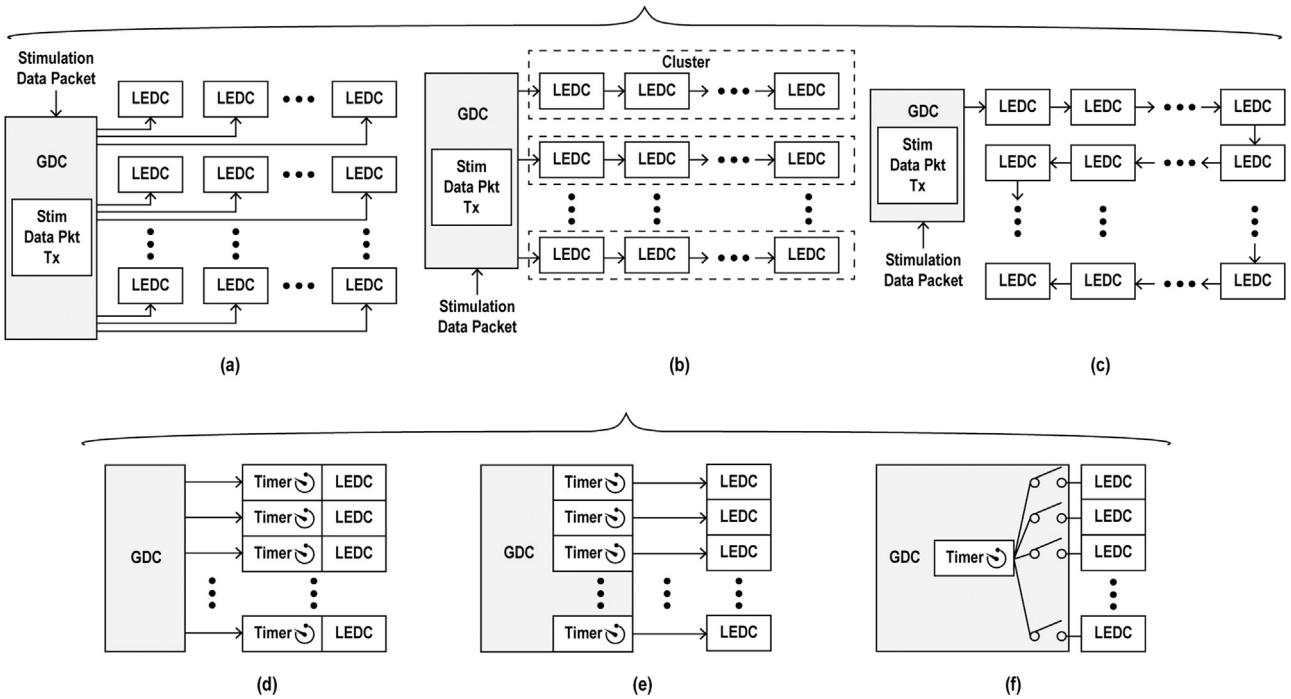

Fig. 1. (Top) Communication protocols for MCMS designs: (a) Parallel bus; (b) Cluster bus; and (c) Serial bus. (Bottom) Timing control protocols for stimulation pattern generation: (d) Local autonomous; (e) Parallel; and (f) Cluster.

power converters required in each stimulation channel. In this regard, DVS supply based stimulators becomes the most viable option in high density stimulation applications.

A DVS supply based stimulator can employ either an array of switched-capacitor or an inductor as energy storage devices for output voltage modulation. Fig. 2(a) shows a switched-capacitor based DC-DC converter employed to generate 4 discrete output voltage levels to adaptively accommodate for the maximum electrode voltage [15]. The split-supply electrode drivers then route current pulses from the working electrodes to the counter electrodes using the minimum voltage levels required. During a particular biphasic stimulation period, an electrode (V_{elec1}) works as a counter electrode during a cathodic stimulation phase, then it works as a working electrode in an anodic simulation phase. Yet, it can still suffer from low efficiency when it has to deal with varying number of electrodes, especially when driving small currents.

For improving the supply voltage resolution, we employed the on-demand charge transfer based power management scheme as shown in Fig. 2(b) [18]. The continuous supply voltage level is achieved by adaptively adjusting the duty cycle so that the inductor can deliver the amount of energy necessary for a supply voltage under a specific loading condition. As a consequence, instead of directly driving each electrode with dedicated DC-DC converters as in [10,11], we can drive multiple electrodes with a single supply using a forward buck/reverse boost converter to achieve a dynamic supply to simultaneously reduce the heat loss and recover the stored electrode charge to improve the

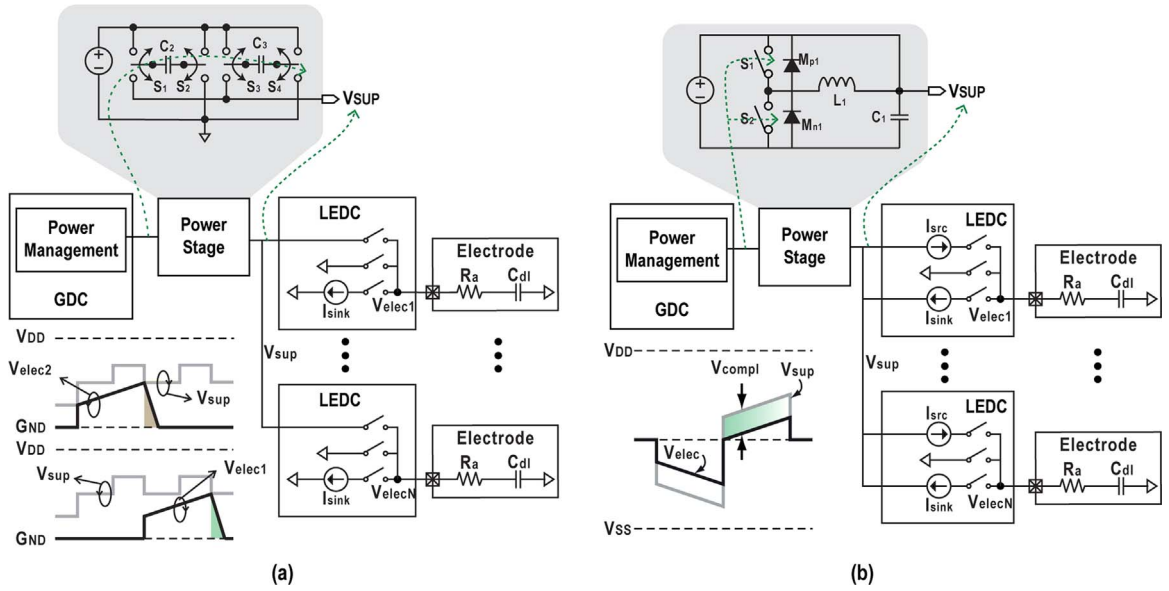

Fig. 2. On-the-fly power supply modulation methods for adapting to electrode compliance voltage: (a) Multi-level DC-DC converter based split power supply modulation [15]; (b) Power supply modulation based on on-demand charge delivery scheme [18].

stimulation efficiency. The GDC power management block modulates the inductor based power stage to achieve an adaptive voltage level following the electrode voltage (V_{elec}) with an offset determined by the voltage compliance (V_{offset}). To support expandable MEA implementation, the CPRS stimulator topology is also proposed to connect a group of simultaneously driven electrodes to share a single power management unit. Apart from that, the electrode voltage samples generated during the power supply modulation can be coherently incorporated to achieve the proposed TEI deduction methodology with minimal overhead.

By continuously monitoring the electrode voltage, the impedance of a particular electrode can be indirectly estimated. In particular, the access resistance (R_a) and the double layer capacitance (C_{dl}) can be calculated through the electrode voltage and the instantaneous stimulation parameters, and are defined as:

$$R_a = \frac{V_{stim}}{I_{stim}}, \quad C_{dl} = \frac{I_{stim} \bullet \Delta T}{\Delta V_{elec}} \tag{1}$$

A widely adopted impedance sensing method [20] based on monitoring the feedback voltage against the alternating current (AC) excitation is shown in Fig. 3(a), which requires an additional ac excitation source and a feedback voltage sensor that inevitably complicates the system implementation. Instead, our proposed TEI deduction method as shown in Fig. 3(b) provides a simpler mean to calculate the impedance by fully exploiting the dynamic state variables (e.g. electrode voltage) which are already available for the existing system power management function.

3. Proposed GDC architecture

As shown in Fig. 4, the proposed GDC controls the pulse timing and amplitude, and the leading phase polarity of each LEDC for flexible stimulation with a 5-wire global-local interface. The GDC is connected to the LEDCs array where each row forms a cluster and the electrode driver output of each column shares a dedicated readout circuit composed of an analog-to-digital converter and a charge-transfer voltage-scaling interface (ADC/CTVSIF). The GDC and the LEDC array perform three major functions as discussed in Section 2: 1) cluster bus communication protocol for disseminating the stimulation profiles to LEDCs; 2) global timer based stimulation pattern generation; and 3) on-demand charge transfer based DVS power management and real time TEI monitoring. In the practical implementation as shown in Fig. 4, the GDC consists of 4 sub-controllers: **Channel Controller, ADC Controller, FIFO Controller**, and **SMPS Controller**. The **Channel Controller** generates the anodic and cathodic stimulation commands using the time-division clustered timer protocol. It also delivers serial communication signals containing stimulation current data packets to each LEDC. The **ADC Controller** collaborate with the **FIFO Controller** to trace and store the electrode and supply voltage data, which are further fed to the power management block for DVS control. The FIFOs gives the SMPS Controller the freedom of tuning the duty cycle update algorithm which require varying depths of data records. The **SMPS Controller** determines the duty ratio of the PWM signals of the power stage according to the dynamic voltage profile at the electrode.

The LEDC consists of a shift register that stores the stimulation current amplitude and dual-polarity current drivers controlled by the current-steering DACs. In the proposed CPRS topology, the LEDC array is accessed row by row in each appointed time slot. The **Channel Controller** maneuvers the LEDC stimulations with *ACT_AN*, *ACT_CAT* and *CHG_CC* in the current row, while delivering the 5-bit stimulation current amplitude packets using data and clock serially to the LEDCs in the next row. The *ACT_AN* and *ACT_CAT* signals indicate the timing of the anodic and cathodic stimulation phases, respectively. After a biphasic pulse is emitted, the charge cancellation signal (*CHG_CC*) is sent to the LEDCs to remove the residue electrode charge and avoid electrolysis. The CPRS scheme allows column readout sharing for the LEDC array, significantly reducing the hardware overhead imposed for monitoring the electrode and supply voltage for each LEDC.

Fig. 5(a) shows the schematic of the **Channel Controller** incorporating two finite state machines (FSM), two counters, a shift register, and a stack for storing the data packets containing the stimulation current amplitude to be distributed to LEDCs in a specific row. The role of the **Channel Controller** is two-fold. The first role is to program the LEDCs in a row with the stimulation current profiles that would be used in the subsequent time frame. To achieve this, it signals the **Prog Channels FSM** (Fig. 5(d)) to manipulate the Address Counter, Bit Counter, and Stim Profile Stack, so that the data packets containing stimulation current amplitudes can be serially transmitted to the LEDCs via *data* and *clock*. The second role of the **Channel Controller** is to control the timing and polarity of a biphasic stimulation phases followed by charge cancellation. This is accomplished by the **Main FSM** through controlling *ACT_CAT*, *ACT_AN*, and *CHG_CC*, as shown in Fig. 5(c). When the **Main FSM** is processing a particular stimulation frame, it moves into the "Load Frame" state, where a new stimulation data frame is fetched into the data distribution register in the GDC. Subsequently, in the "Load Row DataPkt" state, a set of 5-bit current DAC amplitude data for all the channels in the selected row is concurrently loaded into the shift register in the **Prog Channels FSM**. Then, the **Main FSM** issues the StaStim signal to instruct the **Prog Channels FSM** to distribute the 5-bit N_{col} packets into every LEDC in that row.

Fig. 5(b) shows the timing diagram of the operation sequence of the 5-wire interface during a complete biphasic stimulation cycle for the entire LEDC array. A CPRS stimulation cycle starts with the *StimRdy* signal of the **Main FSM**, indicating that the first row data packets have been preloaded in the first row. The completion of a particular CPRS stimulation cycle is acknowledged when the **Main FSM** asserts the *StimDone* signal after finishing the stimulation of the last row of the LEDC array, as shown in Fig. 5(c). A biphasic stimulation cycle for a particular row in the LEDC array in one stimulation time frame (STF) is initiated through the *StaStim* signal in the "Load Row Data Pkt" state of the **Main FSM**, while triggering the **Prog Channels FSM** to start the serial data communication with the LEDCs in the next row. The **Main FSM** generates both the cathodic and anodic stimulation commands for the current row, followed by the charge cancellation command. At the same time, the LEDCs in the next row retrieve the current amplitude

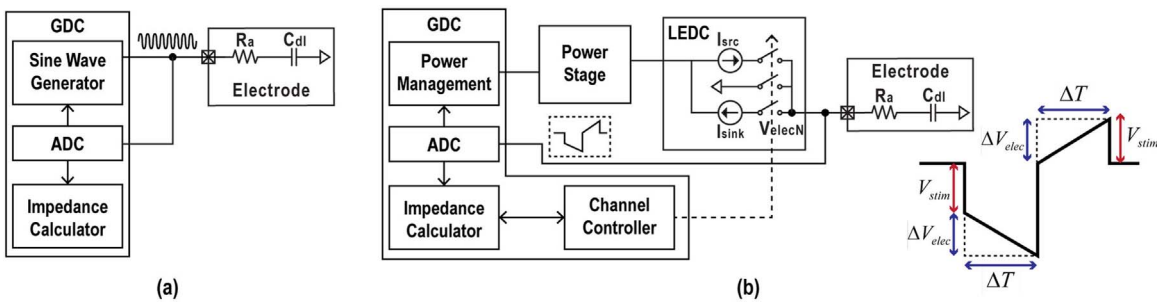

Fig. 3. Tissue-electrode impedance (TEI) monitoring methods: (a) Traditional method [20]; (b) Proposed stimulation waveform based impedance deduction method.

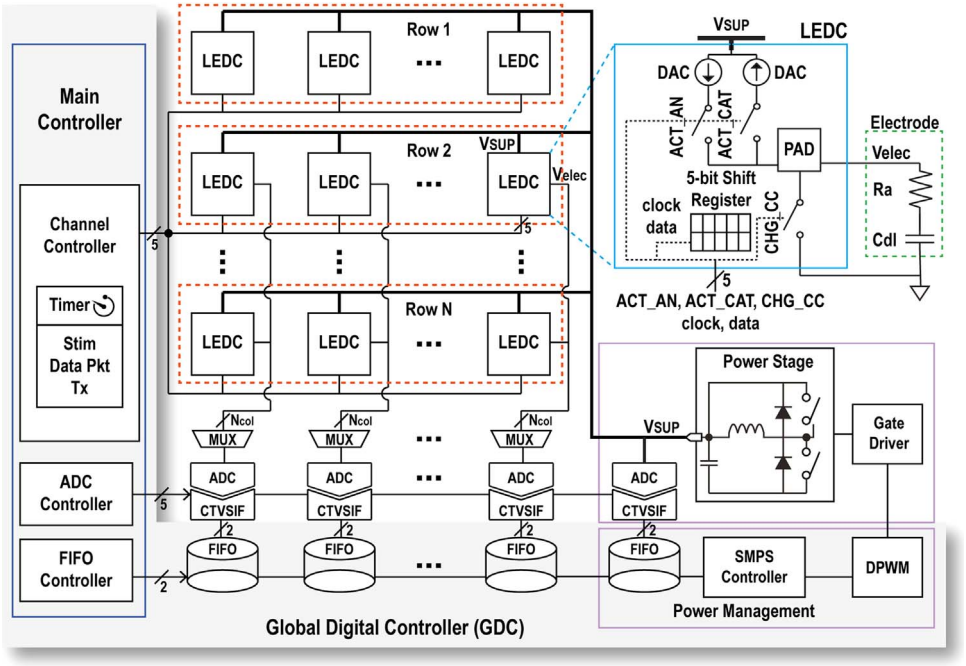

Fig. 4. The system architecture with the proposed global digital controller.

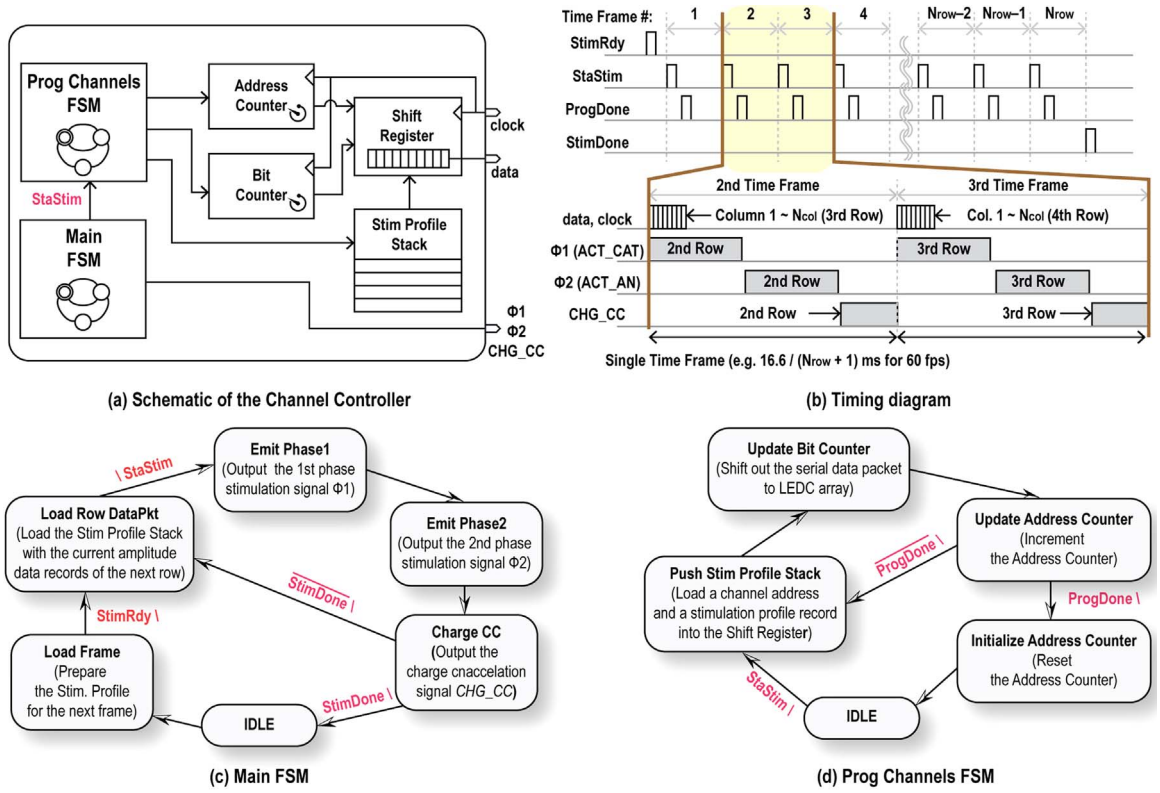

Fig. 5. Operation of the **Channel Controller.** (a) Schematic diagram. (b) Timing diagram during a full cycle of the CPRS stimulation of the LEDC array (with the first row data preloaded). (c) **Main FSM** serves for generating pulse commands. (d) The **Prog Channels FSM** distributes the data packets to LEDCs.

information that sets the current DAC individually. In general, the **Main FSM** generates the stimulation timing signals for the row (N-1) during the N-th STF. Then, it begins to traverse the sequential states "Emit Phase1" (Φ_1) and "Emit Phase2" (Φ_2), generating the cathodic (*ACT_CAT*) or anodic (*ACT_AN*) stimulation pulses for the specified time duration. Then in the "Charge CC" state, the 5-bit DAC current amplitudes of the selected row is reset to zero, and the electrode shorting signal is raised for charge cancellation. After the ($N_{row}+1$)-th STF, the **Main FSM** moves back into the "Load Frame" state and prepare for stimulation in the next row.

The proposed GDC can also efficiently handle the power supply modulation and TEI monitoring functions via the column-parallel readout circuits. The **ADC Controller** and the **FIFO Controller** in Fig. 3 operate the CTVSIF [19] and the SAR ADC to capture the electrode (V_{elec}) and supply (V_{SUP}) voltages. The 8-b ADC results are fed into the FIFO for SMPS duty ratio computation as well as TEI

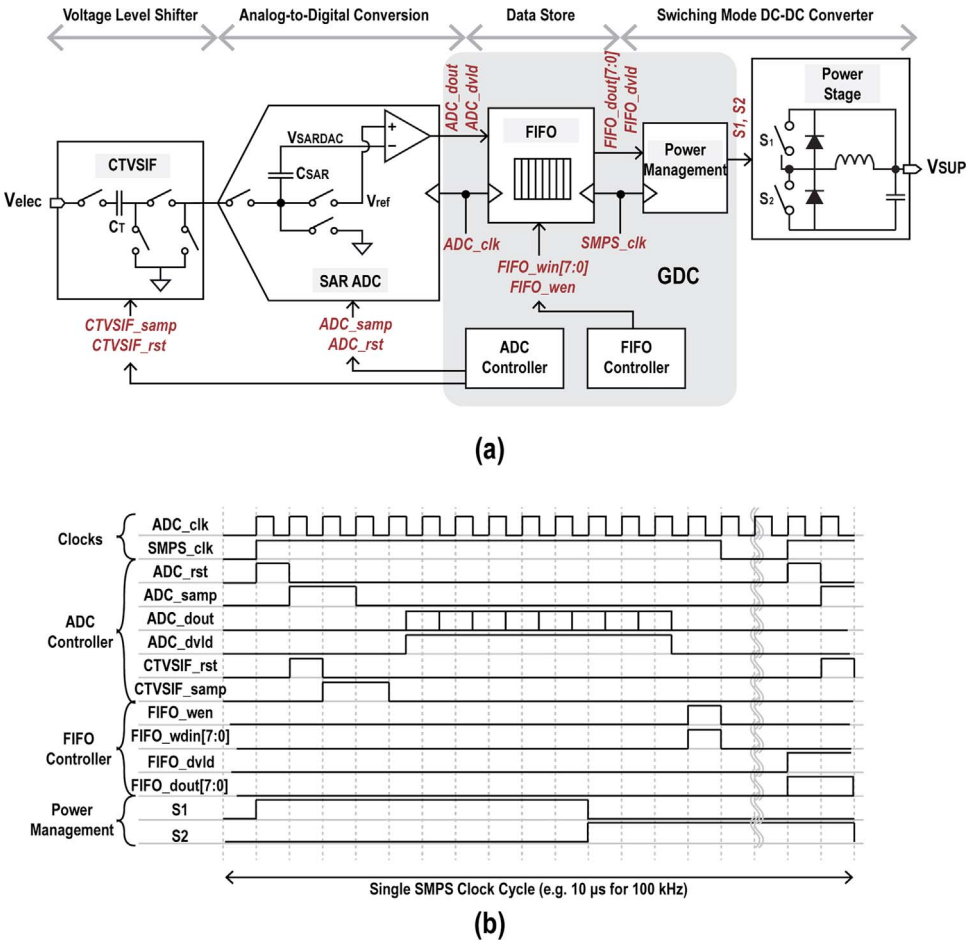

Fig. 6. Operating procedure for generating the adaptive power supply. (a) Schematic diagram showing the power management function that involves the sampling of the electrode voltage and PWM signal generation. (b) Timing diagram for the control signals related to the power management function.

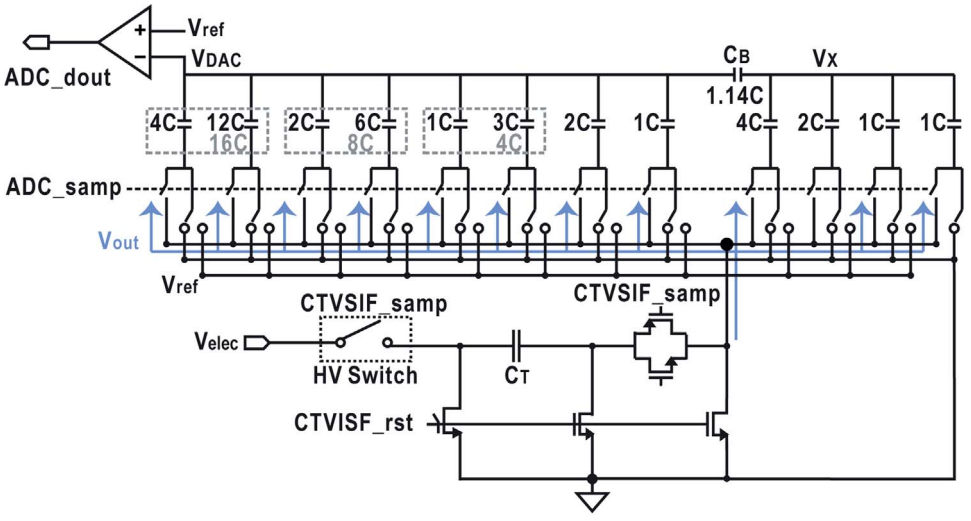

Fig. 7. Schematic of the CTVSIF with ADC [19].

calculation. For ADC input conditioning, the CTVSIF as shown in Fig. 7 is employed to translate the signal from the high-voltage domain for stimulation to the low voltage domain for the ADC. This is achieved by transferring the charge at the high-voltage input node to the bottom plates of the SAR ADC, leading to a relaxed power and area overhead when compared with the conventional resistive voltage divider approach.

Fig. 6(a) shows the CTVSIF-ADC-FIFO power supply modulation pathway. The GDC manages the process of sampling the electrode voltage, shifting the sampled voltage to the low voltage domain through the CTVSIF block, and digitizing the resultant signal and storing the digital data by the ADC-FIFO blocks. The power management block then generates PWM pulses for driving the power stage with the stored data. Fig. 6(b) shows the timing diagram of the power supply modulation process. The signals in the timing diagram are also annotated in Fig. 6(a) with the originating sub-controllers indicated. The *SMPS_clk*

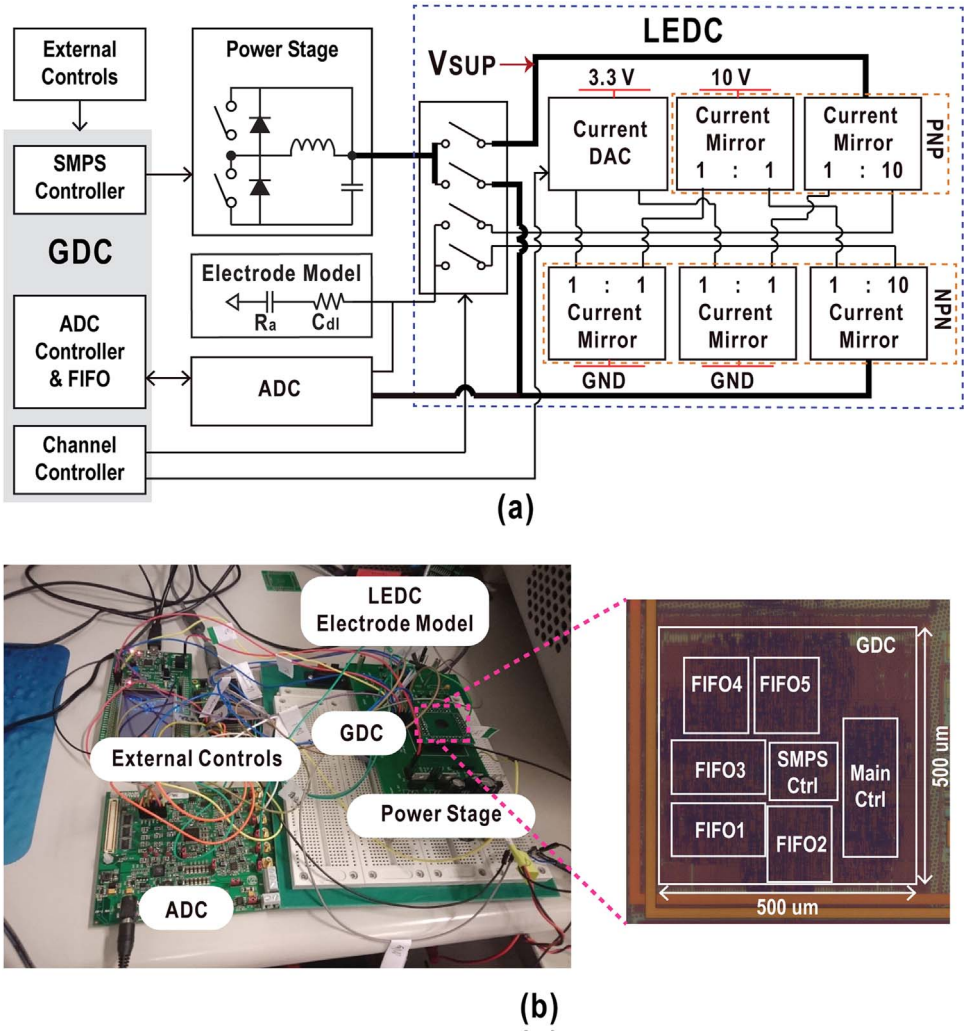

Fig. 8. (a) Schematic of the test setup for evaluating the proposed GDC. (b) The measurement setup consists of a microcontroller board for external controls, an ADC board, and a GDC board containing the fabricated GDC chip prototype, the LEDC electrode model and the power stage circuits. (For interpretation of the references to color in this figure, the reader is referred to the web version of this article.)

and *ADC_clk* are set to 100 kHz and 2 MHz, respectively. The GDC takes voltage samples and updates the duty cycle every 10 μs, which translates into 100 updates for a 1 ms stimulation pulse duration for effective power supply modulation and TEI monitoring. The ADC output is serially stored into *FIFO_wdin[7:0]* by the **FIFO Controller** when *ADC_dvld* is asserted, and the data is pushed into the FIFO using *FIFO_wen*. When *FIFO_dvld* is asserted at the rising edge of the consecutive *SMPS_clk*, the FIFO data records (*FIFO_dout[7:0]*) are extracted and fed to the **Power Management** block for calculating the duty ratio for digital pulse width modulation (DPWM) to adaptively generate V_{SUP} through the gate driving signals S_1 and S_2. The TEI can also be simultaneously monitored by using the V_{elec} data in Equation (1).

4. Experimental results

A GDC prototype is implemented in a 0.18 μm CMOS process with $N_{col} = 4$, occupying a total active area of 0.13 mm^2, as shown in Fig. 8(b). The FIFO depth is set to 16 for flexible duty cycle update to test various algorithms for the **SMPS Controller** requiring varying number of data records. With the digital PWM controller proposed in [18], the FIFO depth can be reduced to 4-words so as to achieve a 67% area reduction with no observable system performance degradation (as verified in measurement). The test setup as shown in Fig. 8(a) is employed for characterizing the GDC prototype. An LEDC circuit consisting a current DAC and current mirror as an electrode driver (Maxim DS4412 & BCV61) and switch arrays (TI CD4066B) is connected to RC-modeled electrodes. The GDC generates the control signals to manipulate the LEDC to source and sink current into and out of the electrode.

Fig. 9(a) and (b) show the voltage waveforms of V_{elec} and V_{SUP} when driving 100 μA and 300 μA electrode current during a biphasic stimulation cycle, respectively. V_{SUP} can be successfully modulated to follow V_{elec} while monitoring the TEI (which can be calculated using V_{elec} with Eq. (1)). When the stimulation amplitude is at 100 μA, we can observe the periodic triangular shapes in the V_{SUP} waveform. This is due to the lowering of the switching frequency of the SMPS Controller to reduce the switching loss for improving the conversion efficiency at low loading condition. When driving a larger current of 300 μA, the voltage displacement of V_{elec} during either the cathodic or anodic stimulation phase exhibits 3 times increase when compared to that for driving 100 μA (so as the voltage jump magnitude (V_{stim}) at the interphasic boundaries as indicated in dashed blue boxes). To calculate the TEI, the GDC uses four data points during a biphasic stimulation cycle: two data points for V_{stim} for computing the access resistance (R_a), and the other two data points for ΔV_{elec} for computing the double layer capacitance (C_{dl}). Based on the experimental results, it can be concluded that the GDC can successfully conduct flexible stimulations together with real-time TEI monitoring. The corresponding GDC control

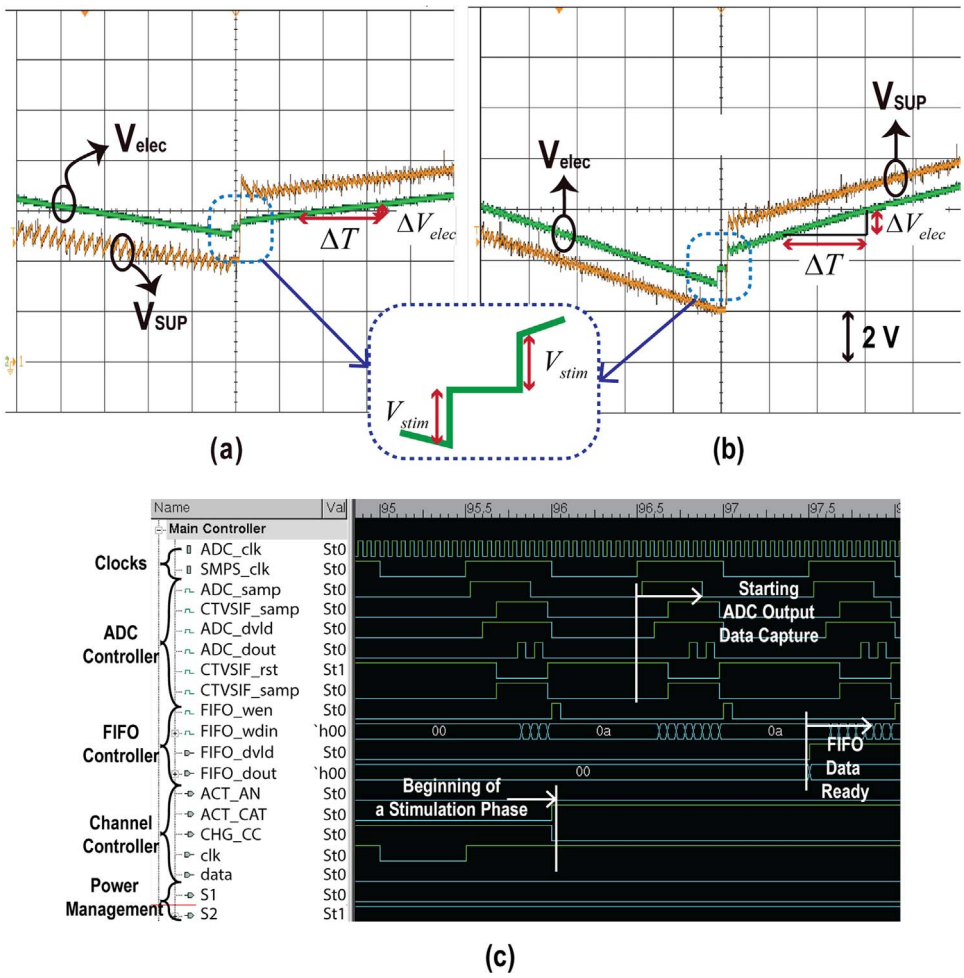

Fig. 9. The voltage waveform of the power supply modulated stimulator during a cathodic-first stimulus, when driving (a) 100 μA and (b) 300 μA current into an electrode model consisting of $R_a = 1$ kΩ and $C_{dl} = 110$ μF. (c) Post-layout transient simulation result of the proposed 4-channel GDC.

signals during the experiments are shown in Fig. 9(c). After the data packets containing the DAC amplitudes are distributed to the LEDCs, the GDC starts to capture the ADC output bit-streams with a half SMPS clock cycle delay. Once the first digitized electrode voltage is loaded into the FIFO, the **SMPS Controller** starts to calculate the PWM duty cycle for supplying or recycling the necessary charge in the consecutive SMPS clock cycle. Operating at 100 kHz, the **Main Controller** and the **SMPS controller** consumes 4.7 μW and 1.1 μW respectively. The rest of the power is mainly consumed by the FIFO operations.

5. Conclusion

A GDC for MCMS system is presented. The proposed GDC governs the timing, polarity and amplitude of the stimulation at every LEDC with only 5 interface wires. The LEDC stimulation control can be reduced to a pair of 5-b shift registers by centralizing the functions such as stimulation timing, amplitude, polarity control, power supply modulation, and TEI monitoring in the GDC. The CPRS stimulation strategy is also adopted to ensure flexible stimulation while enabling each row to share resources (e.g. CTVSIFs, ADCs etc.) for dynamic duty ratio update of the SMPS and for real-time TEI monitoring.

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