# A Fully Integrated Digital LDO With Coarse–Fine-Tuning and Burst-Mode Operation

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***Abstract*—The digital low dropout regulator (D-LDO) has drawn significant attention recently for its low-voltage operation and process scalability. However, the tradeoff between current efficiency and transient response speed has limited its applications. In this brief, a coarse–fine-tuning technique with burst-mode operation is proposed to the D-LDO. Once the voltage undershoot/overshoot is detected, the coarse tuning quickly finds out the coarse control word in which the load current should be located, with large power MOS strength and high sampling frequency for a fixed time. Then, the fine-tuning, with reduced power MOS strength and sampling frequency, regulates the D-LDO to the desired output voltage and takes over the steady-state operation for high accuracy and current efficiency. The proposed D-LDO is verified in a 65-nm CMOS process with a 0.01-mm$^2$ active area. The measured voltage undershoot and overshoot are 55 and 47 mV, respectively, with load steps of 2 to 100 mA with a 20-ns edge time. The quiescent current is 82 $\mu$A, with a 0.43-ps figure of merit achieved. Moreover, the reference tracking speed is 1.5 V/$\mu$s.**

***Index Terms*—Burst mode, coarse–fine-tuning (CFT), digital control, dynamic voltage scaling (DVS), energy-efficient digital, fast transient, low dropout regulator (LDO).**

## I. Introduction

TO achieve a high-accuracy and high-efficiency power management solution for a system on chip (SoC), as shown in Fig. 1(a), low dropout regulators (LDOs) are widely used as the postregulators following the dc–dc converters. Analog LDO (A-LDO) can achieve fast transient response and good ripple immunity at high input voltages, 1.2 V for example [1]. However, for energy-efficient systems, the input voltage of an LDO might go down to 0.6 V, at which the error amplifier in the conventional A-LDO may be difficult to design [2]. The digital LDO (D-LDO), on the other hand, draws significant attention for its low-input voltage and process scalability.

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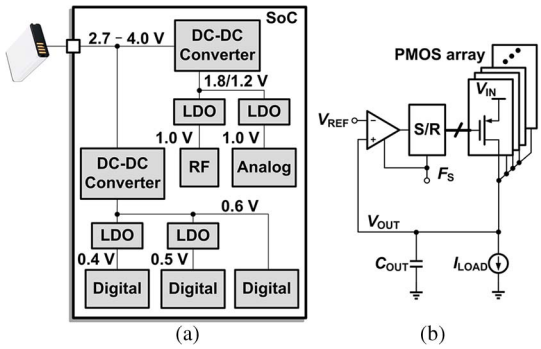


Fig. 1. (a) Energy-efficient low-voltage power management solution for SoC and (b) simplified block diagram of the conventional D-LDO.

The D-LDO was first brought out in [2]. As shown in Fig. 1(b), it consists of a comparator, a serial-in parallel-out bidirectional shift register (S/R), and a P-channel MOSFET (PMOS) array acting as the power transistors. The comparator is used to sense the difference between the output voltage $V_{\rm OUT}$ and the reference voltage $V_{\rm REF}$, whereas the S/R plays a role of an integrator to minimize the loop steady-state error. Nonetheless, since only one PMOS is turned on/off per clock cycle for the S/R operation, the transient speed of this D-LDO is mainly determined by its sampling frequency $F_S$. Increasing $F_S$ leads to faster transient response but larger steady-state power consumption. As such, improving the transient speed and current efficiency simultaneously is highly favored.

Several previous works have been proposed to tackle this issue [3]–[7]. A linear resistance scaling PMOS array with reduced levels was used in [3], but the 1-GHz sampling clock for fast transient sacrifices the quiescent current. A scheme of $\times 4$ counting at each sampling clock was employed when an undershoot/overshoot was detected in both [4] and [5], while a fast sampling clock is still necessary for maintaining fast transient response. A binary weighted PMOS array and a gated voltage controlled oscillator were employed in [6] and improved the transient speed to a certain extent. A unit gain frequency extension technique was applied in [7] with a digital filter and an 8-bit analog-to-digital converter, which increased the power consumption. Asynchronous circuits (see [8] and [9]) were introduced to advance the tradeoff of the synchronous D-LDOs. However, the inherent sensitivity to PVT variations limits its applications [5]. An improved transient response was achieved in [10] with reduced dynamic stability but only demonstrated at the relatively low current cases.

In this brief, a wide load range D-LDO with coarse–fine-tuning (CFT) and burst-mode techniques has been proposed for fast transient response and low quiescent current. This brief is organized as follows. The principles of the proposed techniques are discussed in Section II. Then, the circuit implementations and

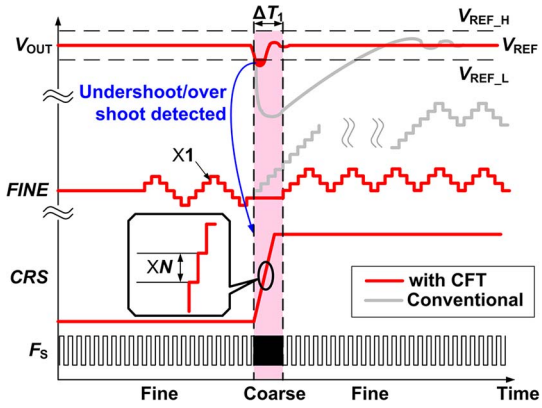


Fig. 2. Transient response of the D-LDO with the proposed schemes.

design considerations are presented in Section III. Section IV gives the measurement results, and a conclusion is drawn in Section V.

## II. Principles of the CFT and Burst-Mode Operation

In this brief, the PMOS array is divided into the coarse and fine sections, where the unit PMOS in the coarse section provides N times current of that in the fine one. These two sections are controlled by independent S/Rs, with the control words CRS and FINE that indicate the respective numbers of PMOS to be turned off. The combined control word COMB, corresponding to the overall output current, is thus defined as

$$\text{COMB} = N \times \text{CRS} + \text{FINE}. \tag{1}$$

The operation principle of the proposed D-LDO is depicted as in Fig. 2. In steady state, the D-LDO works at the fine-tuning mode, with a small PMOS strength and low $F_S$. When the variation on $V_{\text{OUT}}$ exceeds overshoot or undershoot detection boundaries ($V_{\text{REF\_H}}$ or $V_{\text{REF\_L}}$) under certain disturbances, the coarse tuning will be triggered whereby the coarse section takes over the D-LDO with FINE held constant. In this scenario, COMB shifts by $N$ unit in each clock cycle, comparing to the 1-unit shifting in fine-tuning (as the gray curves in Fig. 2). This boosts the open-loop gain of the D-LDO, allowing it to be quickly regulated to a status that is close to the desired value. For further improvement, a higher $F_S$ is employed in the coarse tuning as well. These operations prevent a large overshoot or undershoot on $V_{\text{OUT}}$ and thus significantly improve transient response.

To simplify the control and remove the external freeze signal required in [8], the coarse tuning will only last for a fixed $\Delta T_1$ duration, which is regarded as a burst-mode operation. After $\Delta T_1$, the coarse tuning is disabled while the fine-tuning is reactivated. Then, only FINE is shifting at a lower $F_S$. With a reduced speed but higher accuracy, this allows the D-LDO to be regulated to $V_{\text{REF}}$ with a desired load current.

For the quiescent current, it is evident that the D-LDO will consume larger power in the coarse tuning because of the higher $F_S$. However, the coarse tuning is activated for a short time with the burst mode, which only occupies a very small fraction of the D-LDO working time in most scenarios. Thus, the power overhead of the proposed D-LDO is negligible.

Therefore, with the proposed schemes, the D-LDO can achieve fast transient response and low quiescent current simultaneously.

## III. Implementations and Design Considerations

### A. Architecture

Fig. 3(a) shows the block diagram of the proposed D-LDO. As discussed earlier, the PMOS array consists of the coarse and fine sections, driven by their corresponding S/Rs. Both of the S/Rs are controlled by the comparator $\text{CMP}_1$, which senses the difference between $V_{\text{OUT}}$ and $V_{\text{REF}}$ and outputs a control signal $\text{CMP}_{\text{OUT}}$. To extend the load current range, the coarse PMOS array is designed to be with 64 power transistors. The unit size of the coarse PMOS is designed to be 16 times that of the fine PMOS for the loop gain boosting. To cover the current gap between two adjacent CRS, the fine PMOS array is designed with 32 units with sufficient margin.

For the undershoot/overshoot detection, a peak detector is implemented with two comparators ($\text{CMP}_2$ and $\text{CMP}_3$) and an exclusive-OR gate, which outputs 1 if $V_{\text{OUT}}$ is not within the range between $V_{\text{REF\_H}}$ and $V_{\text{REF\_L}}$. All $V_{\text{REF\_H}}$, $V_{\text{REF\_L}}$, and $V_{\text{REF}}$ come from the same resistor ladder such that $V_{\text{REF\_H}}$ and $V_{\text{REF\_L}}$ will follow $V_{\text{REF}}$ during dynamic voltage scaling (DVS).

The output of the peak detector is fed to a control logic block that generates a mode selection signal MOD to determine whether the D-LDO operates in coarse tuning or fine-tuning mode. A fast clock $\text{CLK}_{\text{FAST}} = 500$ MHz is applied to the coarse tuning S/R, while a slow clock $\text{CLK}_{\text{SLOW}} = 50$ MHz is for the fine-tuning S/R. These clocks are typically available for a SoC application. The coarse and fine S/Rs are clock gated by the multiplexers $\text{MUX}_1$ and $\text{MUX}_2$, respectively, which save the quiescent current in both modes, particularly in the fine-tuning mode in steady state. To allow a possible full range CRS change during coarse tuning with sufficient margin, $\Delta T_1$ is designed to be 128 times of the fast clock cycle ($\Delta T_1 = 256$ ns).

### B. Comparators and S/Rs

The schematic of the clocked comparators is given in Fig. 3(b) in which no dc bias current is needed. A latch following the first stage restores the output signal. When the CLK signal is low, the internal nodes will be precharged to high while the latch output keeps unchanged; when the CLK turns high, the comparison will be performed. Thus, dynamic current exists only during the transition periods. Since all the transistors in the clocked comparator will be fully turned on or off, this topology can operate at low supply voltage.

The simplified schematic of the bidirectional S/R is presented in Fig. 3(c), which consists of D-type flip-flops and multiplexers. When $\text{CMP}_{\text{OUT}}$ is high, all the bits are shifted to the right by one count at the rising edge of the sampling clock and vice versa. Accordingly, the number of the turned off PMOS will be increased or decreased by one.

### C. Regulation Compensation

The CFT technique would give rise to the degraded dc regulation, as intuitively shown in Fig. 4(a). It is possible that the coarse tuning ends up with a nearby CRS, rather than the exactly required one, for the desired load current. Then, the FINE may fail to make up for the gap between these two CRS; thus, the dc level of $V_{\text{OUT}}$ will deviate from $V_{\text{REF}}$ to compensate for this gap, degrading the output accuracy.

To address this issue, a regulation compensation technique as in Fig. 3(a) is implemented by defreezing the CRS without coarse tuning once a carry operation is detected. The transient waveforms with this technique are given in Fig. 4(b). Once

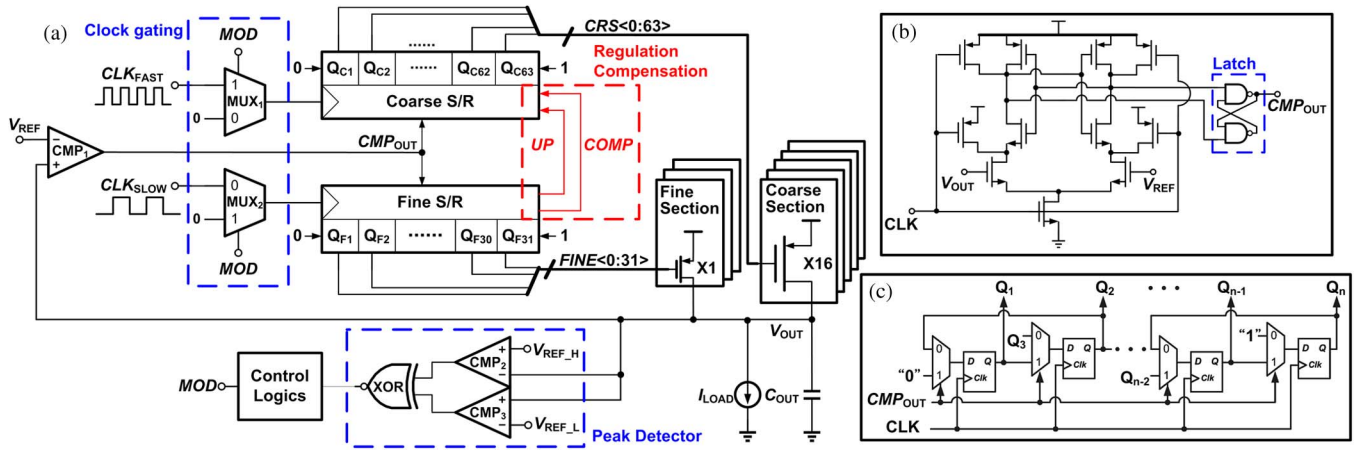


Fig. 3. (a) Block diagram of the proposed D-LDO, and schematics of (b) the clocked comparator with latch and (c) the S/R.

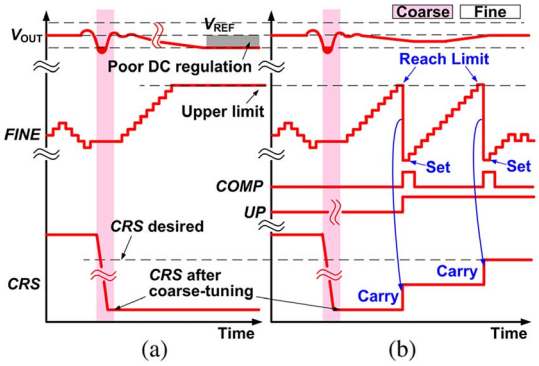


Fig. 4. Transient waveforms of the D-LDO (a) without and (b) with regulation compensation when the fine-tuning range reaches its limit.

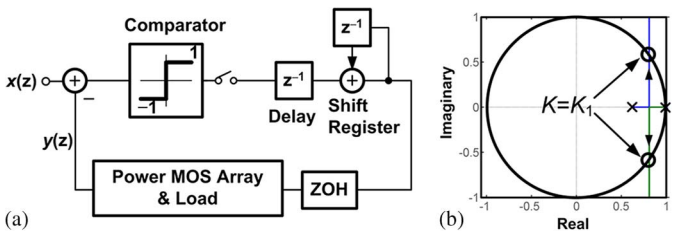


Fig. 5. (a) Small signal model and (b) root locus of the proposed D-LDO.

FINE reaches its upper/lower limits (32/0 in this design), a COMP pulse is generated to activate a carry in/out operation in the CRS, while a UP signal is generated to indicate whether carry in or out takes place in the coarse S/R. Meanwhile, FINE is set to maintain a seamless transition for this carry operation. With the aid of this regulation compensation, the load current accommodation range of fine-tuning is enlarged; thus, the D-LDO is capable of providing the desired load current without reactivating the burst mode.

### *D. Guard Period*

The small signal model of the proposed D-LDO is shown in Fig. 5(a), which is composed of a sampled comparator, an S/R, and a first-order plant driven by a zero-order hold, representing the continuous time plant consisting of the PMOS array and the load. Due to the synchronous sampling in the comparator and the S/R, a $z^1$ is used to model the delay between these two components. The open-loop transfer function of this model $G(z)$ is written as [10]

$$G(z) \propto \frac{K}{(z-1)(z-e^{-T_S/\tau})} \tag{2}$$

where $K$ is the loop dc gain, $\tau$ is the time constant of the output pole, and $T_S$ is the sampling period. The root loci of this system can be plotted in Fig. 5(b).

The root loci cross the unit circle where $K = K_1$. For $0 < K < K_1$, all the roots are inside the unit circle; thus, the system is asymptotically stable. At the crossing point, limit cycle oscillation (LCO) occurs. For this system, since the root position tends to move into the unit circle when $K$ decreases, the amplitudes of the signals grow when the system becomes stable and diminish when unstable [11]. This leads to a stable LCO and a stable system [12]. The frequency and amplitude of the LCO can be calculated by using the describing function method in [13].

Based on the calculation derived in [14], large LCO will be incited in the coarse tuning, which might cause $V_{\rm OUT}$ variation to exceed the boundaries, retriggering an immediate coarse tuning after it ends, as explained by Fig. 6. Assume that the LCO in coarse tuning gives rise to CRS variation from $\rm CRS_H$ to $\rm CRS_L$. If the coarse tuning ends up with $V_{\rm OUT}$ within the boundaries, the fine-tuning will take over the D-LDO and regulates it to the desired value, as shown in Fig. 6(a). However, if $V_{\rm OUT}$ is not within the boundaries, as shown in Fig. 6(b), the peak detector will judge it as another undershoot/overshoot, which immediately incites the coarse tuning again. This traps the D-LDO in the coarse tuning, which will increase the power consumption overhead.

In this brief, a guard period is inserted to prevent the potential trap. As shown in Fig. 6(b), D-LDO will be shielded from the peak detection for a duration of $\Delta T_2$ (the guard period) after the coarse tuning ends. During this guard period, coarse tuning will not be triggered. After that, the D-LDO is released from the guard mode, and peak detection is reactivated. Although this mechanism would temporally prevent D-LDO from fast response, it is acceptable for most of the D-LDO applications as long as $\Delta T_2$ is restrained to a limited time.

From the numerical calculation and transistor-level simulation in [14], the maximum LCO amplitude estimated in this design will be $|\rm CRS_H - CRS_L| = 6$. Hence, fine-tuning needs to compensate a maximum of 3 CRS bits (half of $|\rm CRS_H - CRS_L|$,

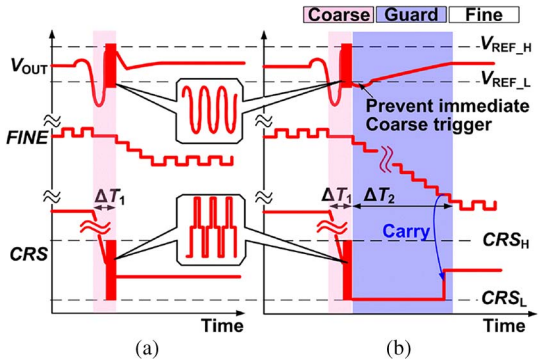


Fig. 6. Transient waveforms of D-LDO with coarse tuning ending when CRS is (a) in the middle of and (b) at the upper/lower limit of the LCO range.

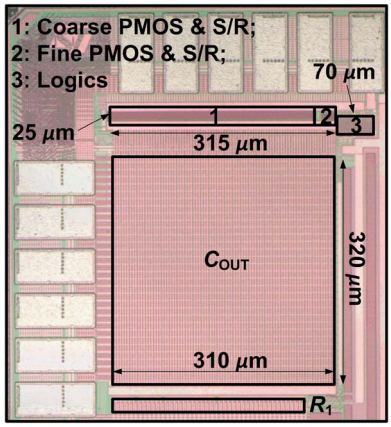


Fig. 7. Microphotograph of the proposed D-LDO.

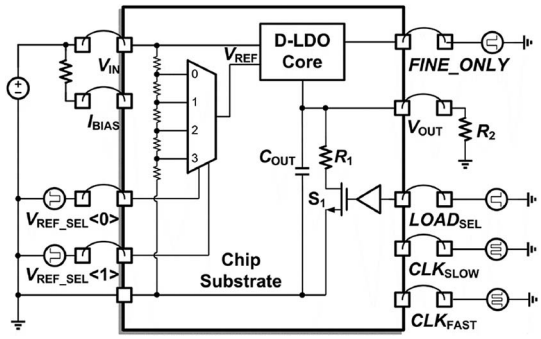


Fig. 8. Measurement setup of the proposed D-LDO.

equivalently 48 FINE bits) if coarse tuning ends up with CRS $=$ CRS$_H$ or CRS$_L$. Therefore, with CLK$_{\rm SLOW}$ $=$ 50 MHz, it will take at most 48 bit $\times$ 20 ns $=$ 0.96 $\mu$s for the D-LDO to be stable, which is chosen as the value of $\Delta T_2$.

## IV. Measurement Results

The proposed D-LDO was implemented in a 65-nm CMOS 1-poly 7-metal process. The chip microphotograph is shown in Fig. 7. The active area of the proposed D-LDO, including coarse/fine PMOS arrays, S/Rs, and logics, is 0.01 mm$^2$. Moreover, the 1-nF on-chip capacitors occupy 0.09 mm$^2$.

The measurement setup of the proposed D-LDO is shown in Fig. 8. An on-chip resistor $R_1$ is connected in series with a switch $S_1$ driven by an on-chip buffer. The light load current is set by an off-chip resistor $R_2$. The static currents of the D-LDO

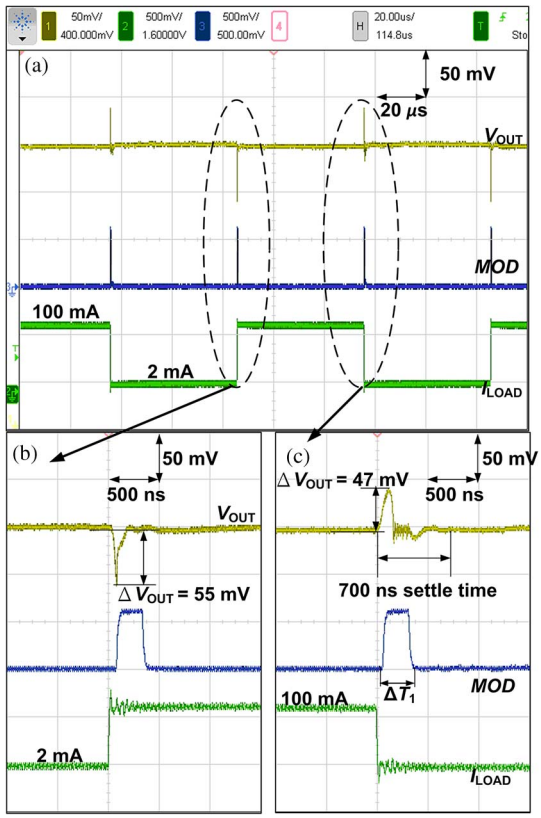


Fig. 9. (a) Measured transient responses with $V_{\rm IN} = 0.6$ V, $V_{\rm OUT} = 0.5$ V, and load change from 2 to 100 mA within edge times of 20 ns. Zoom-in details of $V_{\rm OUT}$ (b) undershoot and (c) overshoot.

with $S_1$ ON/OFF are measured as $I_{\rm max}/I_{\rm min}$, respectively. The quiescent current $I_Q$ is measured with $S_1$ OFF and $R_2$ removed. The reference voltage $V_{\rm REF}$ is generated by an on-chip resistor ladder, which can be selected with the 2-bit off-chip control word $V_{\rm REF\_SEL}\langle 1:0\rangle$. For a comparison, a FINE_ONLY signal can be used to set the proposed D-LDO to a fine-tuning-only mode as a conventional one does.

Fig. 9(a) shows the measured transient response of $V_{\rm OUT}$ with the on-chip load current changing from 2 to 100 mA with the rising/falling edges of 20 ns, while the zoom-in details of the undershoot and overshoot voltages are given in Fig. 9(b) and (c), respectively. During the load transient, the D-LDO needs several clock cycles to change the CRS bits, and the VOUT will keep going upward/downward until a dynamic equilibrium is attained between the load current and the D-LDO output current. Thus, a larger undershoot/overshoot will happen with faster edges. The measured undershoot and overshoot voltages are 47 and 55 mV, respectively, and a 700-ns settling time, consisting of $\Delta T_1$ and a fraction of $\Delta T_2$, is achieved. Here, $V_{\rm IN}$ is 0.6 V, whereas $V_{\rm REF}$ is 0.5 V, and the measured $I_Q$ of the D-LDO core is 82 $\mu$A. Fig. 10 shows the comparison of the measured undershoots of $V_{\rm OUT}$ with and without the proposed techniques, by setting the FINE_ONLY signal, under the same testing conditions used in Fig. 9. The rising edge of the load current is intentionally shifted for clarity. Moreover, $\Delta V_{\rm OUT}$ is reduced from 340 to 55 mV with the proposed techniques.

To ensure the DVS function, the $V_{\rm REF}$ control word $V_{\rm REF\_SEL}\langle 1:0\rangle$ is repeatedly set to 10, 11, 01, and 00 for $V_{\rm OUT} = 0.5$, 0.55, 0.45, and 0.4 V, respectively, with a 0.6-V $V_{\rm IN}$. Fig. 11(a) shows that the $V_{\rm OUT}$ can accurately follow the

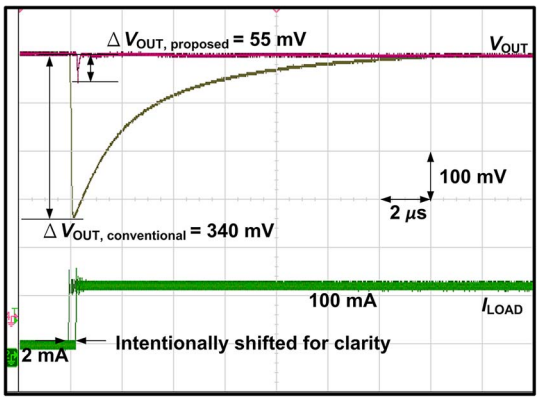


Fig. 10. Comparison of the measured $\Delta V_{\mathrm{OUT}}$, with and without the proposed CFT and burst-mode techniques.

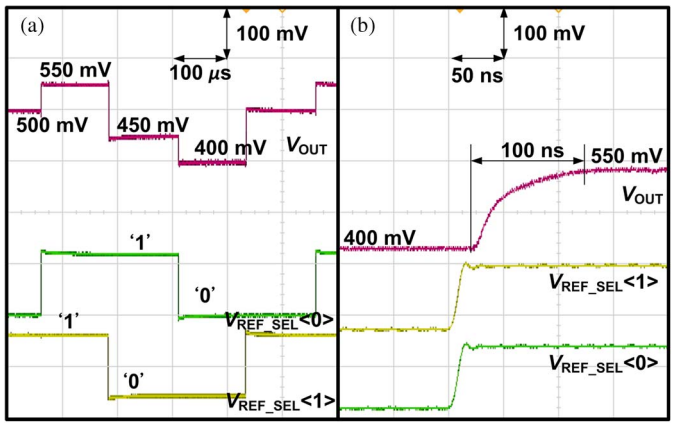


Fig. 11. (a) Measured waveforms of the overall DVS function. (b) Zoom-in details of $V_{\mathrm{REF}}$ tracking from 400 to 550 mV. All with $V_{\mathrm{IN}} = 0.6$ V.

TABLE I
COMPARISON WITH STATE-OF-THE-ART D-LDOS

| | [7] 2013 | [5] 2015 | [10] 2015 | This work |
|---|---|---|---|---|
| **Process (nm)** | 180 | 110 | 130 | **65** |
| **Active area ($mm^2$)** | 0.81 | 0.04 | 0.114 | **0.01** |
| **$V_{\mathrm{IN}}$ range (V)** | 0.9-1.8 | 0.6-1.2 | 0.5-1.2 | **0.6-1.1** |
| **$V_{\mathrm{OUT}}$ range (V)** | 0.8-1.5 | 0.5-0.9 | 0.45-1.14 | **0.4-1** |
| **$C_{\mathrm{OUT}}$ (nF)** | 1000 | 1 | 1 | **1** |
| **$I_{\mathrm{Q}}$ ($\mu$A)** | 750 | 32 | 78 | **82** |
| **Peak current eff. (%)** | 99.6 | 99.96 | 98.3 | **99.92** |
| **Line reg. (mV/V)** | N/A | 2 | N/A | **3** |
| **Load reg. (mV/mA)** | N/A | 0.3 | <10 | **0.06** |
| **Edge time (ns)** | 100 | 25000 | N/A | **20** |
| **Load step (mA)** | 1-100 | 80 | 0.5-2 | **2-100** |
| **$\Delta V_{\mathrm{OUT}}$ (mV)** | 70 | 53 | <40 | **55** |
| **FOM (ps)** | 5250 | 0.26 | 76.5 | **0.43** |
| **Settling time ($\mu$s)** | 4 | 38 | 1.1 | **0.7*** |
| **DVS speed (V/$\mu$s)** | N/A | N/A | N/A | **1.5** |

* The maximum possible settling time is $\Delta T_1 + \Delta T_2 \approx 1.2$ $\mu$s from calculation.

$V_{\mathrm{REF}}$ variations. Zoom-in details of tracking $V_{\mathrm{REF}}$ from 400 to 550 mV are given in Fig. 11(b), with $V_{\mathrm{REF\_SEL}}\langle 1{:}0\rangle$ switching from 00 to 11. It takes 100 ns for the D-LDO output to track a 150-mV reference voltage step, which corresponds to a tracking speed of 1.5 V/$\mu$s and makes it fit for fast DVS.

Table I compares the performance metrics between this design and the other state-of-the-art works [5], [7], and [10]. In this table, output capacitors have been excluded for all the active area calculations. A widely used figure of merit (FOM) of speed [15] is employed as FOM $= C_{\mathrm{OUT}} \cdot \Delta V_{\mathrm{OUT}} \cdot I_Q/(I_{\mathrm{MAX}})^2$, and thus, a 0.43-ps FOM is calculated for this design. As observed from the table, the proposed D-LDO has achieved comparable or better performances than the recent state-of-the-art works.

## V. CONCLUSION

A fully integrated D-LDO with CFT and burst-mode techniques for fast transient response and low quiescent current has been proposed and demonstrated in 65-nm CMOS. By boosting the D-LDO loop gain and sampling frequency when voltage undershoot/overshoot is detected, the measured undershoot voltage is reduced from 340 to 55 mV, under a 2–100-mA load step within a 20-ns edge time. On the other hand, with the burst-mode operation, the current efficiency is not degraded, which is measured to be 99.92% in the steady state. With these techniques, a 0.43-ps FOM of speed is thereby achieved with negligible power and area overheads.

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