A 220-MHz Bondwire-Based Fully-Integrated KY Converter With Fast Transient Response Under DCM Operation

Wen-Liang Zeng, *Student Member, IEEE*, Chi-Seng Lam, *Senior Member, IEEE*, Sai-Weng Sin, *Senior Member, IEEE*, Franco Maloberti, *Life Fellow, IEEE*, Man-Chung Wong, *Senior Member, IEEE*, and Rui Paulo Martins, *Fellow, IEEE*

***Abstract*— This paper presents a 220-MHz pulse width modulation (PWM) fully integrated KY dc–dc step-up converter utilizing bondwire as power inductor, with discontinuous conduction mode (DCM) calibration control. We develop the first DCM closed-loop PWM controller for the KY converter, including: 1) its parameter design; 2) a DCM closed-loop voltage mode control with Type II compensator; 3) a zero current detection method to activate DCM control; and 4) a DCM calibration loop. Fabricated in 65-nm CMOS, the designed KY converter core occupies 0.93 mm^2 and achieves an output conversion range of 1.5–2 V from a 1.2-V input. The measured peak efficiency is 75.2% at 97.5 mW. With a 500-ps rising/falling time of the load current step (56 mA), the undershoot/overshoot is 245/205 mV at 146-/140-ns recovery time, and the dc–dc converter achieves a settling time per load transient step of 2.6 ns/mA, which is competitive with the state-of-the-art boost converters.**

***Index Terms*— Fully integrated KY converter, boost converter, PWM, discontinuous conduction mode (DCM), zero current detection (ZCD), load transient response, voltage ripple, bondwire inductor.**

I. Introduction

IN RECENT years, IoT (Internet of Things) and SoC (System-on-Chip) require compact size, power-efficient, fast response and a stable power management unit, then, a fully integrated DC-DC converter is a good candidate to target those applications [1]. It benefits from less noise and smaller parasitic loss without expensive off-chip components [2]. Analog circuits such as the audio or the RF power amplifiers may require a step-up function DC-DC converter, tht use either an inductor- or a switched-capacitor-based DC-DC boost converter [3].

As for the conventional inductor-based boost and buck-boost converters, their output currents are pulsating, thereby causing a large output voltage ripple [4], [5]. Moreover, they have a right-half-plane zero (RHPZ) in the continuous conduction mode (CCM), thereby lowering the system stability with poor load transient responses [3]. The switched-capacitor (SC) based boost converter is simple to integrate on-chip, but its conversion range is small, and the conversion efficiency is limited by the topology [3], [6].

To overcome those drawbacks referred above, a boost converter named KY converter was original proposed by Hwu and Yau [7] for power electronics applications in 2007, as Fig. 1 shows. This converter comprises a switched- capacitor charge pump converter and a buck converter, and combines the advantages of both converters and exhibits the characteristics of non-pulsating output current, low output voltage ripple and no RHPZ in CCM [7], [8]. The CCM operation principles and control of the KY converter have been presented and discussed in [3] and [9]. In 2017, the KY converter integrated

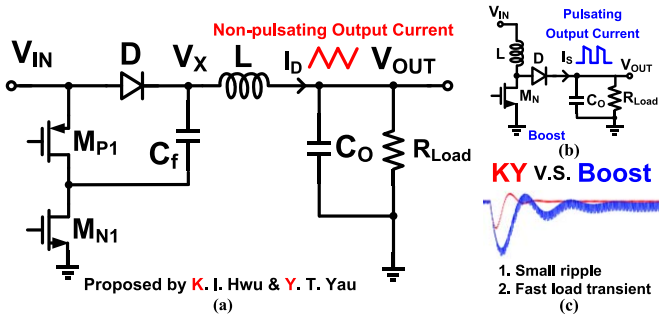

Fig. 1. (a) KY converter. (b) Conventional boost converter. (c) Comparison in terms of ripple and load transient response between the KY and the conventional boost converters.

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W.-L. Zeng, S.-W. Sin, and M.-C. Wong are with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau 999078, China, and also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macau 999078, China.

C.-S. Lam is with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau 999078, China (e-mail: cslam@umac.mo; c.s.lam@ieee.org).

F. Maloberti is with the Department of Electrical, Computer and Biomedical Engineering, University of Pavia, 27100 Pavia, Italy.

R. P. Martins is with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau 999078, China, and also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macau 999078, China, on leave from the Instituto Superior Técnico, Universidade de Lisboa, 1649-004 Lisbon, Portugal.

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circuit (IC) with off-chip passive components under CCM operation [3] has been implemented, which confirmed its low output voltage ripple, fast load transient response and high-efficiency characteristics.

Recently, both industry and academia have shown great interest in the fully integrated DC-DC converter, based on the considerations of the limited and compact size in a SoC or in an IoT application. If fully integrated, when compared with the inductor-based boost converter, the KY converter has potential to obtain a smaller output voltage ripple and a faster load transient response. On the other hand, when compared with the SC based boost converter, the KY converter has wider output conversion range and larger power density. As a result, this work focuses on the design and study of a fully integrated KY converter. When the KY converter is fully integrated on-chip or in a package, due to a small inductance and load variation, its discontinuous conduction mode (DCM) operation cannot be avoided for longer battery life. In 2015, we already developed the necessary DCM operation principles of the KY converter [10], but the design and control of the DCM closed-loop controller of the KY converter still lacks studies among the existing literature [3], [7]–[11].

In this paper, we implement a fully integrated KY converter IC under DCM operation in 65-nm CMOS, presenting, as well the details of its circuits and system design. Since this is the first design of the KY converter IC under DCM operation, there are many challenges that need to be solved, such as the zero current detection (ZCD) and the DCM control. In particular because the detection and control methods developed for the conventional inductor-based buck or boost converter cannot be directly applied. The main contributions of this work are:

1. Design of a fully integrated KY converter utilizing bondwire inductor under DCM operation;
2. Parameters design of the KY converter under DCM operation;
3. Design of a PWM voltage mode control with a Type II compensator based on the developed DCM operation theory [10];
4. Design of a DCM calibration loop with load transient enhancement circuitry [2] for KY converter;
5. Proposal for a ZCD method to activate the DCM calibration loop control.

II. DCM Operation Principle and Parameter Design of the KY Converter

Fig. 2(a) shows the KY converter IC topology under DCM operation, where V_{IN} and V_{OUT} are DC input and output voltages; C_f and V_{Cf} are the flying capacitor and its voltage ($V_{Cf} = V_{IN}$ in the ideal case [8]); L and C_O are the inductor and capacitor of the LC filter; R_{Load} is the load resistor; I_{IN}, I_{Load}, I_{Cf}, I_L and I_{Co} are the input, load, flying capacitor, inductor and capacitor currents. The KY converter contains three power transistor switches (M_{P1}, M_{P2} and M_{N1}).

In State 1 as shown in Fig. 2(b), M_{P2} and M_{N1} turn off and only M_{P1} turns on. The input current I_{IN} flows through C_f and L. In this state, C_f is discharged and L is magnetized. Since V_X is charged to V_{IN} in State 2 as shown in Fig. 2(c), V_X is equal to $2V_{IN}$ in State 1 in the ideal case.

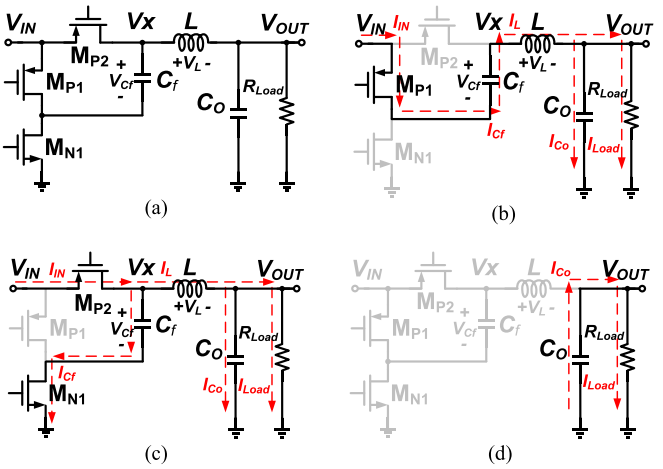


Fig. 2. DCM operation of the KY converter in IC. (a) Overall circuit. (b) State 1: Inductor L magnetized and C_f discharged. (c) State 2: Inductor L demagnetized and C_f charged. (d) State 3: Output capacitor C_O discharged.

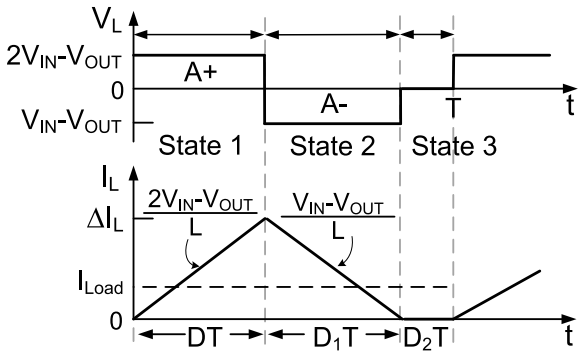


Fig. 3. Idealized V_L and I_L waveforms of KY converter in DCM.

In State 2, both M_{P2} and M_{N1} turn on and M_{P1} turns off. Hence the input current I_{IN} flows into both L and C_f. In this state, C_f is charged and L is demagnetized. V_X is equal to V_{IN} in State 2 in the ideal case.

In State 3, all the switches turn off, and the loading current I_{Load} is maintained by the output capacitor C_O, where C_O is discharged. V_X is a floating voltage in State 3.

Fig. 3 shows the KY converter idealized inductor voltage V_L and current I_L waveforms for DCM [10].

A. The CCM/DCM Boundary of the KY Converter

The boundary between CCM and DCM can be defined as when $D_2 = 0$ in Fig. 3. The peak inductor current ΔI_L can be deduced, then the average DC output load current I_{LoadB} at the boundary can be expressed as:

$$I_{\mathrm{LoadB}} = \frac{\Delta I_L}{2} = \frac{(2V_{IN} - V_{OUT})\,D}{2 f_s L} \tag{1}$$

where f_s is the switching frequency and D is the duty cycle for the State 1. (1) can help to determine the relationship among the required inductor value L, switching frequency f_s and the operation boundary.

B. C_f Design of the KY Converter in DCM

In the KY converter design under CCM operation [8], as the switching frequency is not fast ($f_s = 1$ MHz), those passive components including the fly capacitor C_f are usually off-chip. Thus C_f can be selected with a larger value to keep $V_{Cf} \approx V_{IN}$ as in the ideal case model, allowing the V_{Cf} variation effect to be simply neglected. However, when the KY converter is designed to be fully integrated (usually $f_s \geq 50$ MHz), the V_{Cf} variation cannot be ignored, hence, it yields the design constraint of the minimum on-chip C_f value requirement. In this KY converter, as a result, the voltage variation/drop over the on-chip C_f should be considered, where the minimum on-chip C_f value requirement will be deduced and discussed.

In State 1, the inductor L is magnetized and the fly capacitor C_f is discharged, the charge from C_f (Q_{Cfdis}) totally flows into L (Q_{Lmag}) if we neglect the parasitic loss. According to Fig. 3, we get

$$Q_{Cfdis} = Q_{Lmag} = \frac{1}{DT}\int_0^{DT} i_L dt = \frac{1}{DT}\int_0^{DT} i_{cf} dt \quad (2)$$

and also from Fig. 3,

$$I_{Load} = \frac{\Delta I_L (D + D_1)}{2} = \frac{V_{OUT}}{R_{Load}} \quad (3)$$

$$Q_{Cfdis} = C_f \Delta V_{Cf} \quad (4)$$

where ΔV_{Cf} is the flying capacitor voltage deviation. Then, substituting (3) and (4) into (2) yields,

$$\Delta V_{Cf} = \frac{Q_{Cfdis}}{C_f} = \frac{2DV_{OUT}}{b(D + D_1)} \quad (5)$$

where $b = 2f_s C_f R_{Load}$ [10]. Now, considering the influence of C_f (V_{Cf} variation) in State 1, V_L is not equal to $2V_{IN} - V_{OUT}$ as in the ideal case, but V_L is equal to

$$V_L = 2V_{IN} - V_{OUT} - V_{Cf}(t) \quad (6)$$

In State 1, V_L should always be kept as a positive value, which means at least

$$2V_{IN} - \Delta V_{Cf} - V_{OUT} > 0 \quad (7)$$

and then applying the volt-second balance principle, yielding,

$$(2V_{IN} - \Delta V_{Cf} - V_{OUT})DT_s = (V_{OUT} + \Delta V_{Cf} - V_{IN})D_1 T_s \quad (8)$$

leads to the DCM DC gain of the KY converter given by:

$$M_{VDC} = \frac{V_{OUT}}{V_{IN}} = \frac{2D}{D + D_1 + \frac{2D}{b}} \quad (9)$$

Finding D_1 from (9) and substituting it and (5) into (7) imposes that,

$$C_f > \frac{M_{VDC}}{f_s R_{Load}(2 - M_{VDC})} \quad (10)$$

We can plot a graph with (10), and the design constraint of the minimum on-chip C_f value can be found from Fig. 4.

With $V_{IN} = 1.2$ V and target $V_{OUT} = 1.8$ V, $f_s = 220$ MHz, $M_{\mathrm{VDC}} = 1.5$, $R_{Load} = 30\Omega$, the required C_f values can be found via Fig. 4, which is 455 pF without considering all the losses. Finally, we select a 600 pF capacitor in this work. Fig. 5 presents the simulation results of V_{OUT} under $C_f = 400$ pF and 600 pF, in which V_{start} is a starting step voltage signal, in which the details will be discussed in next Section. During the start-up process, a duty ratio is generated to achieve a V_{OUT} slightly larger than the target value. After that, the voltage-mode (VM) feedback loop will be activated. In the VM loop control process, when $C_f = 400$ pF, the converter fails to achieve the target V_{OUT}. When $C_f = 600$ pF, V_{OUT} can achieve the target 1.8 V. Finally, the simulation result as shown in Fig. 5 verifies the minimum on-chip C_f design constraint in (10).

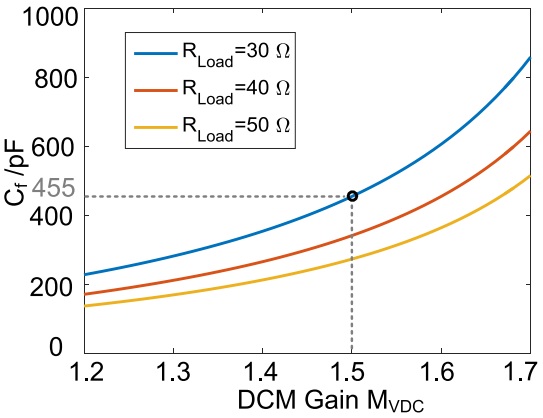


Fig. 4. C_f versus M_{VDC} with different R_{Load} when $f_s = 220$ MHz.

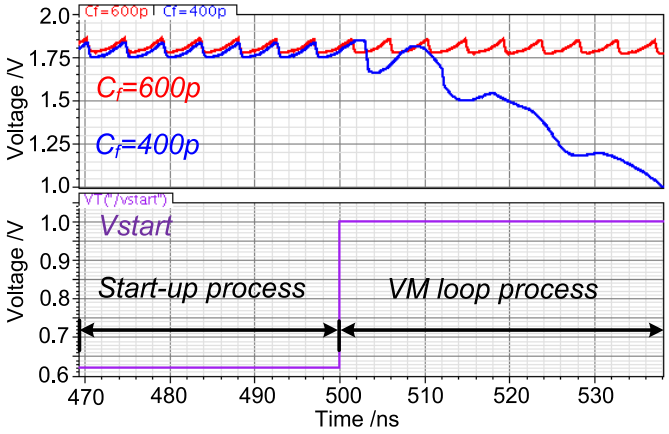


Fig. 5. V_{OUT} waveform when $V_{IN} = 1.2$ V and target $V_{OUT} = 1.8$ V, $f_s = 220$ MHz and $R_{Load} = 30\ \Omega$, with $C_f = 400$ pF and 600 pF.

Fig. 6 shows the relationship between the power efficiency and the flying capacitor C_f size with $V_{IN} = 1.2$ V, $V_{OUT} = 1.8$ V and $R_{Load} = 30\ \Omega$. It can be observed that the power efficiency just improves by about 2% if the flying capacitor size is doubled. However, doubling it requires an additional 60% active core chip area, which is not cost-effective.

The output power of KY converter depends on flying capacitor size. When the output voltage increases, the maximum load current decreases. Refer to (4) and (7), the maximum charge that flows away from the flying capacitor to the power inductor

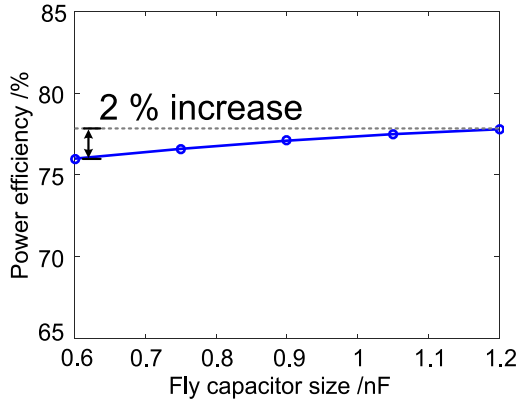


Fig. 6. The efficiency versus flying capacitor C_f size.

of the KY converter can be defined as:

$$Q_{Cfdis\_max} = C_f(2V_{IN} - V_{OUT}). \tag{11}$$

According to (11), when V_{OUT} increases, the maximum charge Q_{Cfdis_max} can be delivered from the flying capacitor to the power inductor is smaller, thus the maximum output load current is smaller.

The following two sections summarize the DCM DC gain M_{VDC} and the DCM small-signal transfer function of the KY converter directly, as the deduction details and analysis can be found in [10].

C. DCM DC Gain of the KY Converter

Assuming that $k = \frac{2Lf_s}{R_{Load}}$ and ignoring the variation of the fly capacitor voltage V_{Cf}, the DCM DC gain of the KY converter can be obtained as [10]:

$$M_{VDC} = \frac{V_{OUT}}{V_{IN}} = \frac{\left(1 - \frac{D^2}{k}\right) + \sqrt{\frac{D^4}{k^2} + \frac{6D^2}{k} + 1}}{2} \tag{12}$$

If the V_{Cf} variation is considered as well, then the DCM DC gain becomes (13), as shown at the bottom of this page.

D. Small-Signal Transfer Function of the KY Converter for DCM

With the average switch modeling technique in DCM [12], we can obtain the small-signal transfer function G_{vd} of the KY converter in DCM, with the DCM DC gain expressed in (13) [10] leading to,

$$G_{vd} = \frac{\hat{V}_{OUT}}{\hat{d}} = H_d \frac{1 + {}^{s}\!/_{s_{z1}}}{1 + a_1 s + a_2 s^2} \tag{14}$$

where the details of the parameters H_d, a_1, a_2 and S_{z1} in (14) can be found in [10], as well.

III. Circuit Implementation

Fig. 7 shows the overall system block diagram of the proposed fully integrated KY converter under DCM operation. The active circuits are power stages (M_{P1}, M_{P2} and M_{N1}), start-up control, Type II compensator, ramp generator, zero current detector (ZCD), DCM calibration loop, logic and drivers. The passive components are input decoupling capacitors C_{IN} and C_{IO}, flying capacitor C_f, bondwire inductor L and output capacitor C_O, and scalar resistors R_A and R_B.

The C_{IO} is connected between V_{IN} and V_{OUT} to reduce the output ripple by using a smaller area when compared with the case of using C_{IN} only [13]. When we consider the passive capacitors within a given area, it is usually a good choice to select a reasonable C_{IO} in the fully integrated KY step-up converter. This, because C_O has to be designed with thick oxide MOS-cap to prevent the capacitor material from over voltage damaging, while it is not the case in C_{IO}. C_{IO} can be designed with thin-oxide MOS-cap. Therefore, the capacitance density will be larger in this case. Also, we utilize here the single-boundary delay-bug-free ramp generation for a high-frequency converter as proposed in [2]. We describe the detailed circuit implementation of each subsystem in the following sections.

A. Fully Integrated KY Converter Design in DCM

With the battery input voltage, V_{IN} = 1-1.2 V and the output voltage ranges from V_{OUT} = 1.5-2 V, the KY converter chip has been fabricated in standard 65-nm CMOS. As a fully integrated KY converter utilizing bondwire inductor as the power inductor to achieve a compact size design target, the inductor value may vary from 3 nH to 8.5 nH [2]. After the measurement, the resistance per millimeter of bondwire is 60 mΩ.

It is evident that the KY converter operates in CCM when $I_{Load} > I_{LoadB}$, and DCM otherwise. We can calculate the range of switching frequency f_s such that the KY converter is operating in DCM for all loading conditions from (1):

$$f_s < \frac{(2V_{IN} - V_{OUT})\,D}{2I_{Load\_max}L_{max}} \tag{15}$$

Based on (15), the switching frequency f_s can be designed such that the KY converter is operating in DCM for all loading conditions. According to the design specifications of the KY converter (i.e. V_{IN} = 1.2 V, V_{OUT} = 1.8 V, D = 0.5, maximum bondwire inductance L_{max} = 8.5 nH [2], and the maximum load current I_{Load_max} = 80 mA), we can obtain f_s < 220.6 MHz. Finally, we chose f_s = 220 MHz as the switching frequency.

B. Start-Up Control for the KY Converter

In the KY converter, during the initial start-up, the PWM voltage-mode (VM) loop usually works only after V_{OUT} >

$$M_{VDC} = \frac{-\left(kD^2b - k^2b - 4D^5\right) + \sqrt{\left(kD^2b - k^2b - 4D^5\right)^2 - 4\left(k^2b + D^5\right)\left(4D^5 - 2kD^2b\right)}}{2} \tag{13}$$

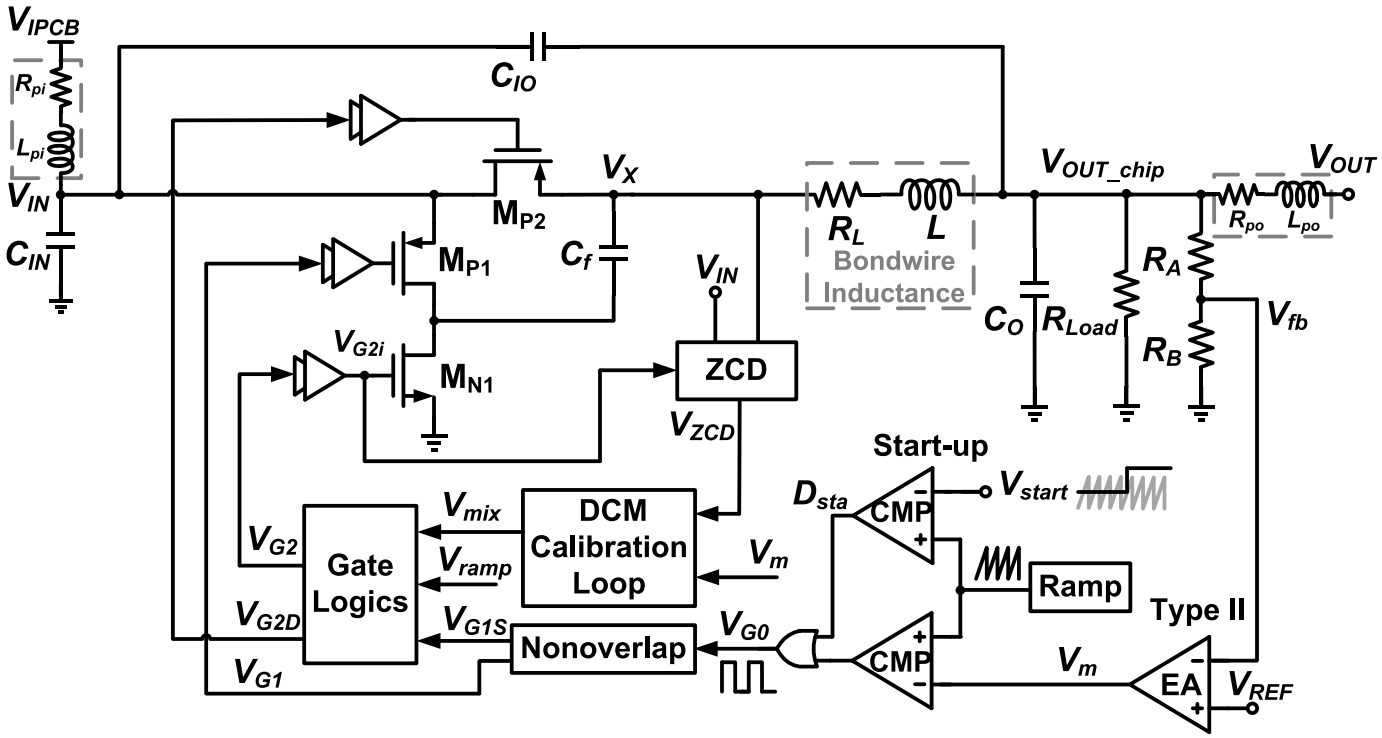


Fig. 7. Block diagram of the proposed fully integrated KY converter under DCM operation (overall system).

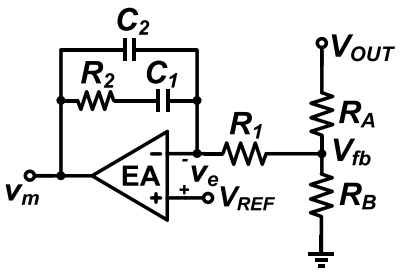


Fig. 8. Integral-single-lead (Type II) compensator.

target V_{OUT} happens. In this work, we provide a starting step voltage signal V_{start} off-chip to be compared with the ramp signal in order to obtain an initial duty ratio D_{sta} during the start-up. After the system starts up, V_{start} will be higher than the peak voltage of the ramp signal then implying that $D_{sta} = 0$, thus it has no effect on the VM loop.

C. Type II Compensator for the KY Converter in DCM

In the PWM voltage-mode control of the KY converter under DCM operation, through appropriate design of the system parameters, the Type II compensator of Fig. 8 can already ensure system stability. This is an integral-single-lead compensator, also called a second-order integral-lead controller or type II controller, whose maximum phase boost is 90° [5]. The error amplifier (EA) in the compensator is a telescope single stage amplifier for higher gain accuracy. As it has small output swing, the ramp signal voltage level should be designed carefully.

According to [5], assuming the operational amplifier is ideal, the voltage transfer function $G_{comp}(s)$ of the Type II compensator (Fig. 8) is given by:

$$G_{comp}(s) \equiv \frac{v_m(s)}{v_e(s)} = \frac{B(1+\frac{S}{\omega_{ZC}})}{K^2 s(1+\frac{s}{\omega_{pc}})} \tag{16}$$

Where

$$h_{11} = \frac{R_A R_B}{R_A + R_B} \tag{17}$$

$$B = \frac{1}{C_2(R_1 + h_{11})} \tag{18}$$

$$\omega_{zc} = \frac{1}{R_2 C_1} \tag{19}$$

$$\omega_{PC} = \frac{C_1 + C_2}{R_2 C_1 C_2} \tag{20}$$

$$K = \sqrt{\frac{\omega_{PC}}{\omega_{ZC}}} = \sqrt{\frac{C_1}{C_2} + 1} \tag{21}$$

Based on the KY converter small-signal transfer function in DCM (14) and the Type II compensator transfer function (16), we can set the crossover frequency $f_c = 20\ MHz < \frac{1}{5} f_s$ [14] and the phase margin should be larger than 76° [15], and we can obtain the parameters (R_1, R_2, C_1, C_2) of the compensator. Fig. 9 shows the KY converter system loop gain bode plot with $R_1 = 10$ kΩ, $R_2 = 37.3$ kΩ, $C_1 = 681$ fF, $C_2 = 83$ fF. The compensator is designed with $L = 3$ nH case due to the variation of the bondwire inductance, another case of $L = 8.5$ nH is added, as well, to confirm that the compensator works well.

D. Zero Current Detection in the KY Converter

The inductor reverse current $i_{L,reverse}$ can be detected by using a zero current detection (ZCD) circuit as Fig. 10 shows,

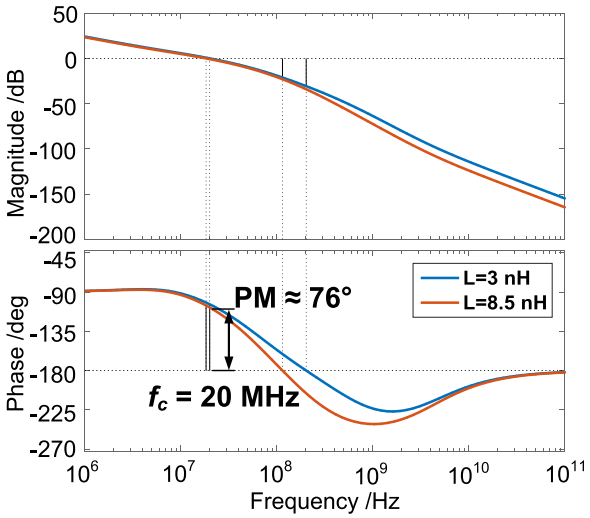


Fig. 9. The loop gain bode diagram of the designed KY converter in: $L = 3$ nH and $L = 8.5$ nH.

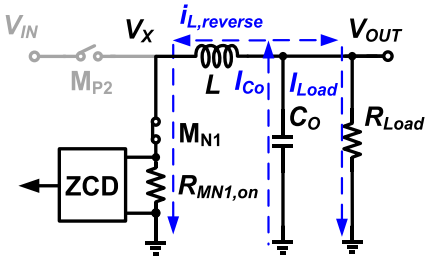


Fig. 10. Conventional ZCD for buck converter.

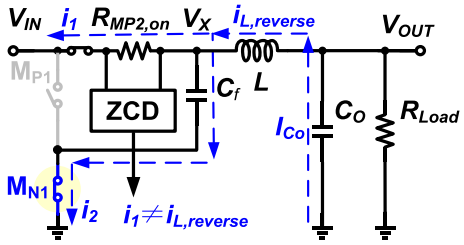


Fig. 11. Problem of conventional ZCD for KY the converter.

the idea is to compare the voltage between the two terminals of a power transistor switch. From Fig. 10, it is evident that we obtain the reverse current information by comparing V_X and GND nodes directly in a buck converter. When the reverse current happens, $V_X > 0$, the ZCD output is activated. However, the conventional ZCD for buck converter cannot be directly applied to the KY converter, because there are two paths for the $i_{L,reverse}$ to flow at the node V_X during State 2, thus the reverse current cannot be detected correctly, as Fig. 11 illustrates. There, i_1 is the current flow through M_{P2} and i_2 denotes the current flow through M_{N1}.

To solve the ZCD problem of the KY converter, we propose a solution in Fig. 12(a) which turns off the switch M_{N1} earlier than M_{P2} (M_{P2} on resistance = $R_{MP2,ON}$) by a short detection sample period (T_{WIN} = 200 ps, ZCD state) with V_{WIN} as

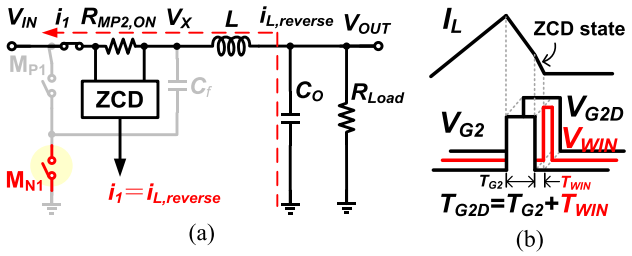


Fig. 12. Proposed ZCD for KY converter: (a) circuit and (b) gate signal.

the sampling signal, thus two paths at the node V_X during State 2 can be reduced to one path for i_L reverse current detection, which means that the ZCD condition $i_1 = i_{L,reverse}$ is valid. Thus, we can detect whether the current flows across M_{P2} ($R_{MP2,ON}$) is reversed or not at this short sample period, by comparing V_X and V_{IN}. If $V_X > V_{IN}$, there is a reverse current flow, then the ZCD output is activated. Fig. 12(b) shows the corresponding gate signals. Originally, the gate signal V_{G2} controls both M_{N1} and M_{P2}, and now it controls M_{N1} only, while the gate signal V_{G2D} controls M_{P2}. The turn-on period T_{G2D} for V_{G2D} is longer than that (T_{G2}) of V_{G2} by a T_{WIN}. During T_{WIN}, V_{IN} and V_X are compared to justify whether switches M_{N1} and M_{P2} should be turned off earlier or later in the next cycle.

E. DCM Calibration Loop for the KY Converter

Under DCM operation, the inductor reverse current $i_{L,reverse}$ significantly reduces the power conversion efficiency of a fast switching PWM-controlled DC-DC converter, hence a precise DCM calibration loop with load transient enhancement control has been proposed to solve this problem for a buck converter in [2] and [16]. The calibration loop can fine-tune the control signals to enable precise DCM operation (zero inductor current point) after some operation cycles. Thus, the reverse current and efficiency can be significantly reduced and improved. Moreover, we implement this calibration loop with a load transient enhancement circuit, which can improve the load transient speed. Fig. 13 shows the proposed ZCD and DCM calibration loop with load transient enhancement control circuitry [2] for the KY converter under DCM operation.

In the ZCD sampling window block, V_X is sampled right after M_{N1} is turned off, once a falling edge is detected, a sampling window control signal V_{WIN} with 200 ps long is generated. As V_X is either equal to V_{IN} or $2V_{IN}$ in the ideal case, an inverter using thick oxide 2.5 V transistor is used instead of the 1.2 V thin oxide transistor to prevent overvoltage situation. Then the V_{IN} signal and the sampled V_X as V_{X_Sample} are applied to a level shifter to pull the level down to 1/2 V_{DD} for the inputs of the error amplifier (EA) in State 2. This, because both V_X and V_{IN} can be as high as V_{DD}, which is challenging for the EA inputs. The EA samples the error between two signals at the sampling period. When V_{IN} is larger than V_{X_Sample}, it means that the inductor current is positive and the power transistor switch M_{p2} and M_{N1} should be turned off later. Then V_{mix} increases, and the response of the calibration loop results in a longer period

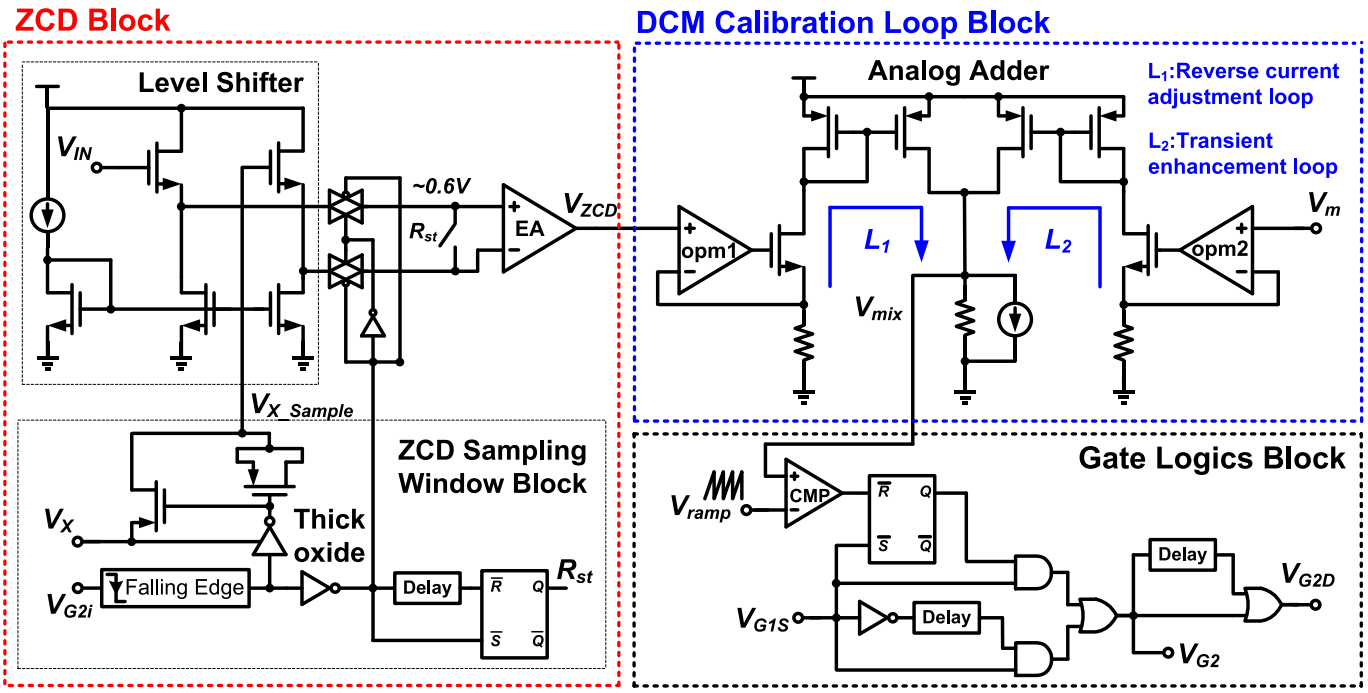


Fig. 13. Proposed ZCD and DCM calibration loop with load transient enhancement circuitry [2] for the KY converter under DCM operation.

TABLE I

DIFFERENCES BETWEEN THE ZCD AND DCM CALIBRATION LOOP CONTROL STRATEGY (THIS WORK AND [2])

	This work (Step-up)	[2] (Step-down)
Signals for ZCD	Sample V_{IN}, V_X	Sample GND,V_X
ZCD action	Detection in "ZCD state"	Detection in State 2
Level shifter	Pull down	Pull up
Sample window	Thick oxide transistor	Thin oxide transistor
Output logics	Two output signals	One output signal

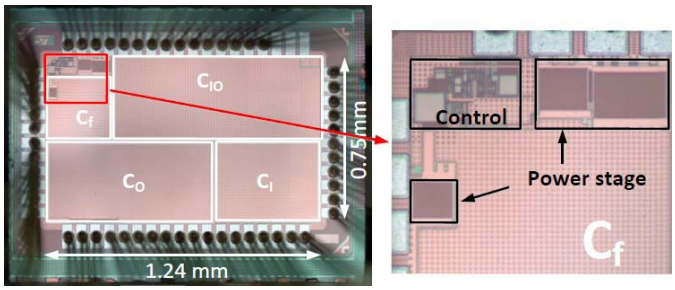
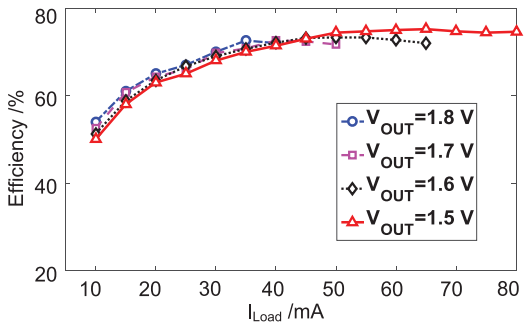
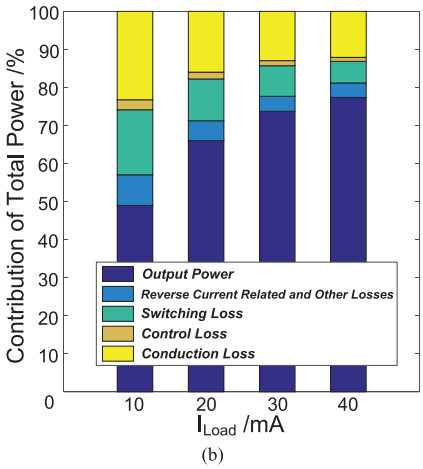


Fig. 14. Chip microphotograph of the proposed KY converter in DCM.



(a)



(b)

Fig. 15. (a) Measurement power efficiency of the proposed KY converter for V_{IN} = 1.2 V and V_{OUT} = 1.5, 1.6, 1.7, 1.8 V under different load current. (b) Power distribution graph under V_{IN} = 1.2 V, V_{OUT} = 1.8 V and I_{Load} = 10 – 40 mA based on post layout simulation.

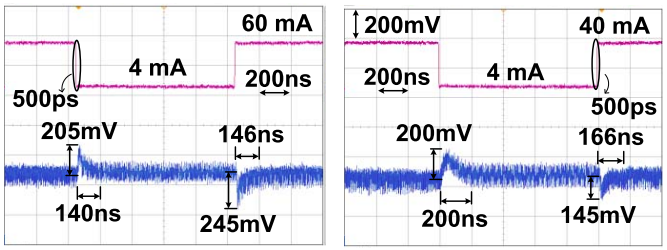
of V_{G2} and V_{G2D} signal. In contrast, when V_{X_Sample} is larger than V_{IN}, it means that the inductor current is negative (reverse current happens) and the power transistor switch M_{P2} and M_{N1} should be turned off earlier. Then V_{mix} decreases, the response of the calibration loop results in a shorter period of V_{G2} and V_{G2D} signal. With this reverse current calibration loop L_1, the precise DCM operation can be achieved dynamically to adjust the KY converter power switches M_{N1} and M_{P2} (V_{G2} and V_{G2D}) turn-on period according to the reverse current level.

From Fig. 13, there are two feedback loops adding together forming the DCM calibration loop. L_1 is the reverse current calibration loop and L_2 is the load transient response

TABLE II
COMPARISON WITH STATE-OF-THE-ART BOOST CONVERTERS

	C. Huang JSSC 13 [2]	N. Tang TPEL 17 [19]	M. Kar JSSC 17 [20]	M. Wens ESSCIRC 07 [21]	D. Bhatia JSSC 13 [22]	T. Das TPEL 14 [23]	S. Dam TPEL 18 [24]	This work
Topology	Inductive Buck	Inductive Buck	Inductive Buck	Inductive Boost	Inductive Boost	SC Boost	Inductive Boost + LC filter	KY (Step-up)
Level of integration	Full (Bondwire L)	Full (Planar Spiral L)	Full (Bondwire L)	Full (Bondwire L)	Off-Chip L&C	Full	Off-Chip L	Full (Bondwire L)
Process /nm	130	65	130	180	130	180	180	65
Switching freq. (f_s) /MHz	100	450	125	100	100	80	118	220
Inductor (L) /nH	3-8.5	1	11.8	18	22*4	---	20	3-8.5
Output capacitor (C_o) /nF	9.8	4	3.2	1.3	20	0.05	1.08	1
Flying capacitor (C_f) /nF	---	---	---	---	---	0.44	---	0.6
Input voltage (V_{IN}) /V	1.2	1	1.2	1.6-2	1.2-2	3.3	1-2.7	1-1.2
Output voltage (V_{OUT}) /V	0.9	0.5-0.8	0.45-1.05	2.5-4	3-5	5-6	3.2	1.5-2
Peak efficiency /% (@mW)	84.7@200.3	76.1@105	71@40	63@80	64@180	83.5@79.5	77.4@103	75.2@97.5
Load current (i_{Load}) /mA	3-370	40-180	5-70	6.25-60	10-84	1-25	6-65	4-80
Load transient step (Δi_{Load}) /mA	10-100	90-180	5-65	---	40	1.6-21.6	6-40	4-60
Δi_{Load} per load transient rising/falling time (mA/ns)	0.09/0.09	---	750/750	---	---	---	34/34	112*/112*
V_{OUT} under/overshoot /mV	38/25	32.4/39.6	110/-	---	170/220	1200/400	192/130	245/205
Settling time /ns	-/-	2000/2000	80/-	---	800/1070	300/750	650/650	146/140
Settling time per Δi_{Load} under/over (ns/mA)	-/-	22.2/22.2	1.3/-	---	20/26.8	15/40.8	19.1/19.1	2.6/2.5
Voltage ripple /mV	<30	14.6	84	200	200	32	21 (Extra LC filter)	160
Chip size /mm^2	2.25	0.65	1.19	2.25	0.55	3.24 (With I/O)	0.52	0.93

*: represent post layout simulation result.



(a) (b)

Fig. 16. Load transient response of the proposed KY converter under DCM operation at: (a) $V_{OUT} = 1.5$ V and (b) $V_{OUT} = 1.8$ V.

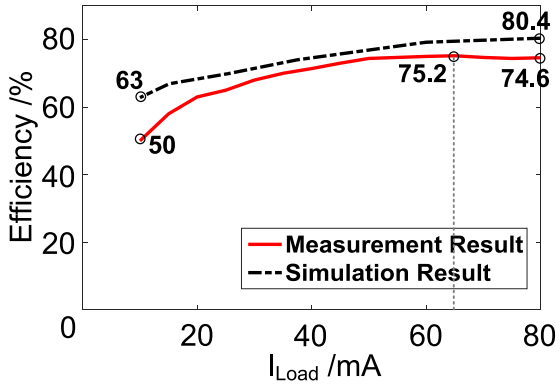


Fig. 17. Simulation and measurement results of power efficiency with DCM control under $V_{IN} = 1.2$ V and $V_{OUT} = 1.5$ V.

enhancement loop. Considering system stability, L_1 should be much slower than the PWM voltage-mode (VM) loop. And the purpose of L_2 is for transient enhancement under the load transient. When load changes, the PWM voltage-mode loop in Fig. 7 will respond and L_2 follows this duty ratio change as well. That means the duty ratio information (V_m) generated by the VM loop is added onto the EA output voltage of the ZCD (V_{ZCD}) with the help of an analog adder. The bandwidth of the analog adder should be larger than the VM loop to catch up the duty ratio change [2].

In the output logic block, V_{mix} compares the ramp signal to determine the on-time of State 2. V_{G2} and V_{G2D} are generated and V_{G2D} is longer than V_{G2} by a ZCD sampling window time (~200 ps) which has been discussed in Fig. 12.

The differences between the ZCD and the DCM calibration loop control strategy of this work and [2] are summarized in Table I.

IV. EXPERIMENTAL RESULTS

The proposed fully integrated KY step-up converter utilizing bondwire as power inductor has been fabricated with standard 65-nm CMOS technology. The total chip area is 0.93 mm^2 including a 4 nF input decoupling capacitor and 1 nF output filter capacitor as exhibited in Fig. 14.

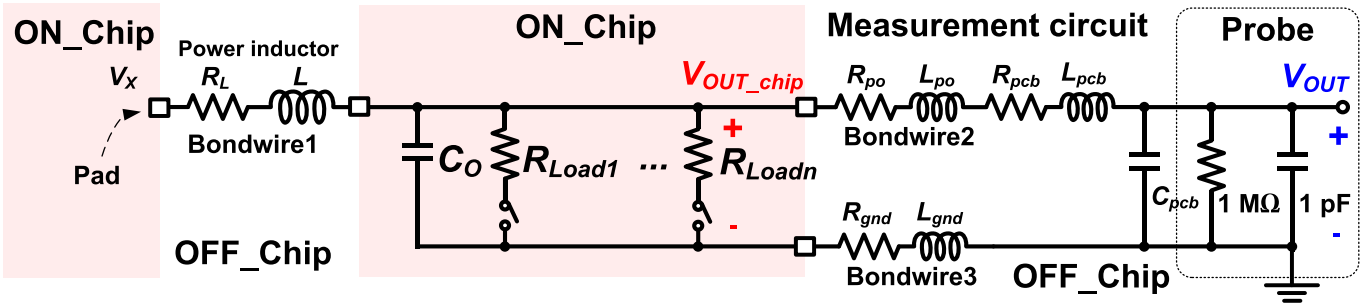


Fig. 18. Equivalent circuit of the KY converter measurement setup.

The input voltage is 1.2 V and the output voltage varies from 1.5 V to 2 V. The load current ranges from 5 mA to 80 mA. Fig. 15(a) shows that the peak efficiency is 75.2 %@V_{OUT} = 1.5 V, I_{Load} = 65 mA. Fig. 15(b) provides the post layout simulation power distribution graph of the KY converter under V_{IN} = 1.2 V, V_{OUT} = 1.8 V and I_{Load} = 10-40 mA, which includes: output power, conduction loss, switching loss, control loss, reverse current related and other losses. From Fig. 15(b), during heavy load situation, the conduction loss dominates the whole power loss of the KY converter. As the load current decreases, the switching loss percentage increases.

Fig. 16 shows the load transient response. Fig. 16(a) shows a load step from 4 mA to 60 mA at V_{OUT} = 1.5 V. The overshoot is 205 mV with 140 ns settling time, and the undershoot is 245 mV with 146 ns settling time, respectively. Fig. 16(b) shows a load step from 4 mA to 40 mA at V_{OUT} = 1.8 V. The overshoot is 200 mV with 200 ns settling time, and the undershoot is 145 mV with 166 ns settling time, respectively. To show a fast transient response, the rising/falling time of the load current transient is just 500 ps.

Fig. 17 illustrates the simulated and measured power efficiency with DCM calibration loop under V_{IN} = 1.2 V and V_{OUT} = 1.5 V. The measured efficiency at I_{Load} = 10 mA and 80 mA are 50% and 74.6%, respectively, while the peak efficiency is 75.2% at I_{Load} = 65 mA. For the efficiency loss issue, one possibility reason should be the parasitics. As an example, the parasitic capacitance and resistance in node V_X can affect the power switches non-overlap time, which can significantly degrade the power efficiency. Even though this problem cannot be resolved by the proposed DCM calibration loop, it can be much alleviated with a non-overlap time calibration circuit similar to [16] and [17].

The measured maximum voltage ripple is 160 mV. Since we measured it with the oscilloscope probe (Keysight N2795A active probe) on a PCB, the output bondwire and PCB trace loading between the on-chip output voltage point (V_{OUT_chip}) and the probe measurement output voltage point (V_{OUT}) will enlarge the output voltage ripple [18]. Fig. 18 shows the equivalent circuit of the KY converter measurement setup, with the corresponding simulation result as shown in Fig. 19. It can be concluded that the output voltage ripple is increased due to this measurement loading. However, when we apply this converter in a SoC, the output voltage ripple will be much smaller than the off-chip measurement, as shown in Fig. 19. The above analysis holds for over/undershoot voltage during load transient response as well.

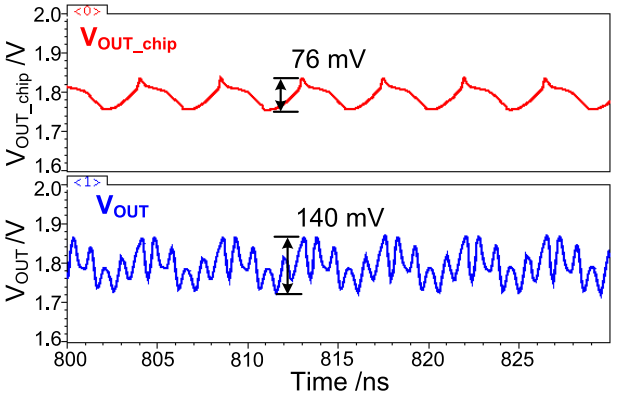


Fig. 19. Simulated on-chip output voltage V_{OUT_chip} and off-chip output voltage V_{OUT} under V_{IN} = 1.2 V,V_{OUT} = 1.8 V,I_{Load} = 40 mA.

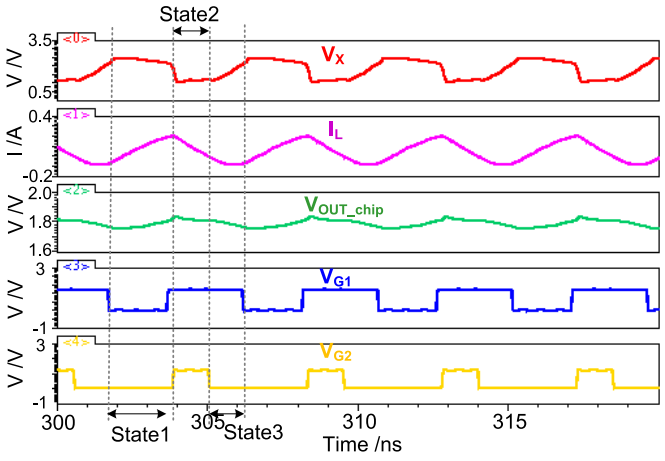


Fig. 20. The simulated V_X, I_L, V_{OUT_chip}, V_{G1} and V_{G2} waveforms of the proposed KY converter.

Fig. 20 shows the simulation waveforms of V_X, I_L, V_{OUT}, V_{G1} and V_{G2} under V_{IN} = 1.2 V, V_{OUT} = 1.8 V, I_{Load} = 40 mA. In State 1, the flying capacitor is discharged and inductor is magnetized, V_X is charged up to $2V_{IN}$-ΔV_{Cf} first and then decreases. In State 2, flying capacitor is charged and inductor is demagnetized, V_X is around V_{IN}. In State 3, all the power switches turn off and V_X is a floating voltage.

Table II shows the comparison with prior works of high frequency ($f_s \geq 80$ MHz) DC-DC converters. Among the state-of-the-art fully integrated buck converter using either bondwire and planar inductors [2], [19], [20], this work achieves fast transient response at sub-μ s level similar to [20] while achieving comparable power efficiency. Comparing this work with the state-of-the-art inductive and SC-based boost converters [21], [22], [24], the settling time per load transient step of this work is competitive. Comparing this work with the SC-based boost converter [23], the chip size is smaller.

V. Conclusion

A PWM fully integrated KY converter utilizing bondwire inductance as power inductor under DCM operation was proposed, and implemented in standard 65-nm CMOS. This work is the first DCM closed-loop controller design for the KY converter, which obtains faster load transient response when compared with state-of-the-art boost converters. This advantage is related to the characteristics of the KY converter topology and its transient enhancement circuitry within the DCM calibration loop. This paper presented the details of its parameter design, the DCM closed-loop voltage-mode controller design to obtain a fast and stable control loop, a ZCD method to activate the DCM control, and a DCM calibration loop to reduce the reversion loss, relax the accuracy requirement of bonding wire inductance, as well as enhance the load transient response performance. Measurement results have shown that with a switching frequency of 220 MHz, the designed KY converter achieves a peak efficiency of 75.2%@97.5 mW from $V_{IN} = 1.2$ V, $V_{OUT} = 1.5$ V and $I_{Load} = 65$ mA, and a load transient response of 245 mV/205 mV undershoot/ overshoot at 146/140ns recovery time. This work achieved a settling time per load transient step of 2.6 ns/mA, which is competitive with the state-of-the-art boost converters.

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Wen-Liang Zeng (S'18) received the B.Sc. and M.Sc. degrees in electrical and computer engineering from the University of Macau, Macau, China, in 2014 and 2016, respectively, where he is currently pursuing the Ph.D. degree in electrical and computer engineering. His research focuses on high-speed fully integrated dc–dc converters and ultra-low quiescent current integrated dc–dc converters.

Mr. Zeng was a recipient of the Macao Science and Technology Research and Development Award for Postgraduates (Master Level) in 2016.

Chi-Seng Lam (S'04–M'12–SM'16) received the B.Sc., M.Sc., and Ph.D. degrees in electrical and electronics engineering from the University of Macau (UM), Macau, China, in 2003, 2006, and 2012, respectively.

From 2006 to 2009, he was an E&M Engineer with UM. In 2009, he simultaneously worked as a Laboratory Technician and started to pursue the Ph.D. degree, and completed the Ph.D. degree within three years. In 2013, he joined The Hong Kong Polytechnic University, Hong Kong, as a Post-Doctoral Fellow. He is currently an Assistant Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, UM. He has co-authored or co-edited four books: *Design and Control of Hybrid Active Power Filters* (Springer, 2014), *Parallel Power Electronics Filters in Three-Phase Four-Wire Systems–Principle, Control and Design* (Springer, 2016), *Tutorials in Circuits and Systems Selected Topics in Power, RF, and Mixed-Signal ICs* (River Publishers, 2017), and *Adaptive Hybrid Active Power Filters* (Springer, in press). He has authored or co-authored over 70 technical journals and conference papers. He holds four U.S. patents and two Chinese patents. His research interests include integrated power electronics controllers, power management integrated circuits, power quality compensators, smart grid technology, and renewable energy.

Dr. Lam was a recipient of the IEEE PES Chapter Outstanding Engineer Award in 2016, the Macao Science and Technology Invention Award (Third-Class) in 2014, and the Research and Development Award for Postgraduates in 2012. He was also a recipient of the Macao Government Ph.D. Research Scholarship from 2009 to 2012, the Macao Foundation Postgraduate Research Scholarship from 2003 to 2005, and the 3rd RIUPEEEC Merit Paper Award in 2005.

In 2007, 2008, and 2015, he was a GOLD Officer, a Student Branch Officer, and a Secretary of the IEEE Macau Section. He is currently the Vice-Chair of the IEEE Macau Section, the Chair of the IEEE CAS Macau Chapter, and a Secretary of the IEEE PES/PELS Joint Macau Chapter. He served as a member for the Organizing Committee or the Technical Program Committee of several international conferences.

Franco Maloberti (M'84–SM'87–F'96–LF'16) received the Laurea degree in physics (*summa cum laude*) from the University of Parma, Italy, and the Dr. Honoris Causa degree in electronics from Inaoe, Puebla, Mexico. He was a Visiting Professor with ETH-PEL, Zurich, and EPFL-LEG, Lausanne. He was the TI/J. Kilby Analog Engineering Chair Professor with Texas A&M University and the Distinguished Microelectronic Chair Professor with The University of Texas at Dallas. He is currently an Emeritus Professor with the University of Pavia, Italy. He is also an Honorary Professor with the University of Macau, China. He has authored over 550 published papers and seven books and holds 33 patents. His professional expertise is in the design, analysis, and characterization of integrated circuits and analog digital applications, mainly in the areas of switched capacitor circuits, data converters, interfaces for telecommunication and sensor systems, and CAD for analog and mixed A-D design. He is the Chairman of the Academic Committee of the Microelectronics Key Laboratory, Macau, China. He was a recipient of the 1999 IEEE CAS Society Meritorious Service Award, the 2000 CAS Society Golden Jubilee Medal, the IEEE Millenium Medal, the 1996 IEE Fleming Premium, the ESSCIRC 2007 Best Paper Award, the IEEJ Workshop 2007 and 2010 Best Paper Award, and the IEEE CAS Society 2013 Mac Van Valkenburg Award. He is the Past President of the IEEE CAS Society from 2017 to 2018 and was the President of the IEEE CAS Society from 2015 to 2016. He was a VP Region 8 of the IEEE CAS from 1995 to 1997, an Associate Editor of the IEEE-TCAS-II, the President of the IEEE Sensor Council from 2002 to 2003, an IEEE CAS BoG Member from 2003 to 2005, and a VP–Publications of the IEEE CAS from 2007 to 2008. He was a DL of the IEEE SSC Society from 2009 to 2010 and also a DL of the IEEE CAS Society from 2006 to 2007 and from 2012 to 2013.

Sai-Weng Sin (S'98–M'06–SM'13) received the B.Sc., M.Sc., and Ph.D. degrees in electrical and electronics engineering from the University of Macau, Macau, China, in 2001, 2003, and 2008, respectively. He is currently an Associate Professor with the Faculty of Science and Technology, University of Macau. He is also the Coordinator with the Data Conversion and Signal Processing Research Line in State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. He has authored one book entitled *Generalized Low-Voltage Circuit Techniques for Very High-Speed Time-Interleaved Analog-to-Digital Converters* (Springer). He has authored or co-authored over 130 technical journals and conference papers in the field of high performance data converters and analog mixed-signal integrated circuits. He holds seven U.S. patents.

Dr. Sin is/has been a member of the Technical Program Committee of the IEEE Asian Solid-State Circuits Conference, the IEEE ISCAS, the International Wireless Symposium, the IEEE Sensors, and the IEEE RFIT Conference, the Track Chair in TPC of the IEEE TENCON, a Review Committee Member of PrimeAsia, Technical Program and Organization Committee of the 2004 IEEJ AVLSI Workshop, as well as the Special Session Co-Chair and a Technical Program Committee Member of the 2008 IEEE APCCAS Conference. He co-supervised the student who got the 2015 SSCS Pre-Doctoral Achievement Award. He was a co-recipient of the 2011 ISSCC Silk Road Award, the Student Design Contest Award of the A-SSCC 2011, and the 2011 State Science and Technology Progress Award (second-class) in China. He was the Secretary of the IEEE Solid-State Circuit Society (SSCS) Macau Chapter (with the 2012 IEEE SSCS Outstanding Chapter Award) and the IEEE CAS/COM Joint Macau Chapter (with the 2009 IEEE CAS Chapter of the Year Award).

Man-Chung Wong (SM'06) received the B.Sc. and M.Sc. degrees in electrical and electronics engineering from the University of Macau (UM), Macau, China, in 1993 and 1997, respectively, and the Ph.D. degree in electrical engineering from Tsinghua University, Beijing, China, in 2003.

He was a Visiting Fellow with Cambridge University, U.K., in 2014. An industrial power filter platform was developed and installed in a practical power system based on his research results. He is currently an Associate Professor with the Department of Electrical and Computer Engineering, UM. He has co-authored four books (Springer) and over 100 journal and conference papers. He holds 10 Chinese and U.S. patents. His research interests are power electronics converters, pulse width modulation, active power filters, hybrid active power filters, and hybrid power quality compensator for high-speed railway power supply system.

Dr. Wong received the Macao Young Scientific Award from the Macau International Research Institute in 2000 and the Young Scholar Award from UM in 2001. He was a recipient of the Second Prize for Tsinghua University Excellent Ph.D. Thesis Award in 2003 and the Macao Science and Technology Invention Award (Third-Class) in 2012 and 2014, respectively. He supervised several students to receive merit paper awards in conferences and champions in student project competitions.

Dr. Wong was a member of several conference committees. He was the General Chair of the IEEE TENCON 2015, Macau. He is with the IEEE Macau Section and the IEEE Macau Power Joint Chapter for many years. From 2014 to 2015, he was the Chair of the IEEE Macau Section. He is currently the North Representative of the IEEE Region 10 Power and Energy Society and the Chair of the IEEE Macau PES/PELS Joint Chapter.

Rui Paulo Martins (M'88–SM'99–F'08) was born in 1957. He received the bachelor's, master's, and Ph.D. degrees and the Habilitation for Full-Professor degree in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively. He has been with the Department of Electrical and Computer Engineering /IST, TU of Lisbon (from 2013 as the University of Lisbon), since 1980.

Since 1992, he has been on leave from IST, University of Lisbon, and is also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macau, China, where he has been a Chair Professor since 2013. He was the Dean of the FST, UM, from 1994 to 1997 and he has been a Vice-Rector of UM since 1997. Since 2008, after the reform of the UM Charter, he was nominated after open international recruitment, and reappointed in 2013, as a Vice-Rector (Research) until 2018. He was a Co-Founder of Chipidea Microelectronics, Macau, (now Synopsys, Macau), in 2001/2002, and in 2003, he created the Analog and Mixed-Signal VLSI Research Laboratory, UM, elevated in 2011 to the State Key Laboratory of China (the first in Engineering in Macau), being its Founding Director. Within the scope of his teaching and research activities, he has taught 21 bachelor and master courses, and in UM, he has supervised (or co-supervised) 45 theses, Ph.D. (24), and masters (21). He has co-authored seven books and 11 book chapters, 442 papers in scientific journals (141) and in conference proceedings (301), as well as other 64 academic works, in a total of 554 publications. He holds 30 patents [U.S. (28) and Taiwan (2)].

Dr. Martins was the Founding Chairman of the IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications from 2005 to 2008 [2009 World Chapter of the Year of IEEE CAS Society (CASS)]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on CAS—APCCAS 2008 and the Vice-President for Region 10 (Asia, Australia, and the Pacific) of the IEEE CASS from 2009 to 2011. He was the Vice-President (World) Regional Activities and Membership of the IEEE CASS from 2012 to 2013 and an Associate Editor of the IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS from 2010 to 2013. He was a nominated Best Associate Editor of T-CAS II from 2012 to 2013. He has been a member of the IEEE CASS Fellow Evaluation Committee in 2013, 2014, and 2019, and a CAS Society Representative in the nominating committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)–the Director of the IEEE. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference—ASP-DAC 2016 and received the IEEE Council on Electronic Design Automation Outstanding Service Award in 2016. He was a Nominations Committee Member of the IEEE CASS from 2016 to 2017 and the Chair of the IEEE CASS Fellow Evaluation Committee (Class 2018). In representation of UM, he was one of the vice-presidents during 2005–2014 and the President during 2014–2017 of the Association of Portuguese Speaking Universities. He was a recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999 and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In 2010, he was elected, unanimously, as a Corresponding Member of the Portuguese Academy of Sciences, Lisbon, being the only Portuguese academician living in Asia.