A 0.0018-mm^2 153% Locking-Range CML-Based Divider-by-2 With Tunable Self-Resonant Frequency Using an Auxiliary Negative-g_m Cell

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***Abstract*— This paper presents an area-efficient current-mode-logic (CML)-based divider, with a tunable self-resonant frequency for locking range (LR) extension. Specifically, a negative-g_m (NG) cell is inserted between the resonated shunt-peaking inductor and the load resistor to shift the divider's sensitivity curve (SC), enabling concurrently a higher operating frequency and a wider LR. We also use the injection-locking concept, together with a graphical phasor diagram with the frequency-phase information, to systematically explain the LR-extension mechanism. Prototyped in a 65-nm CMOS, the divider occupies a tiny active area of 0.0018 mm^2. The measured LR is 153% (4–30 GHz) while consuming 4.06–4.28 mW at 30 GHz under a single 1.2-V supply. The performance corresponds to two figure of merits: FOM$_{Pdc}$ of 25.5 dB and FOM$_P$ of 71.5, both compare favorably with the state of the art.**

***Index Terms*— CMOS, self-resonant frequency (f_{SR}), injection locking, sensitivity curve (SC), shunt peaking, 5G New Radio, current-mode-logic (CML), phasor diagram, negative-g_m (NG), divider-by-2, locking range (LR), latch.**

I. Introduction

HIGH-PERFORMANCE RF-to-mmWave frequency dividers are the cornerstone of advanced local-oscillator generator for the coming fifth-generation (5G) New Radio [1], [2], and clock synchronization in the wireline [3] and optical [4] transceivers. All of them pose serious design challenges as wider tunability and locking range (LR) are required together with smaller area and power budget. The injection-locked frequency divider (ILFD) [5]–[10] is popular for its high-frequency operation at low power, but the LR is very limited. Distributed-high-order resonators can aid extending the LR [7], [8], but significantly penalizing the chip area. The dynamic-latch-based divider [11] can achieve a broader LR via a tunable load. Yet, its LR and operating frequency are sensitive to the process, voltage and temperature (PVT) variations. The current-mode-logic (CML) dividers [12]–[16] are another promising alternative for their wide LR and small footprint. Yet, their operating frequencies are often limited by the parasitic effect, and their static power is high to achieve a high operating frequency. To surmount those tradeoffs, techniques for bandwidth (BW) extension such as inductive peaking [12], split loading [13] and LC-tank loading [14], [15] have been studied. In [17], a tunable grounded active inductor (GAI) was used for tunable BW extension, but it was applied to the wideband amplifier only. The cross-coupled pair, which can provide a negative g_m (NG) has been widely used in mixers to provide a proper load [18]–[21]. Extending the concept, this paper employs the NG cell to extend the operating range of the CML-based divider via tuning the self-resonant frequency (f_{SR}) while not compromising the die area, power and sensitivity issues. To optimize our divider's performance with balanced power and area, a graphical-aided methodology is developed based on the injection-locking concept [22]–[24] to systematically analyze the self-resonant frequency.

This paper is organized as follows. Section II introduces the proposed divider-by-2 and the graphical analysis based on the injection-locking concept. Section III discusses the self-resonant frequency of the CML divider with three types of load tanks. Subsequently, Section IV details the simulation of our design. Section V presents the measurement results. Finally, the key contributions of this work are summarized in Section VI.

II. Proposed Divider and Its Graphical Analysis

Illustrated in Fig. 1(a), the proposed divider-by-2 consists of two identical latches arranged in a feedback loop, and driven

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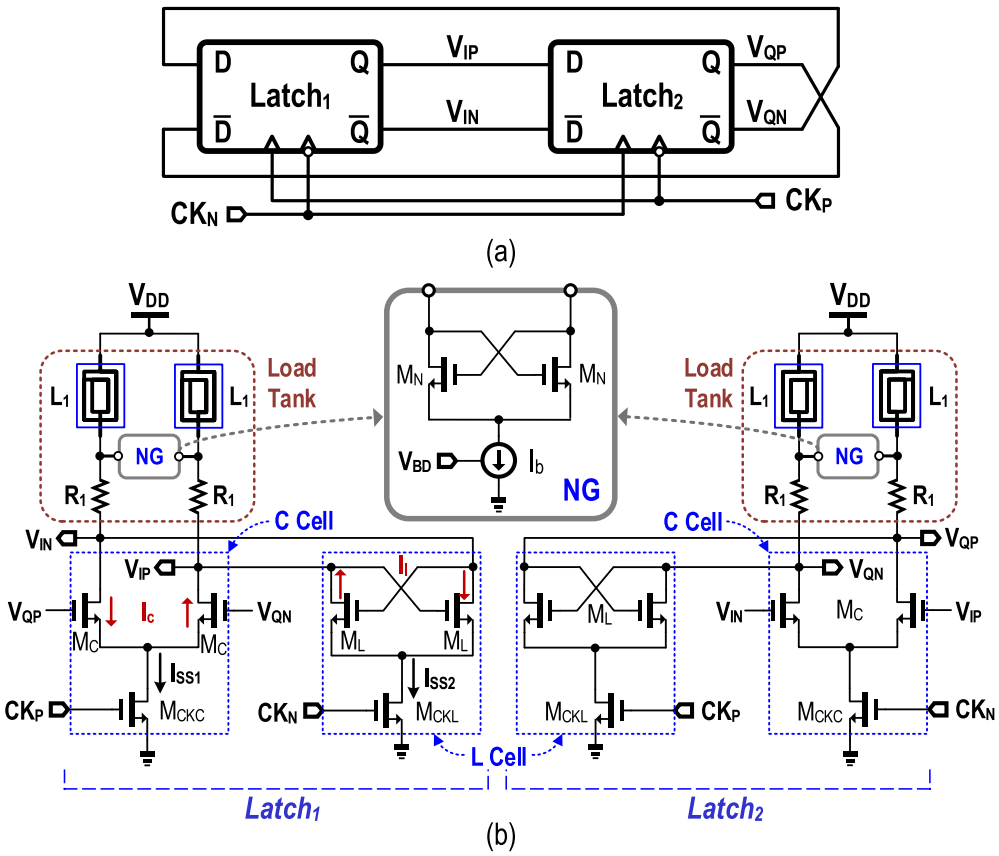

Fig. 1. (a) Two latches view and (b) detailed schematic of our proposed CML-based frequency divider-by-2.

by two complementary clocks, i.e., CK_P and CK_N. Fig. 1(b) shows its detailed schematic. Each latch is comprised of a coupling pair (C cell), a cross-coupled latch pair (L cell) and a resonant load tank [Fig. 1(b)]. Apart from the load resistor (R_1) and parasitic capacitor at the output nodes, shunt-peaking inductors (L_1) are introduced to enhance the operating frequency. Besides, a negative-g_m (NG) cell is inserted between L_1 and R_1, which provides extra tunability for f_{SR}.

Although there is no absolute phase relationship between the two outputs of the latch, it will be useful to make a remark about the notations, for the analysis to be presented later. The two outputs of the divider are in quadrature phase with each other. Note that the signal which holds a leading phase is denoted as in-phase (I) output, and the other one is denoted as the quadrature (Q) output.

To clearly develop the theoretical analysis on f_{SR}, the C cell and L cell [Fig. 1(b)] can be viewed as two single-balanced active mixers [15], [16]. The tail transistors (M_{CKC}, M_{CKL}) operate as the voltage-to-current (V/I) converters which transform the differential clock voltages to the currents (I_{SS1}, I_{SS2}). Thereafter, the mixer transistors (M_C, M_L) steer the tail currents by their input signals. Finally, the load tank converts the total current (I_t) summed from M_C and M_L to the output voltages.

Fig. 2(a) depicts the phasor diagram of the currents in a CML latch. To simplify our analysis, we define the initial phase of I output (V_{IP}) is 0°. Additionally, we denote $I_{ca}(t)$ and

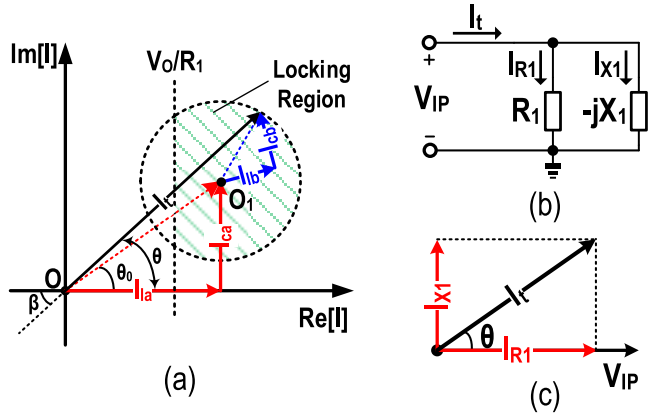

Fig. 2. (a) Phasor diagram of the currents in a CML latch. (b) Illustration for a general load tank. (c) Phasor for (b).

$I_{la}(t)$ as the currents mixed by the dc components (I_{DC}) of tail currents, e.g., currents of M_{CKC} and M_{CKL} in Fig.1 (b), and the feedback output signals in the C cell and L cell, respectively. While $I_{cb}(t)$ and $I_{lb}(t)$ are the mixed currents from the ac part (I_{ac}) of tail currents and feedback output signals. Referring to the behavior model in [15], [16], $\overrightarrow{I_{ca}}$ and $\overrightarrow{I_{cb}}$ always lead $\overrightarrow{I_{la}}$ and $\overrightarrow{I_{lb}}$ by a phase of $\pi/2$, respectively. Without the clock injection, both $\overrightarrow{I_{cb}}$ and $\overrightarrow{I_{lb}}$ are nullified. Hence, the total current $\overrightarrow{I_t}$ flowing through the tank equals the sum of $\overrightarrow{I_{ca}}$ and $\overrightarrow{I_{la}}$, which is related to f_{SR} of the divider. As the amplitude of the

clock signals (V_{QP} and V_{QN}) increases, $\overrightarrow{I_{cb}}$ and $\overrightarrow{I_{lb}}$ enlarge as well. Since the phase (φ_{in}) of input clock ranges from 0 to 2π arbitrarily and consider that the end of the $\overrightarrow{I_{ca}} + \overrightarrow{I_{la}}$ always locates at point "O_1". Obviously, the trajectory of $\overrightarrow{I_t}$ exhibits a circle, whose radius equals $\left|\overrightarrow{I_{cb}} + \overrightarrow{I_{lb}}\right|$, and the angle θ depends on φ_{in}. Note that a general load tank consists of a resistor in parallel with a negative reactance shown in Fig. 2(b). The current phasors (I_{R1} and I_{X1}) are perpendicular with each other, forming the total current (I_t), which leads V_{IP} by θ, as illustrated in Fig. 2(c). This relationship will be instantiated in Section III later.

Considering the divider as an injection-locking oscillator which operates at one-half of the input frequency, the Barkhausen criterion should be satisfied to sustain the oscillation, i.e., the gain criterion $\mathrm{Re}[I_t(\omega)]R_1 \geq V_O$ and the phase criterion $\theta + \beta = 0$, where V_O is the amplitude of V_{IP}, θ is phase between I_t and V_{IP}, and β is the phase shift introduced by the load tank. The phase criterion implies that the phase of $\overrightarrow{I_t}$ must be compensated by that of the load tank when the divider operates normally.

III. f_{SR} in CML Divider With Different Load Tanks

Particularly, f_{SR} represents the most critical point on the sensitivity curve (SC) and indicates the operating speed of the divider. To clearly demonstrate our divider with a larger LR and a higher f_{SR}, the theoretical analysis focusing on f_{SR} will be developed for the CML divider with three different load tanks.

A. Conventional RC Tank

In the conventional CML divider, $\beta_{tank1} = -\arctan(\omega R_1 C_1)$, thus f_{SR} can be expressed as

$$f_{SR} = \frac{\tan(-\beta)}{2\pi R_1 C_1} = \frac{\tan(\theta_0)}{2\pi R_1 C_1} = \frac{\left|\overrightarrow{I_{ca}}\right| / |\overrightarrow{I_{la}}|}{2\pi R_1 C_1} \quad (1)$$

where θ_0 is the angle between $\overrightarrow{I_{ca}} + \overrightarrow{I_{la}}$ and $\overrightarrow{I_{la}}$ in Fig. 2(a) and C_1 denotes the output-to-ground-node parasitic capacitors, i.e., the parasitic capacitors at V_{IP}, V_{IN}, V_{QP}, and V_{QN}, can be viewed as X_1 in Fig. 2(b). With a fixed tank, f_{SR} can be changed by tuning the ratio of $\left|\overrightarrow{I_{ca}}\right|$ to $\left|\overrightarrow{I_{la}}\right|$, which can be changed easily by varying the size of tail transistors M_{CKC} and M_{CKL}. Fig. 3 shows the simulated and calculated f_{SR} based on (1). As the width of M_{CKL} increases, the ratio of $\left|\overrightarrow{I_{ca}}\right| / |\overrightarrow{I_{la}}|$ decreases, meanwhile resulting in lower f_{SR}. Inversely, increasing the width of M_{CKC} leads to a higher f_{SR}.

B. RLC Tank

With a shunt-peaking inductor, the load tank of the divider and its phasor diagram are depicted in Fig. 4(a) and (b), respectively. According to the mixer model, we observe that both $I_c(t)$ and $I_l(t)$ keep constant. Thus, the phasor of $I_t(t)$ keeps unchanged, which is the same as that in the RC tank. Yet, as L_1 increases, R_1+L_1 exhibits more inductive impedance,

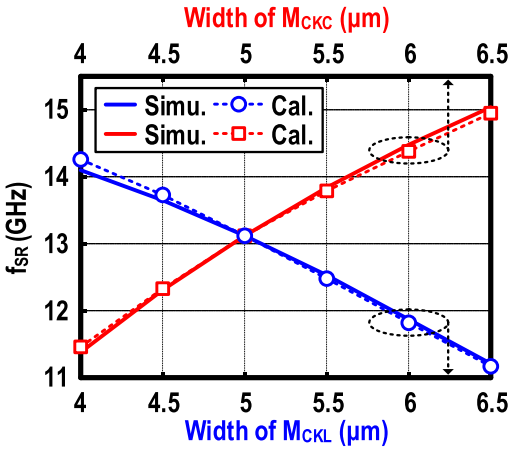

Fig. 3. Simulated (*solid*) and calculated (*dash*) f_{SR} across the width of M_{CKC} (*red*) and M_{CKL} (*blue*).

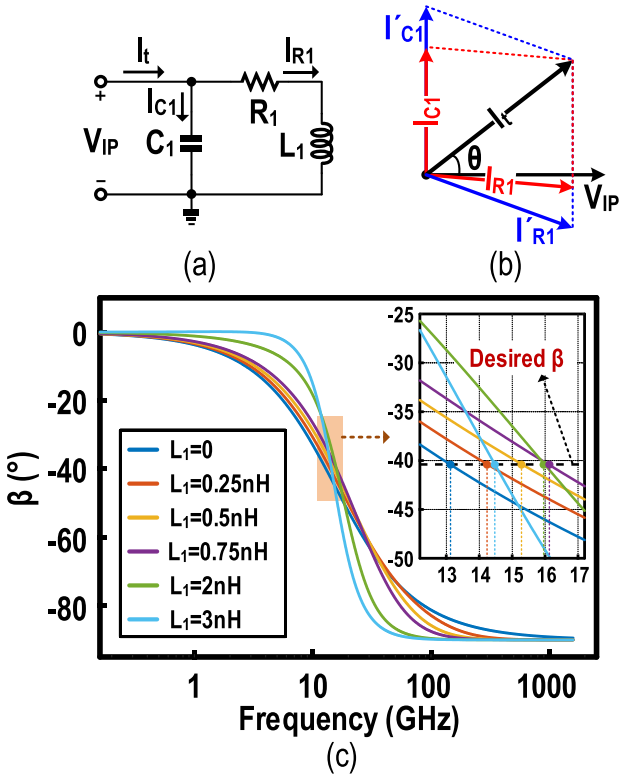

Fig. 4. (a) Load tank with shunt-peaking inductor. (b) Phasor of currents and voltage in (a). (c) Phase response of the load tank in (a) when varying L_1, where $R_1 = 281.8\ \Omega$ and $C_1 = 36.63$ fF.

indicating that the angle between $\overrightarrow{I_{R1}}$ and $\overrightarrow{V_{IP}}$ becomes larger. To maintain a constant θ for $\overrightarrow{I_t}$, the amplitudes of I_{C1} and I_{R1} increase (from I_{C1},I_{R1} to I'_{C1},I'_{R1}, respectively), implying a larger current to charge the capacitor, as shown in Fig. 4(b). The impedance and phase shift of the RLC tank can be expressed as (2) and (3), respectively,

$$Z_{tank2}(j\omega) = \frac{R_1 + j\omega L_1}{1 + j\omega R_1 C_1 - \omega^2 L_1 C_1} \quad (2)$$

$$\beta_{tank2} = \arctan\left(\frac{\omega L_1}{R_1}\right) - \arctan\left(\frac{\omega R_1 C_1}{1 - \omega^2 L_1 C_1}\right) \quad (3)$$

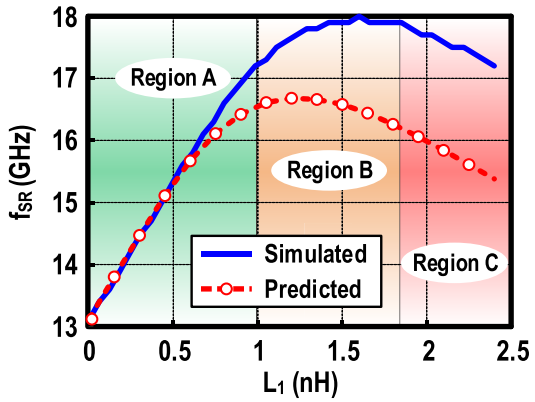

Fig. 5. Simulated and predicted f_{SR} across the inductance of shunt-peaking inductor. Note that the simulation result is based on the pre-layout netlist with an ideal inductor.

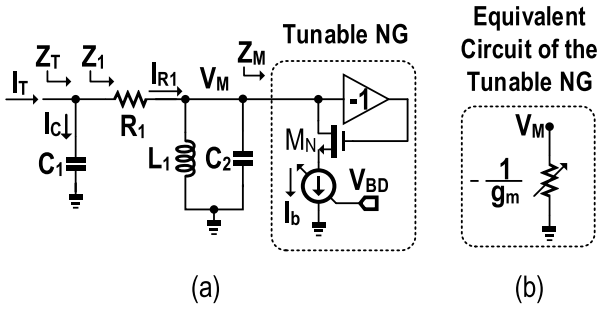

Fig. 6. Simplified schematic of the proposed load tank with a tunable NG. (b) Single-ended equivalent circuit for the NG.

Fig. 4(c) shows the phase shift of the load tank with different inductances. Assuming $\omega^2 L_1 C_1 \ll 1$, we can obtain,

$$\beta_{tank2} \approx \arctan\left(\frac{\omega L_1}{R_1}\right) - \arctan\left(\omega R_1 C_1\right) = \arctan\left(\frac{\omega L_1}{R_1}\right) - \beta_{tank1} \quad (4)$$

Note that the second term in (4) is the phase shift of the conventional RC tank. Thus, the additional phase introduced by L_1 is $\arctan(\omega L_1/R_1)$, which can be approximated as $\omega L_1/R_1$ when L_1 is small enough, namely a linear function of L_1. The close-up view in Fig. 4(c) shows the linear relationship between the phase shift and the small inductance below 0.75 nH.

Referring to the phase criterion and the phase shift in (3), we obtain the simulated and predicted f_{SR} versus the optimal the value of L_1, as shown in Fig. 5. Noted that the desired β in Fig. 4(c) for calculation is equal to θ_0 in Fig. 2(a) and is acquired by extracting current I_{la} and I_{ca} based on the simulation. The f_{SR} increases linearly in *Region A* when $L_1 < 1$ nH. Yet, as L_1 increases, the second term in (3) cannot be approximated as β_{tank1} anymore, and it is an increasing function of L_1. As a result, the increment of β_{tank2} in *Region B* is smaller than that in *Region A* for the same increment of L_1, leading to the f_{SR} saturation in *Region B*. Under larger inductance, the second term dominates (3), thus f_{SR} shows an inverse correlation with L_1 in *Region C*. Considering the area efficiency, we choose the inductance in *Region A*.

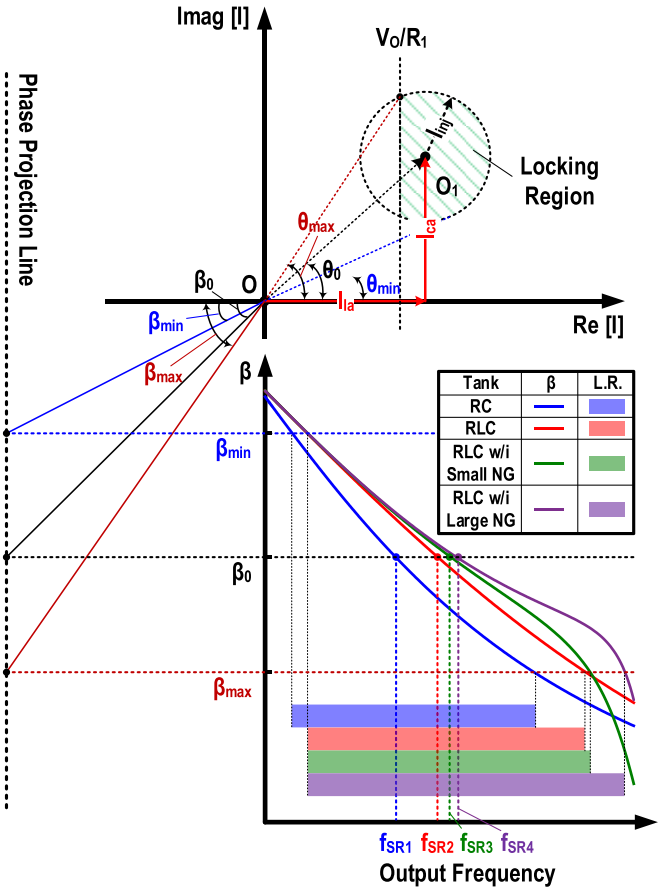

Fig. 7. Proposed phasor diagram involving the link between phase shift and LR with frequency information of different load tanks.

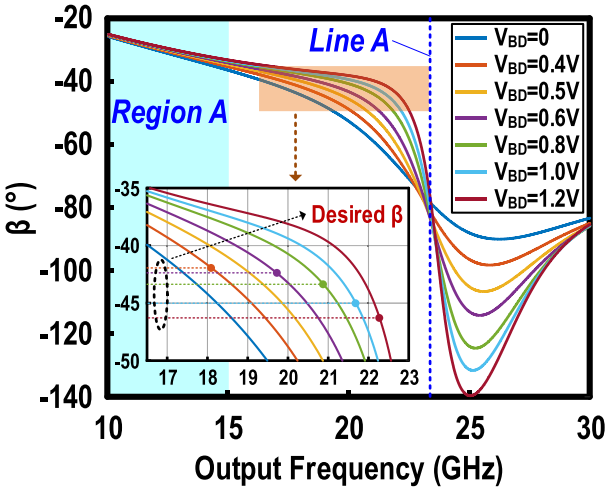

Fig. 8. Phase shift of Z_{tank3} for different V_{BD}, where $R_1 = 281.8\ \Omega$, $C_1 = 36.63$ fF, $L_1 = 735$ pH and $C_2 = 50$ fF.

C. Proposed Load Tank

The rearranged schematic of the proposed load tank is shown in Fig. 6(a), where C_1 and C_2 are the parasitic capacitance at the output and middle (V_M) nodes, respectively. In the small-signal analysis, the NG cell can be viewed as a transistor whose output inversely drives its input, along with a tunable tail current (I_b). As shown in Fig. 6(b), Z_M is equivalent to

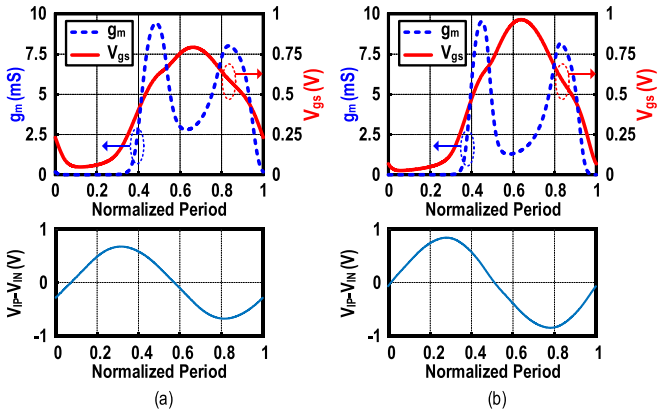

Fig. 9. Periodic waveforms of V_{gs} and g_m of the NG cell and the divider output (V_{IP}– V_{IN}) when V_{BD} = 0.9 V (a) without clock signal input (b) under 0.5-V_{pp} CK swing.

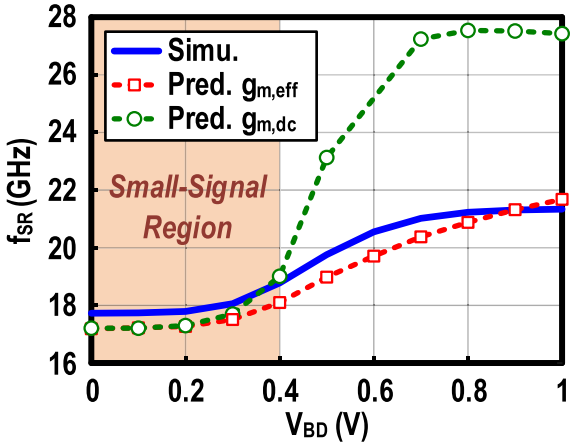

Fig. 10. Simulated and predicted f_{SR} across V_{BD} based on (6) with $g_{m,dc}$ and $g_{m,eff}$, respectively.

a tunable negative-g_m controlled by V_{BD}, which implies an extra ac current to charge the tank capacitors for improving its high-frequency operation [17]. The total impedance of the proposed load tank is given by

$$Z_{tank3}(s) = \frac{L_1C_2R_1s^2 + L_1\left(1 - g_mR_1\right)s + R_1}{D_3s^3 + D_2s^2 + D_1s + 1} \tag{5}$$

where $D_3 = L_1C_1C_2R_1$, $D_2 = L_1C_1(1\text{-}g_mR_1)+L_1C_2$ and $D_1 = R_1C_1\text{-}g_mL_1$. Thus, the corresponding phase shift is expressed as

$$\beta_{tank3}(\omega) = \arctan\left[\frac{L_1\omega\left(1 - g_mR_1\right)}{R_1 - L_1C_2R_1\omega^2}\right] - \arctan\left\{\frac{\omega\left[\left(R_1C_1 - g_mL_1\right) - L_1C_1C_2R_1\omega^2\right]}{1 - \left[L_1C_1\left(1 - g_mR_1\right) + L_1C_2\right]\omega^2}\right\} \tag{6}$$

To obtain the intuitive insight into how the divider benefits from the tank evolution with additional NG cell, an extended phasor diagram is developed in Fig. 7. Assuming that the output swing of V_O and R_1 keep constant and considering that $\overrightarrow{I_{ca}}$ always leads $\overrightarrow{I_{la}}$ by a phase of $\pi/2$ from Section II. Thus, $\overrightarrow{I_{ca}}$ and $\overrightarrow{I_{la}}$ keep unchanged. Without the loss of generality,

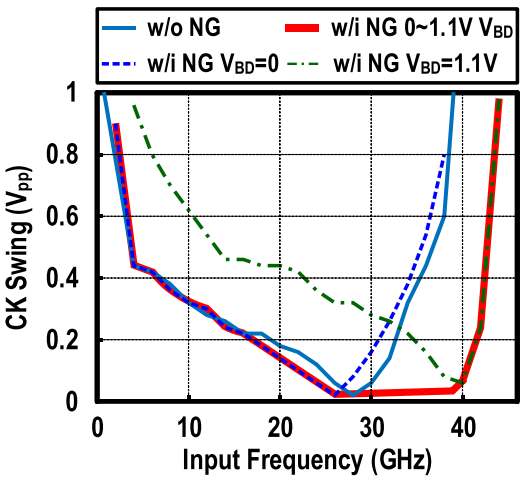

Fig. 11. The SCs comparison with and without the proposed NG cell. Note that the results are obtained by pre-layout netlist with the S-parameter for L_1, when $V_{CK,CM}$ = 0.5 V,V_{DD} = 1.2 V.

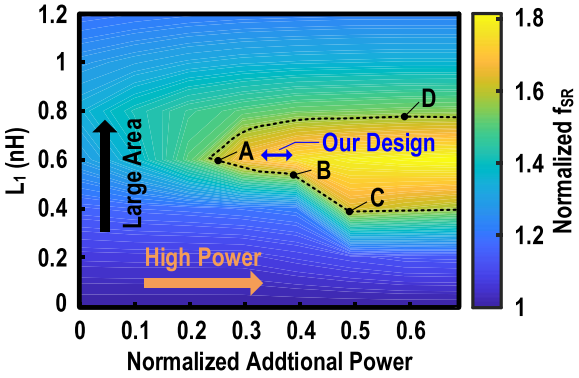

Fig. 12. Contour of normalized f_{SR} versus normalized additional power and shunt-peaking inductance in the proposed load tank.

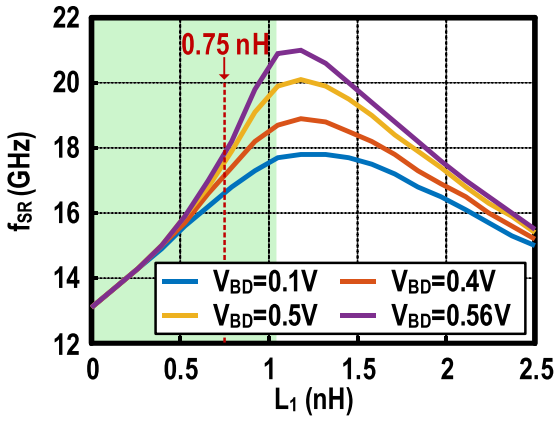

Fig. 13. Simulated f_{SR} across the value of L_1 under different V_{BD}.

Fig. 7 (*upper*) shows the locking condition which is limited by both the amplitude and phase cases [16]. The phase shift can be projected on a vertical line, where the intercepts represent the magnitudes of β.

In the conventional phasor diagram, there is an almost total lack of the frequency-phase information. To reveal the

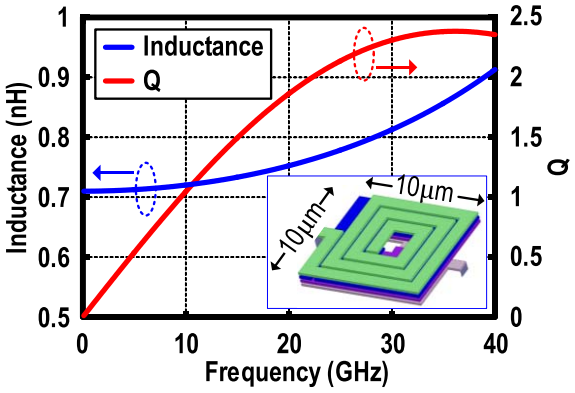

Fig. 14. Ultra-compact inductor details.

effect of the tank evolution, an additional phase profile can be appended in the proposed phasor diagram to show the variations of both f_{SR} and LR. Fig. 7 (*lower*) sketches the phase shift for four different tanks, on the horizontal line of $\beta = \beta_{min}$, the intersections for the RLC tank with and without the NG cell are almost coincident, indicating a similar lower limit operating frequency. Differently, assuming $\beta = \beta_{max}$, the shunt-peaking inductor and NG cell extend the upper limit to a higher frequency, especially for a larger NG. The intersections of $\beta = \beta_0$ exhibits an increment of f_{SR} when shunt-peaking inductor and NG cell are added sequentially.

In practice, when the tank components (e.g., L_1 and NG) vary, phasors in the divider change as well due to the parasitics. Therefore, the parameter extraction based on the simulation is required for more accurate analysis. Fig. 8 shows a practical phase profile based on (6) under different V_{BD}. On the left side of *Line A*, the larger V_{BD}, the less β the tank provides at a specific frequency, indicating a higher f_{SR} to obtain the desired β. However, this tendency reverses on the right side of *Line A*.

Before determining f_{SR}, it is instructive to discuss g_m in (5) and (6). In the conventional small-signal model, it proves valid to use the operation-point transconductance for circuit analysis. However, as the divider outputs a considerable rail-to-rail swing, the NG cell also experiences a large-signal operating behavior. Fig. 9 shows the time-variant g_m and V_{gs} waveforms of the cross-coupled transistor in the NG cell and differential output of the divider across one period. Obviously, whether the divider operates in the self-resonant mode or locked at a half of the input frequency, $g_{m,dc}$ in the quiescent-operation-point can no longer show the circuit behavior. Therefore, an effective transconductance ($g_{m,eff}$) is proposed for a more accurate prediction. Considering that the NG cell mainly manipulates signal at the output frequency, thus the $g_{m,eff}$ can be defined as

$$g_{m,eff} = \frac{|I_{ds-1st}|}{|V_{gs-1st}|} \tag{7}$$

where I_{ds-1st} and V_{gs-1st} denote the fundamental of the drain current and gate-source voltage, respectively, which can be extracted by the PSS simulation using SpectreRF.

According to the phase criterion and β_{tank3} in (6), both the simulated and predicted f_{SR} are obtained versus V_{BD}.

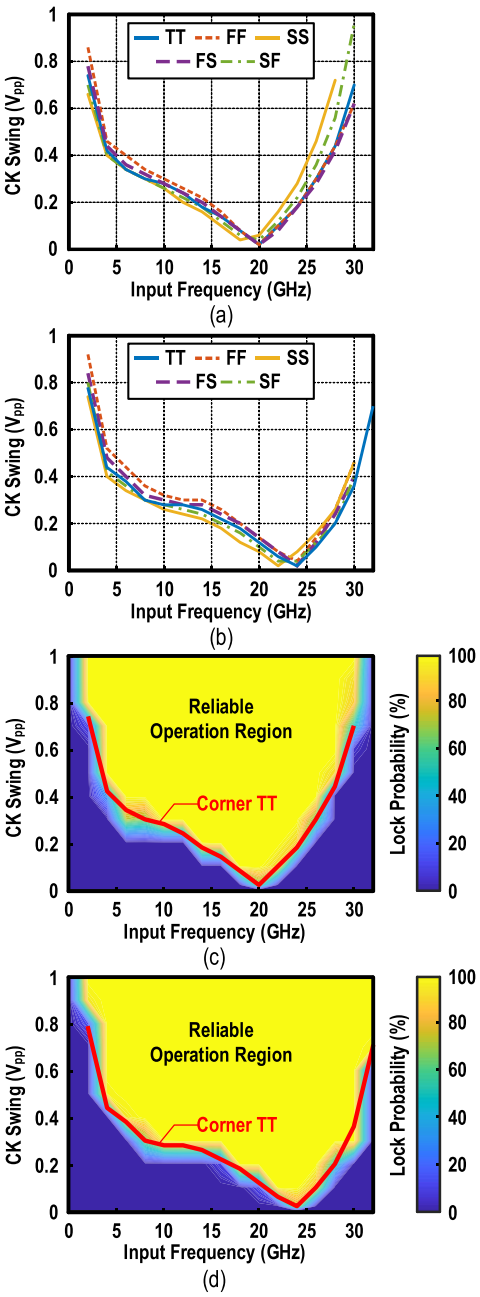

Fig. 15. Post-layout simulation results of SCs (a) and (b) under different process corners: Fast-Fast (FF), Slow-Slow (SS), Typical-Typical (TT), Fast-NMOS-Slow-PMOS (FS) and Slow-NMOS-Fast-PMOS (SF). Lock probability (c) and (d) from Monte Carlo analysis (50 runs), where $V_{BD} = 0.2$ V in (a) and (c), $V_{BD} = 1$ V for (b) and (d).

Both $g_{m,dc}$ and $g_{m,eff}$ are substituted into (6) for the f_{SR} prediction. Similar to the case in Section III-B, the desired β is also obtained by the simulation. Plotted in Fig. 10, when $V_{BD} < 0.4$ V, two predicted curves agree with the simulation results well. Yet, when the NG cell is strong enough to experience the large-signal operation, the result calculated from $g_{m,dc}$ deviates from the simulated one severely, while the calculation by the aid of the time-variant $g_{m,eff}$ provides a better f_{SR} prediction.

Considering a 0.8-V_{pp} CK swing in Fig. 11, the RLC tank and our tank with the NG cell under zero V_{BD} share nearly

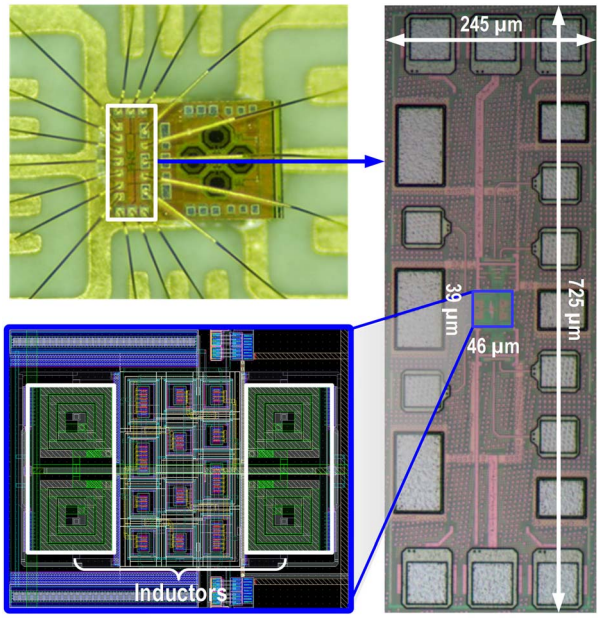

Fig. 16. Chip micrograph with bonding scheme and core layout detail.

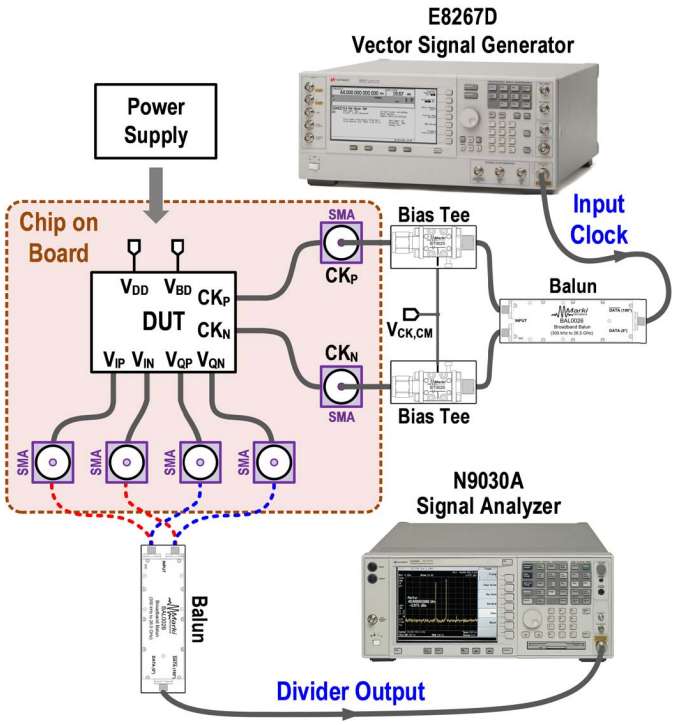

Fig. 17. Measurement setup of our DUT.

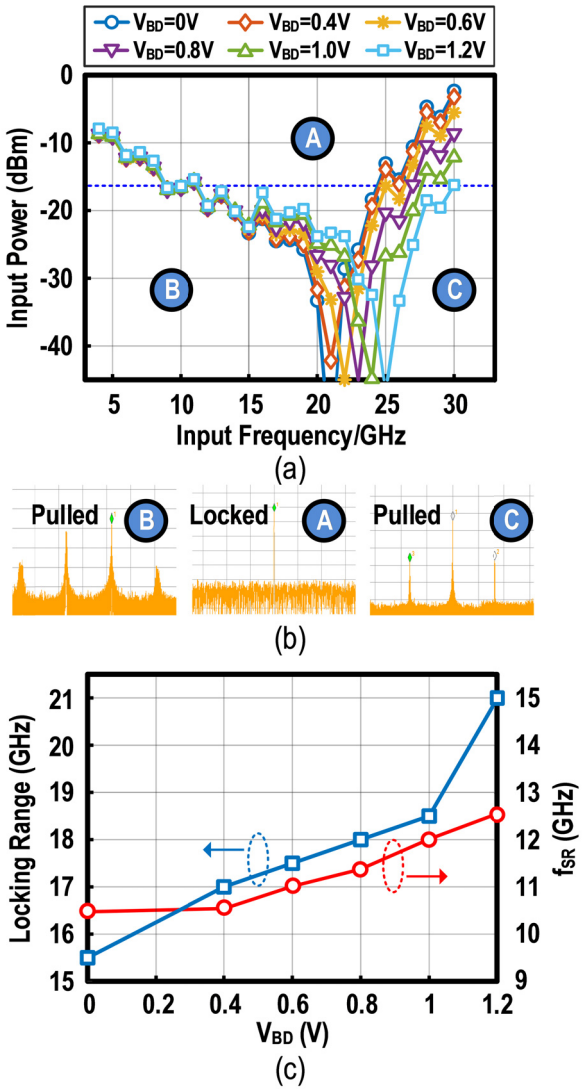

Fig. 18. (a) Measured SCs under different V_{BD}. (b) Spectrums in locked condition and pulled condition. (c) LR and f_{SR} versus V_{BD} with an input power of -16 dBm.

TABLE I
DESIGN PARAMETERS OF THE PROPOSED DIVIDER

M_C	M_{CKC}	M_L	M_{CKL}	M_N
5 / 0.06	5 / 0.06	11 / 0.06	5 / 0.06	10 / 0.06
R_1 = 281.8 Ω		L_1 = 0.73 nH @14 GHz		

the same upper operating limit. However, as V_{BD} increases up to 1.1 V, the limit is expanded to ∼43.5 GHz. Due to the NG cell, our divider achieves a wider overall locking range of ∼15.6% (*red solid line*) than that with the RLC tank (*bluesolid line*).

IV. Implementation and Simulation

Both the shunt-peaking inductor and the NG cell promote our divider to a higher operating frequency. However, the inductor may occupy more area and the NG cell may consume additional power. Therefore, it is instructive to study the tradeoffs between these two issues to achieve the optimal results. The contour of the normalized f_{SR} is plotted in Fig. 12, where f_{SR} and power dissipation are normalized to their corresponding value under $L_1 = 0$ and $V_{BD} = 0$. To operate at a specific f_{SR}, we may penalize some area to reduce the power, and vice versa. For example, all the points A, B, C and D are the candidates to obtain a 1.6-times normalized f_{SR}. Yet, from points A to B and C, the increasing power relaxes the area requirement and it is obviously a sub-optimal choice for the condition at point D.

TABLE II
SUMMARY AND PERFORMANCE COMPARISON WITH STATE-OF-THE-ART DIVIDERS

Parameters	This Work	TCAS-II'11 [15]	JSSC'17 [7]	JSSC'13 [11]	IMS'17 [25]	TMTT'19 [8]	TCAS-I'13 [9]
CMOS (nm)	65	180	130 BiCMOS	32	130 BiCMOS	180	65
Key Technique	Shunt-Peaking with Negative-g_m cell	Active Inductor Tank	Distributed Injection Locking	Dynamic Latch with Load Modulation	Multi-Injection Locking	Resistively Distributed Injection Locking	Harmonic Boosting Injection Locking
Division Ratio	2	2	2	4	2	2	4
V_{DD} (V)	1.2	1.8	1.2	1	1.6	0.8	0.6
f_c [c] (GHz)	17	13.75	47.25	55	36.5	6	65.6
LR [d] (GHz / %)	**4-30** [a] **/ 152.9**	7.5-20 / 90.9	35-59.5 / 51.9	40-70 [b] / 54.5	12-61 / 134.2	3-9 / 100	58.5-72.9 / 21.9
P_{dc} (mW)	4.28	4.3	3.8	4.8	10.4	9.8	2.2
P_{in} (dBm)	0	0	0	0	0	0	0
FOM_{Pdc} (dB) [e]	**25.5**	23.3	21.3	20.6	21.1	20.1	20.0
FOM_P [f]	**71.5**	42.3	27.3	45.5	25.8	20.4	39.9
Area (mm^2)	0.0018	0.014	0.046	0.001	0.0016	0.76	0.042

[a] The maximum and minimum input frequency is limited by our available equipment.
[b] Locking range for a fixed bias voltage. [c] $f_c=(f_{max}+f_{min})/2$. [d] $LR=f_{max}-f_{min}$.
[e] $FOM_{Pdc}=10\log[(LR/f_c)x(1W/P_{dc})]$. [f] $FOM_P=(LR/f_c)x[(\text{Division Ratio})/(P_{dc}(mW)xP_{in}(mW))]x100\%$.

Recalling Section II-B, we select L_1 based on the simulation result in Fig. 5. With the help of the NG cell, we reconsider the effect of L_1 on f_{SR} in pre-layout simulation with the ideal L_1. As shown in Fig. 13, 0.75-nH L_1 is still in the quasi-linear region even for different V_{BD}. Based on the above analysis, a proper inductance is chosen to balance the above trade-off. A 3-D solenoid inductor is designed for shunt-peaking technique, which is composed of four stacked metal layers (Metals 4 to 7), occupying only 10×10 μm^2 (Fig. 14). From the electromagnetic simulation, the inductance and quality factor (Q) are 0.73 nH and 1.41 at 14 GHz, respectively. Table I summarizes the design parameters corresponding to our design *line* in Fig. 12. Benefiting from the 3-D solenoid inductor and NG cell to have a tunable f_{SR} and higher operating frequency, our divider achieves a LR between 2 to 32 GHz.

We perform the post-layout simulation and plot the SCs under different process corners and lock probability contour charts in Fig. 15. The f_{SR} shifts from 10 to 12 GHz when V_{BD} varies from 0.2 to 1 V. At each frequency, Monte Carlo analysis is conducted with 50 times, the SCs at different process corners and contour charts imply a robust operation for our divider.

V. MEASUREMENT RESULTS

Our divider was prototyped along with the test buffers in 65-nm CMOS technology, and was tested via chip-on-board setup (Fig. 16). The core area is 39×46 μm^2, including four ultra-compact shunt-peaking inductors in the layout detail.

The measurement setup is shown in Fig. 17. The differential input clock is provided by the vector signal generator (VSG) with a wideband balun, which is then applied to the device under test (DUT). And two pairs of the differential outputs of our DUT are measured by the signal analyzer.

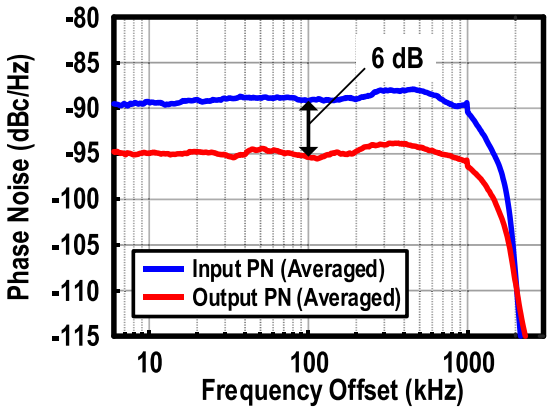

Fig. 19. Input and output phase noise of the proposed divider.

Fig. 18(a) depicts the measured SCs when $V_{DD} = 1.2$ V and $V_{CK,CM} = 0.6$ V. The curves are almost coincident at lower frequency. However, a larger V_{BD} raises f_{SR} and expands the upper limits of SC, which is consistent with the analysis in Fig. 7 in Section III and the simulation in Fig. 15 in Section IV. The f_{SR} ranges from 10.63 to 12.5 GHz when V_{BD} varies from 0 to 1.2 V. Two cases (B, C) in Fig. 18(b) show the characteristics of the pulled oscillator, indicating that the divider is out-of-lock since the Barkhausen criterion is not satisfied. While the case A in Fig. 18(b) represents the spectrum in locked condition. Our divider exhibits a LR of 153% from 4 to 30 GHz suitable for a number of 5G New Radio bands, and draws 4.06 to 4.28 mW. Note that the upper limit of the operating frequency is not 30 GHz, but is limited by the available equipment. Particularly, the input power in Fig.18(a) is the output power of the VSG with calibration for cables, adapters and baluns.

Fig. 19 shows the measured phase noise (PN) performances of the divider with a 28-GHz input signal. The averaged output PN at low-frequency offsets follows the input with a 6-dB difference which matches with the theoretical value. In order to avoid the equipment's limitation, we use the phase modulation (PM) option in the VSG to raise the PN level of the input clock. A Gauss noise is used for the PM at 1 MHz offset, thus obtaining the PN shape in Fig. 19. Table II summarizes the performance comparison of the proposed divider with the state-of-the-art. Our divider succeeds in enhancing the flexibility of f_{SR} with a LR of 153% to achieve good figure-of-merits: FOM_{Pdc} of 25.5 dB and FOM_P of 71.5.

VI. Conclusions

This paper reports a LR-extension technique with the tunable self-resonant frequency for the NG-cell-inserted CML-based divider. Based on the injection-locking concept and graphical analysis, the self-resonant frequency and LR of the CML-based divider with three different tanks are investigated in detail. The proof-of-concept prototype is a divider-by-2 fabricated in a 65-nm CMOS process. It exhibits a 153% LR while occupying a tiny area of 0.0018mm^2. Measured results show that our divider achieves good FOMs with low power consumption.

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