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Quick and cost-efficient A/D converter static characterization using low-precision testing signal

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ABSTRACT

The measurement of the analog-to-digital converter (ADC) output by exciting the signal generator with a high precision input signal allows the determination of ADC's static characteristics using a histogram-based approach. However, this method exhibits some limitations imposed by the input signal, including its high resolution and high linearity that are causes for concern when testing a high precision ADC. Recent research work has been trying to overcome such limitations. Nonetheless, it is necessary to discover a simple and low-cost method to measure the linearity of a high precision ADC through a low precision stimulus. This paper introduces a novel procedure that allows the relaxation of the requirements of the signal source for estimating ADC's linearity characteristics. The proposed method requires two sets of testing sources, being both ramp signals, one of low-precision and the other attenuated. Simulation and experimental results validate the proposed method in different ADCs.

1. Introduction

In mixed-signal systems, analog-to-digital converters play a crucial role and to ensure efficiency in their performance, low cost and high accuracy ADC testing methodologies are necessary. Besides, ADC measurement faces typically various challenges because it requires a large number of samples, and also a long time for high-accuracy converter testing.

As linearity is a crucial characteristic for many commercial ADC applications, integral nonlinearity (INL) constitutes a crucial parameter. Fig. 1 shows a traditional ADC static testing flowchart [1]. To measure static ADC characteristics, a histogram-based method defined by the IEEE standard 1241-2010 [2], which requires the application of a highly precise input signal to such high-resolution ADC, is usually adopted. Because of the degree of linearity, there is a direct relationship between the number of measurement points and the accuracy and reliability of the ADC testing results. For instance, for a 16-bit ADC, with a minimum 19-bit-resolution input signal, the conventional histogram-based approach requires about two million samples and a long testing time. Performing the test with such high precision signal source is quite difficult.

This paper proposes a simple and low-cost method to estimate static integral nonlinearity in high-precision ADCs with low-precision signals, by introducing two different amplitude ramps into the ADC under testing. A quick and straightforward polynomial that requires only a small set of measurement points, leading to a much lesser testing time, can simplify the description of the transfer curve of the ADC. The polynomial allows the estimation of the INL through a set of coefficients, and the ratio-metric relationships between different stimulus signals can assist in desensitizing the nonlinearity errors originated in the signal source. Because of the reduction in the number of samples and the input signal precision, this method provides a more rapid and cost-effective ADC estimation than the traditional histogram-based procedure.

The remaining part of this paper has the following organization: Section 2 presents a brief review of the literature related with this work; Section 3 presents a brief discussion and the definitions of the ADC testing; Section 4 describes, in detail, the proposed method; Sections V and VI provide the simulation and experimental results, respectively, under various resolutions of high-precision ADCs.

2. Review of existing ADC static testing methods

Over the years, the histogram-based method has been widely utilized till recently because of its speed and simplicity of operation. Moreover,

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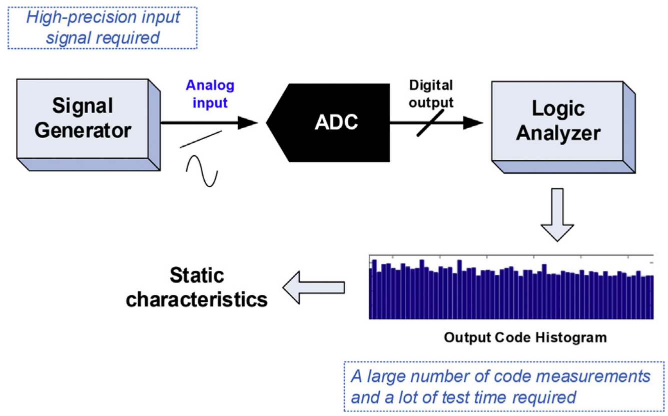

Fig. 1. Traditional ADC static testing flowchart.

many literature works are presented on static ADC testing, using low-precision signals.

In Ref. [3], the authors introduce a deterministic dynamic element-matching approach (DDEM) for ADC testing, under which the DAC is the signal source, and the excitation generated by the DAC is processed by the DDEM before entering the ADC under testing. This technique relaxes the linearity requirement of excitation. The DAC was specially designed, fabricated and tested to verify this approach, but the number of measurement points was found to be still too large for high-resolution ADC testing.

Based on the histogram method used in the testing of high-accuracy static performance ADCs [4], proposes a method for stimulus error identification and removal (SEIR) that uses a signal source with less linearity than that of the ADC under testing. The most salient part of this method is the application of two, nonlinear, low precision, but functionally related excitations to the ADC input to obtain two sets of output code data. In this approach, an algorithm removes the stimulated nonlinear errors by using information from the two sets of ADC output data. However, the number of samples is still too large and the testing time is still too long. In addition, the authors in Ref. [5] also use two low-resolution signals with an offset estimated in the static characterization. This method employs the low-resolution signal and utilizes the polynomial functions with fewer samples. However, it requires an additional potentiometer and an analog adder.

A simple method for the application of a nonlinear ramp input signal was presented by Ref. [6], in which the measured ADC static performance was little influenced, as there were regions that were more linear even in a nonlinear ramp. A ramp signal characteristic was employed to estimate the ADC static performance via a non-linear ramp. In addition, another novel method was introduced in Ref. [7] for estimating the static nonlinearity of the ADC, using a low-frequency sinusoidal signal. It utilizes the theory that the variation of such a signal is “reasonably linear” for small angles. However, when testing the high-resolution ADC using the histogram-based method, a large number of samples are collected to ensure the reliability of the measured results.

An ultrafast segmented model identification of linearity errors (uSMILE) [8] algorithm was introduced to adopt a system identification approach that obtains the linearity performance of ADC. This method can reduce the test data and achieve good test accuracy, but it still requires a highly linear input signal source. In addition, the algorithm proposed in Ref. [9], which combines the concept of SEIR and uSMILE, applies two nonlinear input signals with a constant offset between them to the ADC. It relaxes the requirement on source linearity and reduces the testing time. Nevertheless, it needs an additional offset generator. These methods target high-resolution ADCs, whose architecture facilitates a segmented structure.

With growing demand for high-quality integrated ADCs, the focus of research has been on designing high-performance ADCs. The measurement of a high-performance and precise ADC is a significant technological challenge, and linearity of high-precision converters is the primary concern in commercial applications. The histogram-based method, which is widely used for ADC static testing, requires high linearity and high-resolution signal. Besides, the testing time, which is based on the number of samples and the testing algorithm, continues to be long when estimating high precision ADCs through the traditional histogram-based method. The method proposed in Ref. [10] divides the INL into low and high code frequency components wherein the low code frequency component can be described by a polynomial. However, it requires an exact DC component and still needs the histogram test. The proposed method introduces a more cost-efficient way to obtain higher accuracy estimations of the ADC's static characterization.

The existing methods of ADC static testing are numerous and effective but still have some limitations, and traditional histogram-based method requires simultaneously a high linearity and high-resolution input signal and long testing time. Therefore, a new approach that relaxes the linearity and resolution requirements is needed, and the key advantages of that approach should be the elimination of errors that originate in the input source and faster determination of the actual transfer curve with fewer measurements.

3. Review of terminologies for ADC testing

3.1. Transfer curve test

The ADC transfer curve shows the digital output codes as a function of the analog input. INL, a performance specification of ADC, is the measure of the deviation of the actual values from the ideal transfer function at the transition code point; in other words, it is a specification of the nonlinearity errors of the ADC under testing. The INL, which shows the deviations from the ideal ADC transfer curve, is expressed by

$$INL(i) = \frac{x(i) - x_{ideal}(i)}{\Delta} \tag{1}$$

where i denotes the ADC output code varying from $i = 0 \ldots (2^m\text{-}1)$, $x(i)$ the actual voltage transfer characteristics at the individual steps and m the resolution of the ADC; $x_{ideal}(i)$ is the corresponding ideal version and $\triangle$ the ideal step size. Therefore, the transfer curve constitutes the core of the static ADC linearity, and to obtain it accurately for high-precision ADC testing, numerous test data points and an advanced precision signal source are necessary. In the proposed method, the objective has been to improve the testing efficiency while reducing the cost of generating the test signal.

3.2. Transfer function

Fig. 2 shows an example of two ADC transfer functions, one an ideal one and the other an actual one. The nonlinearity of the transfer function then becomes,

$$x(i) = a_0 + a_1 y(i) + \ldots + a_p y^p(i) \tag{2}$$

where $i = 1,2, \ldots, (2^M\text{-}1)$, and M is the resolution of the input signal. In this nonlinear transfer function, which is a simplified polynomial fitting function based on [11], the simplification implies a limitation to *p-th* order equations and the finding of the coefficients ($a_0 \ldots a_p$) of the best-fitting curve described in this function. All the analog voltage values, $x(i)$ for the digital code $y(i)$, can be evaluated when all the polynomial coefficients a are found.

3.3. Total least squares estimation

Given an over-determined set of L linear equations in N*1 unknowns [12], A is an $L*N$ data matrix, a vector of b observations having L

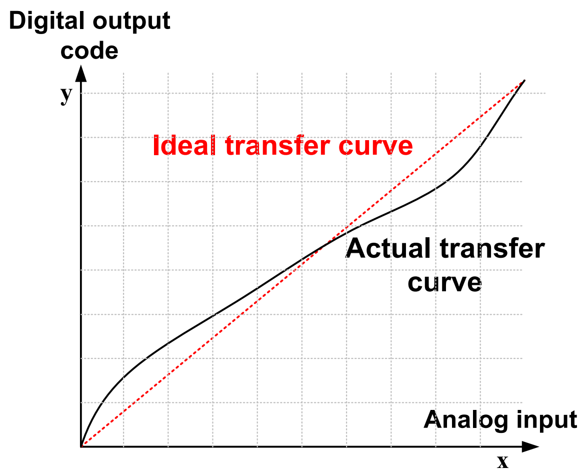

Fig. 2. The ADC transfer curves.

components, and vector c has to be found such that,

$$Ac + r = b \;\; A \in R^{L*N}, b, r \in R^{L*1} c \in R^{N*1} \tag{3}$$

where r is an L vector, which represents the observation noise record. The least squares (LS) problem involves the finding of a solution vector c that allows the sum of the squares of r to be minimum, such that,

$$\|r\|_2 = \|Ac - b\|_2 = \text{minimum} \;\; b + r \in range(A) \tag{4}$$

where $\|\cdot\|_2$ is the l_2 norm given by

$$\|r\|_2 = \left(\sum_{i=1}^{L} r_i^2\right)^{1/2} \tag{5}$$

From the preceding steps, the optimal estimate solutions are,

$$c_{LS} = [A'A]^{-1}A'b \tag{6}$$

However, the idea behind the total least squares (TLS) is to focus on accounting for the perturbation of both b and A,

$$(A + E)c = b + r \tag{7}$$

where E is an $L*N$ vector and (7) can also be expressed as,

$$([A\ b] + [E\ r])\begin{bmatrix} c \\ -1 \end{bmatrix} = 0 \tag{8}$$

or

$$(B + D)Z = 0 \tag{9}$$

where $B = [A\ b]$, $D = [E\ r]$, $Z = [C\ -1]^T$. Here, the TLS estimation should be employed to obtain an optimal estimate of c, which is under the minimum Frobenius norm condition. That is, the solution to the above equation can also be formulated by seeking a solution vector c such that

$$\|D\|_F = \text{minimum}, \;\; b + r \in range(A + E) \tag{10}$$

where $\|\cdot\|_F$ w denotes the Frobenius norm given by $\|D\|_F = (\sum_i \sum_j d_{ij}^2)^{1/2}$. The TLS involves the determination of the perturbation matrix D, having the minimum norm, and a singular value decomposition to overcome such problem.

4. Proposed method

Here we analyze, first, the differences between the traditional histogram-based and the proposed methods, which use different amplitude signals. For the proposed method, a low-precision input signal is enough to obtain ADC static performance; besides, a simple estimation allows for measurement with fewer points.

4.1. Main differences between the traditional and the proposed methods

Fig. 3 shows the proposed testing flowchart, with the normal and the attenuated ramps applied to the ADC (Device-Under-Test, DUT). The change in the signal amplitude will lead to an attenuated signal. However, the histogram reflects the number of times each individual code occurs, and the histogram-based method applies a test signal, which is slightly larger than the full scale of the ADC, to ensure that all valid codes are obtained. During the testing of a high precision ADC, it is challenging to obtain a highly linear ramp; therefore, much more transition-level information is required. Also, the number of measurement points rises exponentially with the increase of the resolution. For testing a 16-bit ADC approximately 32 samples per code are necessary to build reliable histograms [2], which in turn require approximately 2097152 samples. Therefore, implementation of high-resolution ADC static testing, with a large volume of measurement points and many test runs, becomes a formidable task.

On the other hand, in the proposed method, the ADC transfer curve that reflects the correlation between the analog input and the digital output codes is utilized. Further, it is evident that using a simple and effective method to set up the transfer function of the testing ADC is indispensable for static testing, because the transfer function will lead to the determination of ADC static characteristics. However, unlike the histogram-based method, which requires many samples to ensure the reliability of the histogram, the proposed method needs only a few samples to build the transfer curve function. The nonlinearity of the testing ADC can be desensitized, and its measurement results are not affected by the nonlinearity of the testing signal. Therefore, what is determined here is a mathematical algorithm that offers higher efficiency

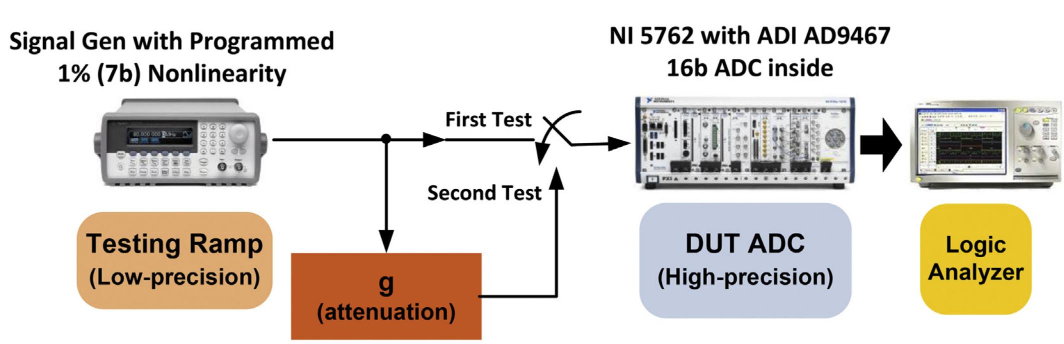

Fig. 3. The proposed ADC testing flowchart.

and improved flexibility, with lower costs and more straightforward deployment.

4.2. Advantages of the proposed method

The proposed method has the following four advantages over the traditional method:

a) It measures high-precision ADCs with relatively relaxing requirements of the signal source, e.g. high resolution and linearity test signals. This, indeed, is an important favorable advantage regarding cost.
b) It uses two test sets, one being an attenuated version of the other. The attenuator can be off-chip, on-chip, or by simple programming of the code-controlled DACs that generate the source.
c) It fully uses the information in the output codes for determination of the transition point. In particular, it applies a simple calculation algorithm after collecting data from the two test sets. It evaluates the static ADC specifications through a polynomial fitting algorithm to get the ADC transfer curve. This saves the testing time, when compared with the traditional histogram-based method, because the number of samples is smaller.
d) It is more cost-efficient, because of a much-reduced testing time than that of the histogram-based method; besides, it utilizes less expensive instruments.

4.3. Theoretical background

In the proposed method, two test sets are used, one a normal test signal *x(i)* and the other an attenuated signal $x_g(i)$. The relation between the two is expressed thus:

$$x_g(i) = g^*x(i) \tag{11}$$

where g is the attenuation of the input signal. The input signals of the two test sets, which are generated by the same signal source, have the same frequency contents and nonlinearity condition. The only difference between them is in their amplitude, which is an attenuated version of the one in the other. In the proposed method, we use two ramps in which the sampling is done at exactly the same instant. Two ramps are from the same signal generator (they are just differentiated by the programmable attenuator g) and their sampling frequencies, as well as the ramping periods, are the same. We store for calculation only one sample period for both ramps in every test cycle. However, the accuracy of the signal source required here is lower than the one required in the conventional histogram-based method. Then, by substituting (2) into (11), it yields:

$$a_0 - g^*a_0 = \sum_{j=1}^{p}\left[g^*a_j y^j(i) - a_j y_g^i(i)\right] \tag{12}$$

The first coefficient is a_0, whose value is determined by the offset and the full-scale voltages. In experimental environment, the real values are not always the same as the default values. Considering the errors between the real a_0 and the tentative A_0:

$$a_0 = A_0 + \Delta a_0 \tag{13}$$

Then,

$$A_0 - g^*A_0 = \sum_{j=1}^{p}\left[g^*a_j y^j(i) - a_j y_g^i(i)\right] + \varepsilon \tag{14}$$

$$\varepsilon = g^*\Delta a_0 - \Delta a_0 \tag{15}$$

Measurement of the output codes from the above and the data of i from 0 to 2^M-1 shows that every digital code corresponds to one equation with the total number of equations determined by the digital output codes. Accordingly, the more the collected data and the test times, the more are the equations generated. Then, from (7), the following matrix can be formulated,

$$\underbrace{(A_0 - g^*A_0)^*\begin{bmatrix}1\\ \vdots\\ \vdots\\ 1\end{bmatrix}}_{b} = \underbrace{\begin{bmatrix}\left(g^*y(0) - y_g(0)\right)\cdots\left(g^*y^p(0) - y_g^p(0)\right)\\ \left(g^*y(1) - y_g(1)\right)\cdots\left(g^*y^p(1) - y_g^p(1)\right)\\ \vdots\\ \left(g^*y(2^M-1) - y_g(2^M-1)\right)\cdots\left(g^*y^p(2^M-1) - y_g^p(2^M-1)\right)\end{bmatrix}}_{A+E}\underbrace{\begin{bmatrix}a_1\\ a_2\\ \vdots\\ a_p\end{bmatrix}}_{c} \underbrace{+\,\varepsilon^*\begin{bmatrix}1\\ \vdots\\ \vdots\\ 1\end{bmatrix}}_{-r} \tag{16}$$

For this overdetermined system, the TLS algorithm can be used to find the unknown vector c. Then the INL of this ADC can be constructed.

4.4. Polynomials discussion

Matrix Equation (16) is linear on the vector of the coefficients, with the errors in the estimation of g transferred to it, because the actual attenuation value may be different from the simulated value. There are errors on both sides of the equation. The TLS method finds an optimal solution vector c that minimizes the error perturbation of the effect from both A and b. Besides, it can average out the effects of noise and errors.

In this case, attenuation g can be estimated by merely averaging the difference between the collected output codes $y(i)$ and $y_g(i)$. The accuracy of this attenuation value g depends on the precision of the signal source and the number of measurement points. In the proposed experiment, this method of estimating the attenuation value is accurate enough to acquire the results presented next. Also, we choose the order value (p), based on the number of points calculated and avoiding over-fitting [13]. In the simulations, 2nd and 3rd orders are chosen for the 12-bit and 16-bit ADC, respectively.

A TLS fitting algorithm evaluates the coefficients, which lead to the determination of ADC's transfer function. Subsequently, the static characteristics of the testing ADC are derived.

Apparently, because the transfer curve is highly complicated, a single-section transfer function is not sufficient to build an accurate model. Therefore, the transfer curve needs to be segmented into many sub-sections. The foregoing polynomial method is used for every section curve, and we use the TLS method to solve the polynomial coefficients, which define the transfer function curve of that section. Each transfer curve in different sub-sections is constructed by the measurement points of that section with the proposed algorithm, and then the overall transfer function can be obtained by fitting together all the sub-section curves from different sections. Based on this, a much more accurate single ordinary transfer function was attained, with no need for any additional measurement points. Each sub-section transfer curve has its own linearity condition. Consequently, in each section, a few output digital codes, experimentally obtained and belonging to that part, will form the matrix about such section transfer function. Also, the total number of sub-sections depends on the number of measurement points, and the number of measurement points in every sub-section should be adequate to ensure we obtain the corresponding polynomial coefficients. In the following simulations, 50 and 200 sub-sections were chosen for the 12-bit and 16-bit ADCs, respectively.

5. Simulation results

The proposed method was verified by analyzing the behavior model (with MATLAB) of two ADCs, one with 12-bit resolution and the other with 16-bit resolution. The simulations were obtained on a nonlinear ramp model, by processing the signals with different resolutions and percentages of nonlinearity.

5.1. Low-precision test signal

The 10-bit resolution input signal source, along with its maximum produced ramp signal, possesses approximately 1% nonlinearity, expressed as follows,

$$x(i) = i + 0.04^{*}\left(i^{2} - i\right) \quad (1.00\%NL) \tag{17}$$

5.2. Simulation details

Simulations with MATLAB, 12-bit and 16-bit ADCs were used. To ensure accurate results for static characteristics as a reference, a high precision signal and a sufficient number of samples (131072 and 2097152 samples for 12-bit and 16-bit ADCs respectively) were used to test the ADC by the traditional histogram-based method, which led to the true INL. The results, presented in Fig. 4(a), show a calculated INL of the 12-bit ADC, which is approximately 7LSBs. Next, a low-precision input signal from Equation (17), used in the model with the traditional histogram-based method, was introduced to calculate the output data and the results obtained are shown in Fig. 4(b) (red line). Then, the proposed method was used to measure the INL of the ADC with this low-precision signal, repeating the measurement 20 times for averaging noise effects from the signal source in each testing case, and collected only 1024*2*20 measurement points with the 10-bit signal source. For this, the amplitude of the input signal was changed to get two sets of data, as shown in Fig. 4(c). An attenuation of 0.9, was chosen for the 12-bit and 16-bit ADCs simulations, respectively. Replication of the 12-bit ADC verification process in the 16-bit ADC case led to the results presented in Fig. 5. The nonlinearity of the input signal was maintained at the same

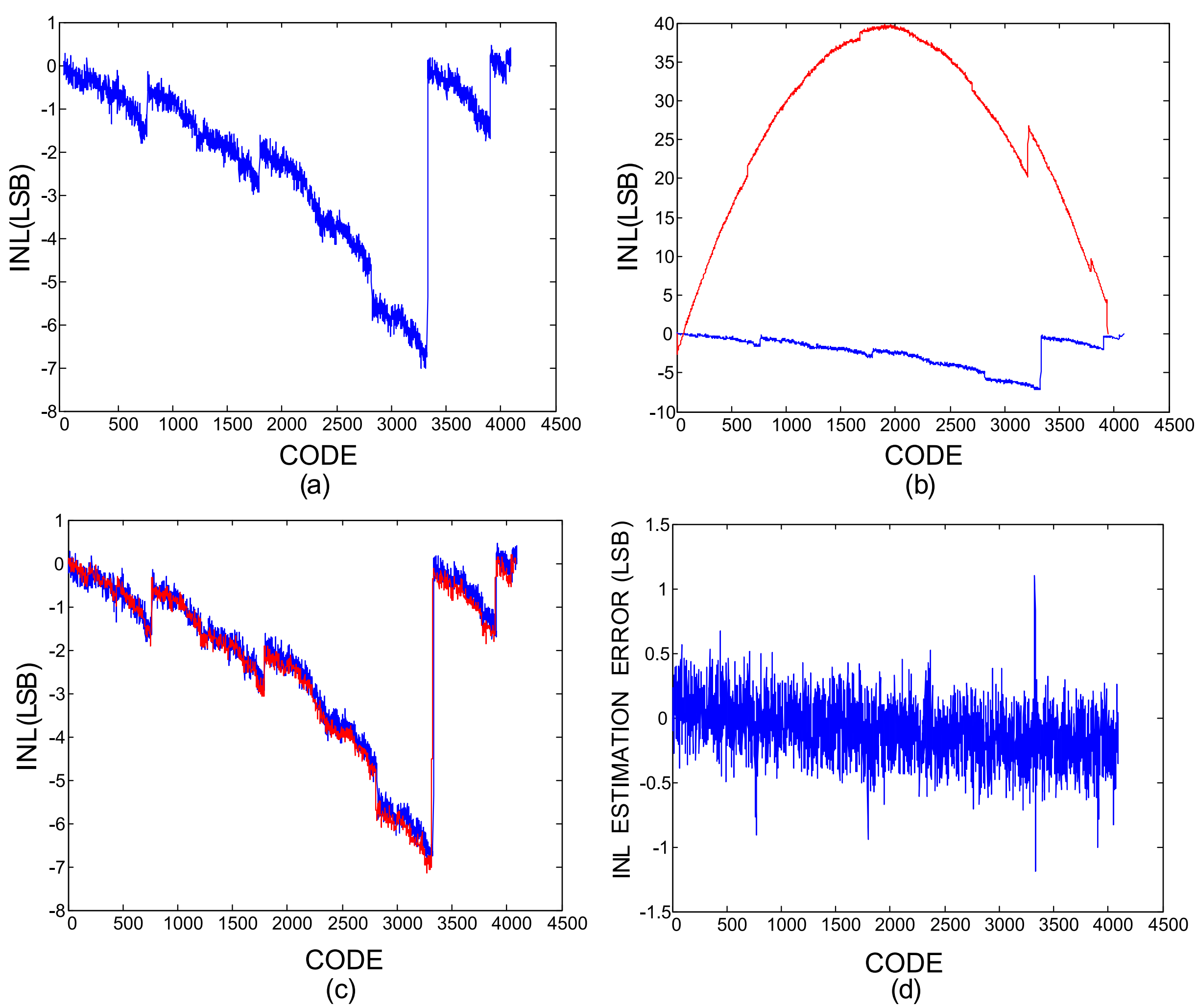

Fig. 4. (a) True INL of a 12-bit ADC; (b) True INL (blue line) and INL obtained from the 12-bit ADC output code histogram with nonlinear input (red line); (c) True INL (blue line) and INL obtained from a 12-bit ADC with nonlinear input (red line) by using the proposed method; (d) INL estimation error of the proposed method. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

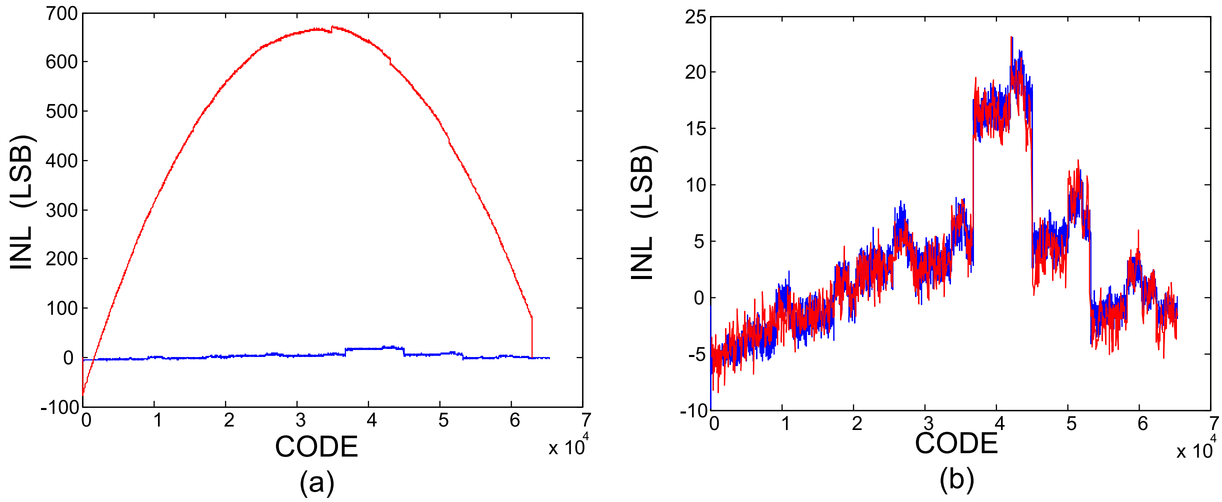

Fig. 5. (a) True INL (blue line) and INL obtained from the 16-bit ADC output code histogram with nonlinear input (red line); (b) True INL (blue line) and INL, using the proposed method obtained in a 16-bit ADC with nonlinear input (red line). (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

level to facilitate comparison of the INL values between the histogram-based method and the proposed method. The number of samples was also equal to 40960.

5.3. Simulation results - discussion

Fig. 4 shows the simulated INL results obtained from the 12-bit ADC, with the true INL errors shown in Fig. 4(a). For nonlinearity input signal, both the histogram-based and the proposed methods were used to measure the INL. Fig. 4(b) shows that the difference between the true INL and the one calculated by the traditional histogram-based method, with 1% nonlinear signal, is approximately 41 LSB. This value clearly confirms that the nonlinearity level of the input signal is approximately 1%. Moreover, the results obtained with the proposed method, which are shown in Fig. 4(c), are much better than those obtained from the histogram-based method, using the same 1% nonlinear test signal. Fig. 4(d) shows that the ΔINL (ΔINL is the maximum difference between the true and the estimated INLs [14]), obtained by comparing the estimated INL from the proposed method with the true INL, is about ± 1 LSB. These results show that the proposed method produces good estimation accuracy over all the codes.

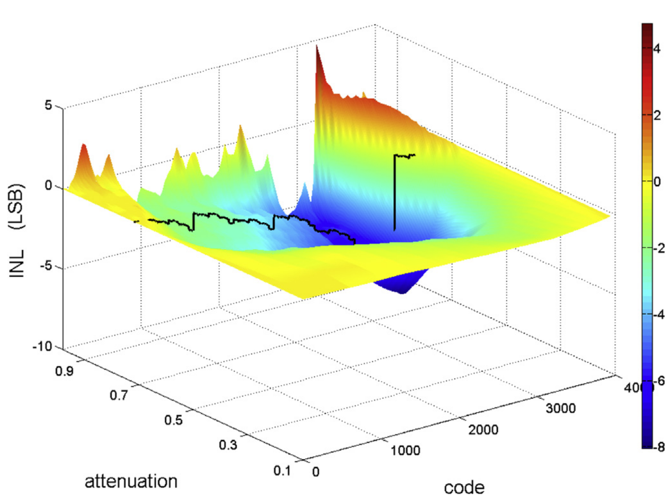

Fig. 6. INL of the 12-bit ADC using the proposed method with different attenuation values.

Fig. 6 illustrates the INL of the 12-bit ADC obtained by using the proposed method with different attenuation values. The solid black line represents the true INL. The value of attenuation (*g*), between the two input signals, affects the final INL estimation results. When the difference between the two input signals is very small, the noise will have a significant effect on the TLS method if the gain is too small. On the other hand, the attenuation cannot be too large either, because the TLS result is optimal for part of the input nonlinearity and not necessarily for the nonlinearity of the whole transfer curve if the attenuation is too large. A lot of simulation results indicate that attenuation of 0.85–0.95 is appropriate for the proposed method. Both simulation and experimental results support this conclusion.

The proposed method was also applied to the 16-bit ADC. Fig. 5(a) shows that the difference between the true INL and the one calculated by the traditional histogram-based method, with 1% nonlinear signal, is approximately 656LSB. The true INL and the INL obtained by using the proposed method with the same nonlinear input are presented in Fig. 5(b). It needs to be emphasized here that the ΔINL in Fig. 5(b) is just 4.9LSB (0.007%). The results of the proposed method are of great significance, because they allow for approximately 99% reduction in the influence of the nonlinearity of the source. Fig. 7 shows the INL obtained with a linear input signal (but with a 10-bit resolution only), using the histogram-based method in the 16-bit ADC. In this case, the ΔINL obtained by comparing the true INL and the INL in Fig. 7 is 63LSB, which is much greater than the ΔINL in Fig. 5(b) with the proposed method (also using a 10-bit resolution of input signal). The proposed method acquires better results than the histogram-based when a low-resolution input signal is utilized. This confirms that the proposed method can relax the resolution of the signal source.

6. Experimental results

The proposed method was verified and compared with the traditional histogram-based method using real ADCs embedded in a modern testing environment, as described below.

6.1. Experimental details

Two high precision ADCs, embedded with the following equipment, were tested: Agilent DSA90254A digital sampling oscilloscope [15] (using an equivalent 13-bit digitizer performance) and NI 5762 16b 250MS/s digitizer module [16] with Analog Devices 9467 CE chipset inside [17]. NI PXIe-5451 Arbitrary Waveform Generator (AWG) [18]

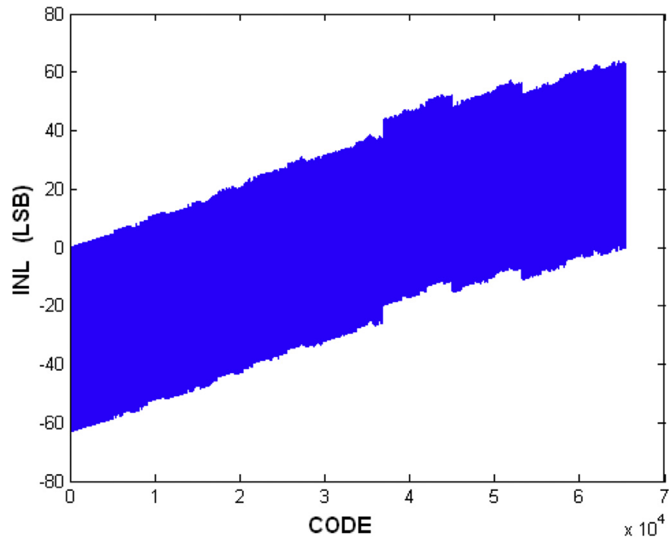

Fig. 7. INL with a linear input signal (only 10-bit) using the traditional method in a 16-bit ADC.

and Agilent 33250A AWG (12-bit) [19] were used as the test signal source for the experiments. The nonlinearity of the signal sources was programmed with computer software. Each ADC test required two test sets, one to generate the ramp signal with the ADC's full-scale and the other with an identical ramp, but, with reduced amplitude. 100 and 200 sub-sections, with 2nd and 3rd order polynomial functions and with an attenuation of 0.9, were chosen for the 13-bit and 16-bit ADCs, respectively. Finally, the digital codes were collected from the logic analyzer, using two different amplitude input signals, to perform the calculations with the proposed algorithm and to determine the static characteristics from the testing of the ADCs.

6.2. *Experimental results - discussion*

Agilent DSA90254A was a high-performance oscilloscope that included a high-performance AD converter. NI PXIe-5451 (16-bit) AWG was used for generating the ramp input signal with programmed nonlinearity. Fig. 8 (a) shows the true INL of the ADCs tested by using 262144 samples. From Fig. 8 (b), it can be seen that the INL measured, using the histogram-based method, is around 70LSB in a 13-bit level with the nonlinearity input signal. The INL measured by using the proposed method is much closer to the true INL, as can be seen in Fig. 8 (c). Thus, even with a low precision signal source the difference between the INL measured by using the proposed method and the true INL is much smaller.

For the 16-bit 9467 CE, a 19-bit high-linearity signal source was found necessary to test this high precision converter, but 16bit NI PXIe-5451 was the highest-precision signal source then available in the laboratory. The increased total measurement points were assumed to compensate for the errors; so, 6553600 samples were sampled to get the INL results, shown in Fig. 9(a), by using the histogram-based method. For the proposed method, only a low-precision arbitrary waveform generator Agilent 33250A AWG was used to obtain a low-frequency ramp signal, and 163840 (4096*2*20) samples are used. The nonlinearity became evident at 16-bit level, and the resolution of this signal was much lower than that of the ADC under testing. But, Fig. 9 (b) shows that the INL obtained with the proposed method is closer to that shown in Fig. 9(a) and the maximum estimation error is approximately 5.5LSB. Furthermore, it almost eliminated the impact from the signal source nonlinearity.

Table 1 compares the proposed method and four other earlier representative methods. The histogram-based method requires a test signal of high-resolution and high-linearity for the ADCs, and approximately 32 sampled points per code to measure the static performance. These results confirm that, in the histogram-based method ([3,4,6,7]), the number of samples is much more significant than that of the proposed method, and therefore, the proposed method is quicker than those.

The proposed method is very robust against nonlinearity errors in the stimulus. To obtain the experimental results with imprecise signals, two sets of data were used. The INLs of 13-bit and 16-bit ADCs were estimated with a low-precision signal, repeating the measurement 20 times for averaging the noise effects from the signal source in each testing case, and collected only 163840 measurement points since the employment of the 12-bit resolution signal source. The proposed method reduces the requirements on linearity and resolution of the signal substantially and achieves a significant saving in time. This is achieved by using two simple ramps, one is the attenuating version of the other. This new requirement can be met rather easily by using simple programmable signal generators.

7. Conclusions

This paper proposed and demonstrated a simple and novel method to estimate ADC static characteristics, which is much different from the well-established histogram-based method. The proposed method utilized two sets of testing stimulus, one being an attenuated version of the other,

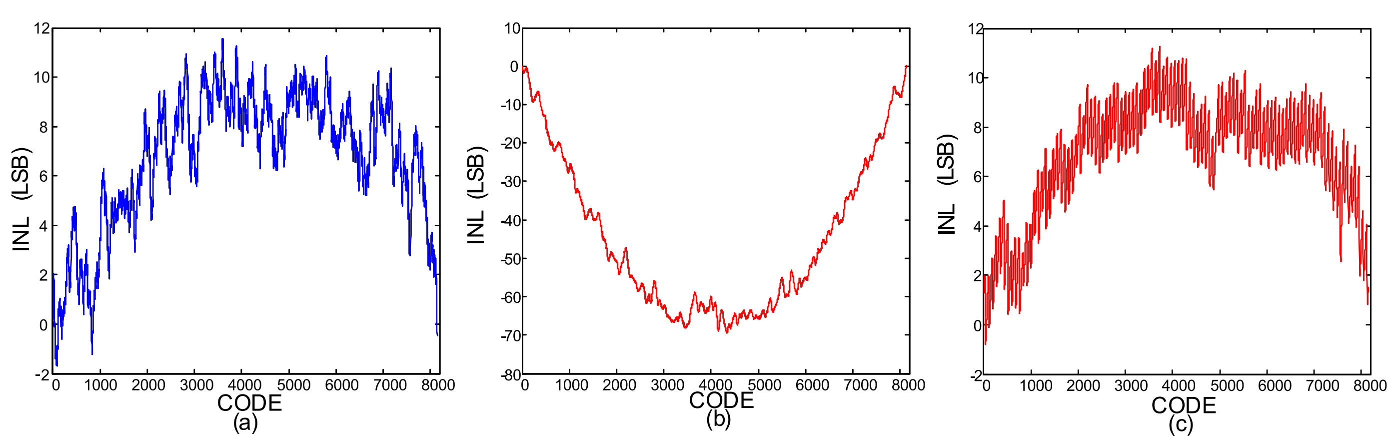

Fig. 8. (a) True INL of DSA 90254 (obtained with the 16b NI PXIe-5451 [18]). (b) INL obtained from the DSA 90254 output code histogram with nonlinearity input. (c) INL using the proposed method obtained in DSA 90254 with nonlinearity input.

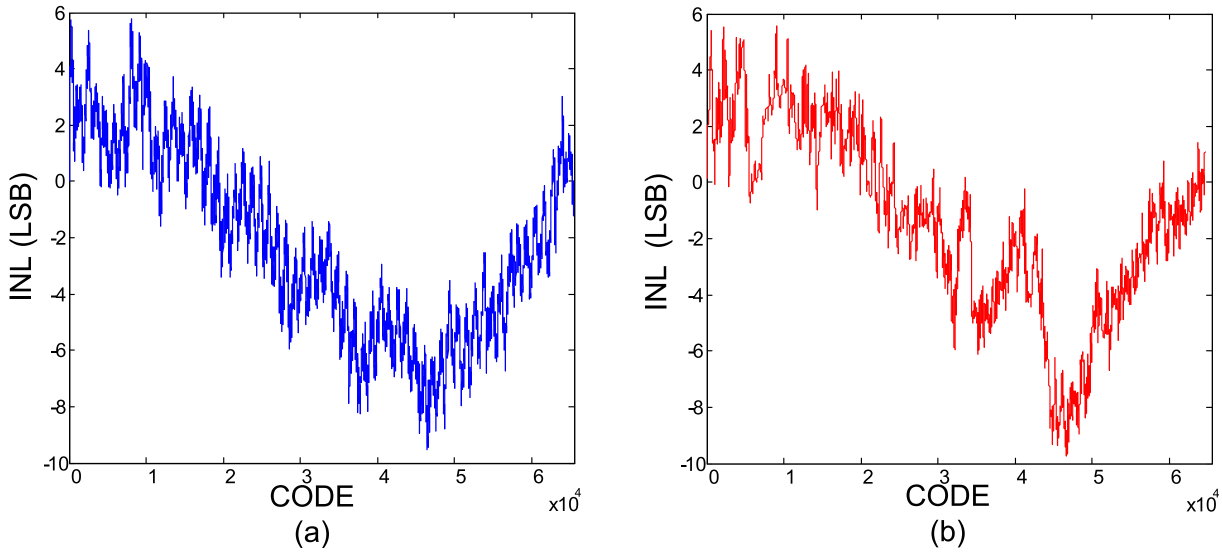

Fig. 9. (a) INL obtained from 9467 CE, using the traditional histogram-based method with 6553600 samples (obtained with 16-bit NI PXIe-5451 [18]) (b) INL obtained from 9467 CE, using the proposed method with nonlinearity input with 163840 samples.

Table 1
Comparison of complexities between the proposed and the other methods.

Parameters	Methods						
	[3]	[4]	[5]	[6,7]	[8]	[9]	Proposed
Input signal source	Digital Sinewave	Low linearity ramp	Low resolution ramp	Low frequency ramp or sinewave	High linearity signal	Low linearity ramp or sinewave, even random input signal	Low linearity and low resolution ramp
Additional sources	A current steering DAC with DDEM control required	DC source required for offset	DC source required for offset	Not required	Not required	DC source required for offset	Not required
Number of samples	Similar to histogram-based method	Similar to histogram-based method	Less than histogram-based method	Similar to histogram-based method	Less than histogram-based method	Less than histogram-based method	Less than histogram-based method

and the method is not sensitive to inaccuracies in the stimulus. The proposed method is practical, reliable and time-efficient, as borne out by simulation and experimental results. The major advantages of the proposed method are that it can achieve a substantial relaxation in linearity and resolution requirements for the test signal source, and reduction in the volume of the test data required for the ADC. Another significant advantage is that it ensures cost-cutting for ADC testing.

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