A 100-MHz BW 72.6-dB-SNDR CT ΔΣ Modulator Utilizing Preliminary Sampling and Quantization

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***Abstract*— This article reports a 4th-order 100-MHz bandwidth continuous-time (CT) delta–sigma modulator in 28-nm CMOS. A preliminary sampling and quantization (PSQ) technique is presented, which allows almost a full utilization of the clock period for the quantization to extend the available conversion time of the backend quantizer (QTZ) under a 0.65 excess loop delay (ELD) coefficient. With the PSQ, both the sampling and quantization of the backend QTZ are splitted into two steps, coarse and fine, similar to the subranging architecture to save power. The QTZ runs at 2 GHz achieving 7 bit (1 b error correction) with only 1.4-mW power. By adding a feedforward ELD compensation path in the cascade of integrators of the cascade of integrators in feedforward (CIFF) topology, only one digital-to-analog converter (DAC) is necessary in this design. The modulator attains a signal bandwidth of 100 MHz with 72.6-dB signal-to-noise and distortion ratio (SNDR) while only consuming 16.3 mW from 1.1- and 1.5-V power supplies. The prototype has a dynamic range of 76.3 dB and a Schreier FoM of 174.2 dB with an active area of 0.019 mm^2.**

***Index Terms*— Analog-to-digital conversion (ADC), continuous-time delta–sigma modulator (CT-DSM), preliminary sampling and quantization (PSQ) technique, successive-approximation-register (SAR) architecture-based quantizer (QTZ), single amplifier biquad (SAB).**

I. Introduction

ADVANCED mobile communication standards, such as fifth-generation new radio (5G NR), call for a receiver analog-to-digital conversion (ADC) with signal bandwidth and dynamic range (DR) over 75-MHz bandwidth and 70 dB, respectively [1]–[4]. In order to prolong the battery lifetime of devices, the architecture of the receiver ADC must be low power. Benefiting from its constant input impedance, continuous-time sigma–delta modulators (CT-DSMs) are a popular choice to relax the input buffer requirement. While under wideband and relative high-DR targets, CT-DSM designs only can experience a low over sampling ratio (OSR), thus asking for a high-order noise-transfer function (NTF). However, the phase delays caused by the high-order loop filter (LF) can easily lead to instability [5], and a large amount of OPAMPs also imposes an energy-inefficient end result. To circumvent such issue, multi-bit quantizers [1]–[3] (QTZs) can be employed but with a penalty on higher power consumption and aggravated linearity.

Under a low OSR and high sampling rate, energy-efficient CT-DSMs often have a higher bit resolution in the backend QTZ rather than higher order in the LF [4]. However, in order to keep its good energy efficiency, such an approach introduces a challenge in the minimization of the loop delay for a longer available QTZ conversion time. In [1], their 3rd-order CT-DSM achieves a 64.9-dB signal-to-noise and distortion ratio (SNDR) and 75-MHz bandwidth, but the OSR is 21.3. Then, the modulator has to run at 3.2 GHz for high bandwidth, which limits the QTZ architecture to flash as well as the QTZ resolution to only 4 b, under a reasonable excess loop delay (ELD). The modulator in [2] maintains a similar bandwidth and SNDR as [1] by increasing the LF order while lowering the OSR and the operation frequency to 13.65 and 2.18 GHz, respectively. Nevertheless, its digital ELD compensation scheme deteriorates both the speed and linearity of the QTZ, thus limiting its flash QTZ to 3 b resolution. In [3] and [4], they both have a reasonable OSR of 10 and a relative high QTZ resolution, 5 and 7 b, respectively. However, in [3], the dedicated low open-loop gain of the amplifier in the LF weakens the in-band (IB) quantization noise suppression ability, thereby alleviating the benefit originated from the high-resolution QTZ. While in [4], even their adopted 7 bit VCO-based QTZ attains a high speed in low power, it necessitates a power-hungry ELD compensation rotator which reduces the overall modulator's energy efficiency.

This design presents a 100-MHz fourth-order CT-DSM with 6 b QTZ. Rather than suffering from the conventional tradeoff between ELD and QTZ conversion time, we propose the preliminary sampling and quantization (PSQ) technique [6]. It allows the backend QTZ to utilize ∼90% of the period for conversion under a 0.65 ELD coefficient, thus enabling a more energy-efficient option for the high-resolution QTZ architecture. A coarse–fine QTZ is used to obtain 7 b with 1 b error correction for the sampling error originated from the PSQ technique. In addition, the ELD compensation is

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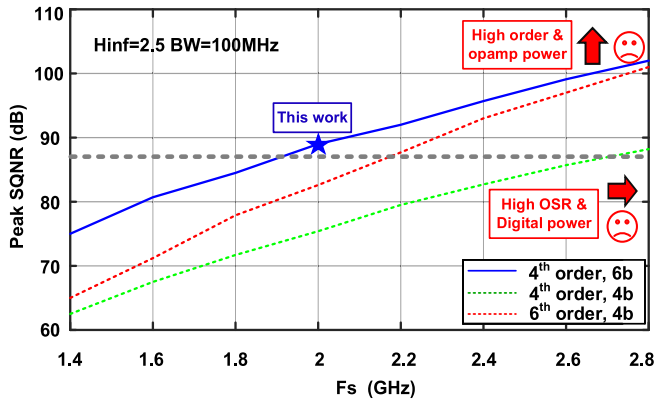


Fig. 1. Peak SQNR versus sampling frequency for different CT ΔΣ modulators.

realized with the feedforward path in the cascade of integrators in feedforward (CIFF) architecture, which avoids the extra multi-bit DAC to save power. Implemented in a 28-nm CMOS process, the prototype exhibits 72.6-dB SNDR with an OSR of 10, consuming only 16.3 mW with 0.019 mm^2 of the active core area.

This article is organized as follows. Section II discusses the tradeoff in the wideband CT-DSM design. Section III presents the architecture of the modulator. Section IV introduces the design considerations of the PSQ technique. Section V shows the circuit implementation. Section VI provides the measurement results, and Section VII provides the conclusion.

II. Energy-Efficient Wideband CT ΔΣ Modulator Design Considerations

A. Tradeoff of LF Order, QTZ Resolution, and OSR

Based on target applications, the required DR of the modulator is ∼75 dB with a bandwidth of ∼100 MHz. In order to provide sufficient margins for device noise and process, voltage, and temperature (PVT) variations, an 87-dB signal-to-quantization-noise ratio (SQNR) is set as the goal in the behavioral evaluation. Fig. 1 shows three possible choices that meet our design target under different OSR, sampling frequency (F_S), and LF order with 2.5 dB maximum NTF out-of-band gain (OBG). They are as follows: 1) 4th-order LF + 6 bit QTZ; 2) 4th-order LF + 4 bit QTZ; and 3) 6th-order LF + 4 bit QTZ. The selection among these three cases involves different tradeoffs in terms of LF stability, QTZ speed, and OPAMP bandwidth, thus eventually affecting the overall energy efficiency. A high LF order (case 3: 6th order) can increase the IB quantization noise attenuation of the modulator but with lower LF stability. Simultaneously, the high order also increases the number of power-hungry OPAMPs in the integrators, thereby leading to a poor energy efficiency. With a high OSR in case 2, both the QTZ and OPAMPs need to run at high speed to ensure a reasonable number of quantization bits and the stability of the modulator, respectively, which significantly increase both the digital and analog power consumptions. Under a wideband target, a higher resolution QTZ becomes a more energy-efficient choice than its high-order counterpart for improving the SQNR. Based on the above analysis, we select case 3 with a 4th-order LF, 6 bit QTZ, and ten OSR in Fig. 2 for its good potential to be energy efficient while targeting to tackle the QTZ speed constraint within this setup. While energy-efficient architectures, such as successive-approximation-register (SAR) [7], [8], cannot run fast enough, the power-hungry flash ADC requires a substantial calibration overhead to handle the offset among the comparators.

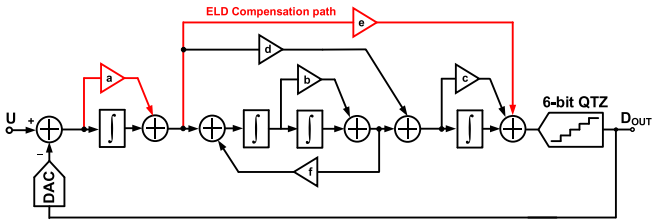


Fig. 2. General structure of the 4th-order CIFF CT ΔΣ modulator.

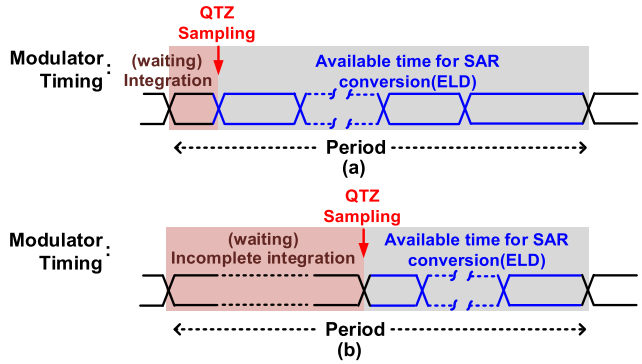


Fig. 3. Timing of the CT ΔΣ modulator with the tradeoff between QTZ available conversion time and LF integration.

B. Backend QTZ Available Conversion Time and Tradeoffs

Rather than just exploring the QTZ architecture as [9]–[13] did, it is important to understand what limits the available conversion time of the QTZ in the first place. Fig. 3(a) and (b) shows two different timing allocations of the modulator in one period. They both consist of two parts which are the LF integration and the QTZ conversion time. In order to leave more time for the QTZ [Fig. 3(a)], a long ELD has to be compensated, which causes the modulator to be easily unstable. In addition, the integration time of the LF becomes short, thus requiring a power-hungry wide bandwidth OPAMP in the integrators. On the other hand, a short ELD [Fig. 3(b)] reduces the available conversion time of the QTZ, but it relaxes the bandwidth requirement of the OPAMPs. In [9] and [14], in order to maintain a good energy efficiency, the later time allocation scheme is usually adopted.

In the allocation shown in Fig. 3(b), the period before the QTZ sampling can be considered as in the process of integration. This is valid as the designed ELD and timing margin for the integration is sufficient to maintain the loop in a stable condition. Therefore, the LF output, which is the QTZ input, within this period can be indicated by the following equation [11]:

$$\mathrm{QTZ_{IN}} \propto \mathrm{STF} \cdot \mathrm{IN} + (\mathrm{NTF} - 1) \cdot Q_E. \quad (1)$$

During this incomplete integration period, the variation of the QTZ input is mainly determined by: 1) the input signal (IN) of the modulator modulated by the signal transfer function (STF) and 2) the noise-shaped quantization noise (Q_E). With the OSR in the modulator, F_s is 2 × OSR fold of the input signal bandwidth, which ensures that the variation of the input signal is relatively small during one period of the modulator. In addition, the remaining time of the integration process is (1-ELD) × T_s when considering the ELD. Then, the variation of the IN is further suppressed with a factor of ∼(1-ELD). On the other hand, the quantization noise affects the variation of the QTZ_{IN} after the noise shaping and is proportional to the LSB/2 of the QTZ. As discussed before, in wideband designs, a moderate-resolution QTZ is often necessary for energy efficiency. With ≥5 number of bits in the QTZ, the small LSB also limits the variation of the QTZ_{IN} within the incomplete integration period. In this design, with 6 bit QTZ, 0.65 ELD coefficient, ten OSR, and a 100-MHz bandwidth input signal, the voltage swing of the QTZ_{IN} is smaller than 175 mV during the incomplete integration. It is worth referring that there is still input information within such period, and a certain amount of extra quantization can be extracted as long as the incomplete integration error can be covered later in the final feedback.

C. ELD Realization Consideration

One of the most common solutions for ELD compensation is to add an extra feedback DAC which is often placed at the input rather than the output of the last integrator to avoid the additional analog adder [15]. However, when a moderate resolution QTZ is used, the ELD multi-bit DAC increases the parallel bit routings, thus eventually inducing extra area, delay, and digital power from the bit data buffering. On the other hand, with the VCO-based QTZ in [4], the compensation can be realized by a rotator, which, however, consumes almost a 1.5-fold power of the whole LF. In [9] and [16], the ELD compensation is realized in the DAC of the SAR QTZ while its input swing is attenuated by half. It requires not only an extra phase but also an additional gate/multiplier logic in each SA bit cycling to inject the compensation codes to the DAC. Along with the attenuated input swing, the overall timing overhead can be in several tens of picoseconds even in advanced technology nodes. Another solution for the ELD compensation is the addition of a feedforward path from the input to the output of the LF. This ELD compensation method avoids an extra DAC and reduces the bit routings. Specifically, at least half parallel bit routing and an extra fan-out in the critical path can be saved in the design. When comparing with the ELD DAC solution, as the ELD path in the feedforward compensation passes the first integrator, it adds extra loads. However, such loading is proportional to the last integrator which is relatively small when compared with the load of the first integrator.

III. CT ΔΣ Modulator Architecture

Fig. 4 shows the selected 4th-order CT ΔΣ modulator architecture. The modulator runs at 2 GHz with a bandwidth of 100 MHz experiencing ten OSR. We choose the cascade of integrators in feedforward (CIFF), as it requires no extra DACs in the modulator for feedback and ELD compensation and the best noise suppression of the succeeding integrators [17]. It also reduces the output swing of the first integrator, which can relax the linearity requirement of the first OPAMP in the LF. However, compared with cascaded integrator with distributed feedback (CIFB) architecture, The CIFF requires extra low-pass filter to alleviate the high STF peaking. The modulator achieves a 4th-order LF with three OPAMPs, and one of the OPAMPs is used as a single amplifier biquad (SAB) integrator to achieve a 2nd-order transfer function which reduces the power and the phase delay of the LF [5], [7]. The SAB integrator also introduces a notch in the NTF to improve the SQNR, which is effective in the low OSR CT-DSM designs.

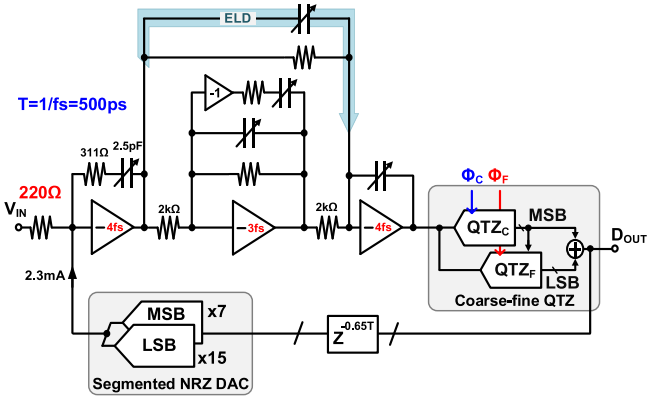


Fig. 4. Block diagram of the proposed 4th-order CT ΔΣ modulator with the coarse–fine QTZ.

The proposed CT-DSM employs the PSQ scheme for additional quantization from the QTZ backend, which runs at 2 GHz with 6 bit resolution and utilizes almost 90% of the clock period. The QTZ of the modulator consists of a 3 bit two-step coarse QTZ and a 4 bit SAR fine QTZ with 1 bit error correction range. As discussed in Section II-C, in order to avoid the extra power and latency introduced by the ELD DAC, we adopt a feedforward scheme. The ELD compensation path is shown in Fig. 4, which includes the first and last integrator. The LF realizes the constant term in the ELD compensation path equivalently acting as an active adder for the ELD compensation scheme [15]. Such ELD realization requires a sufficient high impulse-response speed in the modulator, whereas inadequate speed leads to out-of-band (OB) peaking in the frequency domain and even instability [3]. In this design, the unity-gain bandwidth (UGBW) of the first and last OPAMPs is designed to be higher than the second one with $4F_S$ (detailed in Section IV), and the ELD coefficient is also overdesigned, which ensures the stability with high impulse-response speed.

The process variation of the *RC* integrator is compensated by the 3 bit digital tuning capacitors, covering ±25%-time constant variation. We adopted the non-return-to zero (NRZ) current-steering DAC and segmented structure [4] to reduce the clock jitter sensitivity [18] and the power as well as the area of the feedback DAC, respectively. The DAC mismatch between the segment and the unit element is calibrated in

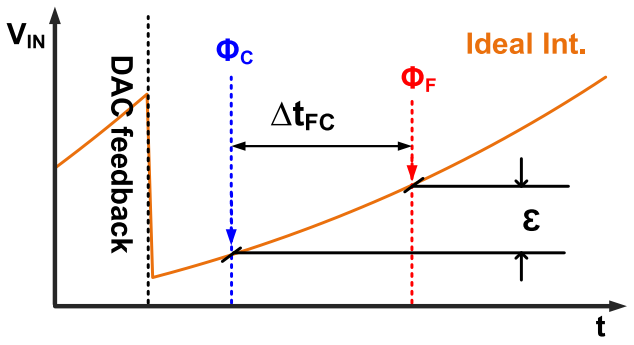


Fig. 5. Sample timing of the proposed coarse–fine QTZ with the PSQ technique.

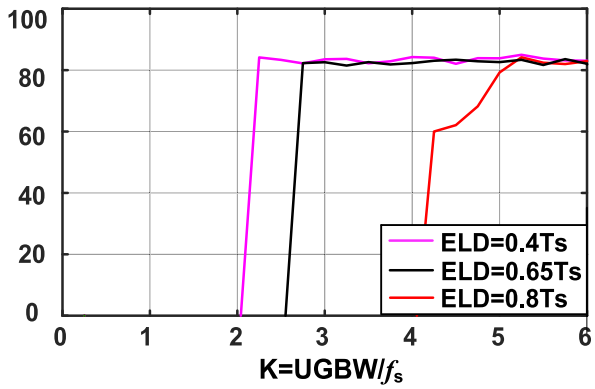


Fig. 6. Peak SQNR versus the bandwidth of the OPAMP with different delays for the ELD compensation in the LF.

the digital domain [19]. The calibration [20] involves three steps: first, the DAC unit cell mismatch error is evaluated in an offline procedure; second, the evaluated DAC error is frozen and digitally stored in the look-up table (LUT); finally, a summation in digital domain is performed that corrects the output by the evaluated DAC error stored in the LUT. Based on the SNDR and spurious-free DR (SFDR) target, a total number of 13 b final output code is necessary to fulfill the accuracy. The estimated total power and area of the calibration including memory are ∼1.4 mW and ∼0.008 mm^2, respectively, with the adopted technology node. Under the temperature variation with long-channel device, as both the threshold and current factor mismatches only have a weak dependence on the temperature [20], the temperature-originated mismatch variation is mainly caused by g_m/I_d, where g_m and I_d are the transconductance and drain current of MOSFET in the unit current cell, respectively. The simulation results based on the setup and sizing of this design show that such a variation leads to a one sigma mismatch of ∼0.05% from −20 °C to 80 °C range after calibrated at 27 °C while that is still within the target requirement.

The noise requirement determines the value of the input resistor ($R1$), which simultaneously decides the consumed current of the main DAC and the capacitance load of the first integrator, thus implying that the value of $R1$ induces a tradeoff between the noise and power of the DAC as well as the OPAMP in the first integrator. In this design, the target SNR is ∼77 dB, where the SQNR has around 10-dB margin. Based on such goal, R and C values are 220 Ω and 2.5 pF, respectively, for the first integrator. Thus, C_{DAC} dissipated ∼2.3 mA.

IV. Preliminary Sampling and Quantization

A. PSQ Technique and Sample Error

As discussed in Section II-C, there is also input information during the incomplete integration period of the LF. When with moderate OSR and number of quantization in the backend QTZ, the swing variation of the QTZ input signal is limited. Therefore, it is possible to resolve several more coarse bits during such a period where the error can still be covered in the fine quantization. Under this circumstance, the conversion time of the QTZ can be extended while simultaneously keeping a reasonable ELD coefficient for the energy efficient target. Fig. 5 shows the QTZ input and the PSQ coarse–fine sample timing. The coarse QTZ samples and quantizes at the time between the fine QTZ sampling and the DAC feedback instant to obtain extra quantization bits. It can be recognized that there is a time difference Δt_{FC} between the coarse and fine QTZ sampling instants, which lead to a sampling error ($\varepsilon_{\mathrm{SAM}}$). In order to alleviate $\varepsilon_{\mathrm{SAM}}$, the coarse sampling instant should be placed as close as possible to the fine one, which, however, leads to a short available time for the coarse QTZ. Therefore, there is a tradeoff between the amount of $\varepsilon_{\mathrm{SAM}}$ and the extra quantization that can be given in the coarse QTZ. Apart from Δt_{FC}, the modulator OBG, the LF frequency response, the input variation, and the resolution of the QTZ, all affect $\varepsilon_{\mathrm{SAM}}$. Its correction scheme and other design considerations will be discussed next.

B. PSQ Technique Design Considerations

The considerations of the fine sampling instant in the PSQ technique are similar to other conventional techniques. As the ELD compensation is realized by the CIFF architecture in this article, the fine sampling instant is bounded by the tradeoff among the fine QTZ conversation time, the stability, and the power consumption of the LF. Fig. 6 shows the relation between the SQNR of the modulator and the OPAMP bandwidth in the LF, with different choices of the ELD coefficient, and it also indicates the stability condition. Furthermore, since the fine QTZ has to cover the sampling error, its correction range also needs to be considered. For instance, when the ELD coefficient is $0.4T_S$, the LF requires OPAMPs with $2F_s$ UGBW in order to keep the modulator stable. With around ∼80 ps one SAR cycle and F_s of 2 GHz in our design, the 0.4 T_s ELD only allows 2 b conversion in the fine SAR QTZ, implying that the remaining 4 bits must resolve during the coarse QTZ. Under this condition, the fine QTZ only can provide a small correction range for the sampling error that eventually limits the coarse sampling instant location and reduces the robustness of the PSQ technique. On the other hand, with a $0.8T_s$ ELD coefficient, a power-hungry wide bandwidth OPAMP is necessary that obviously is not a good choice for an energy-efficient target. In the last case with $0.65T_s$ ELD, the modulator allows 4 bits fine QTZ with 1 b error correction, covering a 175-mV error range.

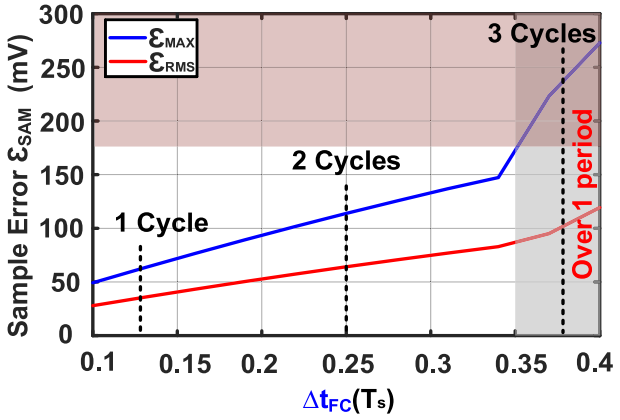


Fig. 7. RMS ($\varepsilon_{\rm rms}$) and max ($\varepsilon_{\rm max}$) sample error versus the different $\Delta t_{\rm fc}$, the time between the coarse and fine sample.

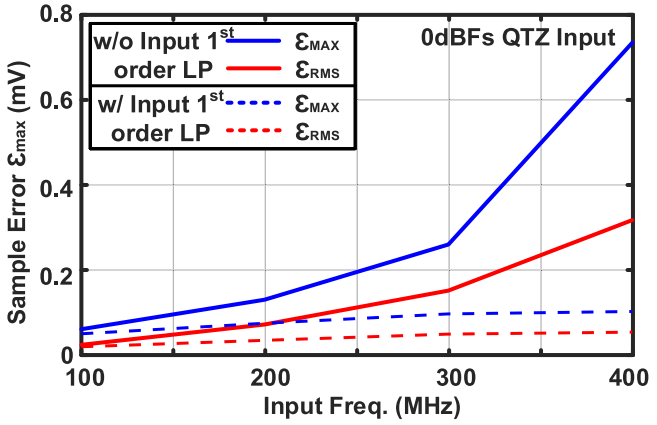


Fig. 8. Sample error versus the input signal frequency with/without 1st-order low-pass filter.

Fig. 7 shows the relation between the sampling error and $\Delta t_{\rm CF}$ in our design. It can be noticed that a shorter $\Delta t_{\rm FC}$ leads to a smaller sample error but with less available time for the coarse quantization. When $\Delta t_{\rm fc} = 0.125T_S$, it has a small sampling error but only allows 1 SAR cycle conversion (~80 ps) in the coarse ADC. With only 1 cycle available time but 3 b quantization, the only possible architecture is the flash which requires seven comparators with offset calibrations and a ladder with static current. As a consequence, the QTZ will occupy a large area subsequently limiting the modulator speed. On the other hand, with a two-cycle available time, a subranging architecture can be adopted to save power and calibration overhead from the pure flash architecture. In the three-cycle case, not only the timing is over $1T_s$ but also the sampling error is over the possible correction range. According to all abovementioned considerations, we picked, in this design, a $0.65T_s$ ELD with $\Delta t_{\rm FC}$ of 0.25.

In the wireless communication system, both conventional and PSQ QTZ can be saturated by the large OB blocker under the same STF. However, the PSQ induces one more concern from the sampling error. In this design, the sampling error (RMS value) exceeds the correction range of the fine stage with >300 MHz and 0 dB F_s blocker signal. However, with a simple first-order loop-pass (LP) filter, the QTZ keeps stable within all frequencies as shown in Fig. 8. The LP filter limits blocker signal's amplitude at high frequency that ensures the sampling error within the dedicated correction range of the fine QTZ. Therefore, in order to tolerate the OB blocker, the overhead is an LP filter which is often available from the ADC driver.

C. Response of the LF

In our CIFF DSM, the ELD is compensated by the feedforward path in the LF, as already shown in Fig. 4. During the DAC feedback, the LF experiences a step-response-like input. Restricted by the finite OPAMPs' bandwidth in the LF, the output deviates from its ideal value but eventually converges when the response becomes moderate during input tracking. As shown in Fig. 9, when compared with the ideal case, the response of the LF in the CT-DSM consists of two

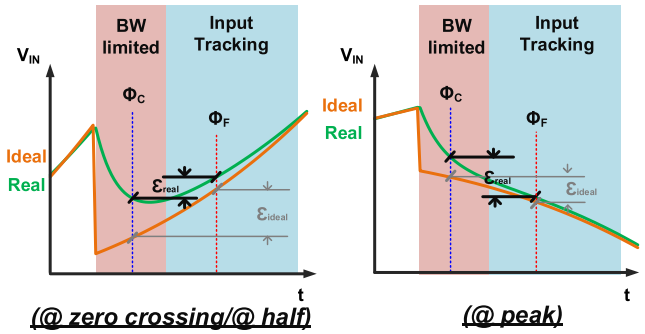


Fig. 9. Output of the LF with ideal and real integrator in the zero crossing, half, and peak of the sine wave, respectively.

parts. The first is the BW limited region, where the output of the LF is mainly dependent on the step-response ability of the LF, thus leading to a different $\varepsilon_{\rm SAM}$ between ideal and real responses. The second is the input tracking, where the output is mainly dependent on the transfer function of the LF. In the BW limited region, the sample error $\varepsilon_{\rm SAM}$ of the LF with $0.25T_s\,\Delta t_{\rm fc}$ can be expressed as follows:

$$\varepsilon \propto D_{\rm out}(1-z^{-1})\left(e^{-t/\tau} - e^{-(t+0.25T_s)/\tau}\right) \tag{2}$$

where $D_{\rm out}(1-z^{-1})$ represents the difference between two sequence output codes. In our CIFF topology, the output of the LF is directly affected by $D_{\rm out}(1-Z^{-1})$ through the ELD compensation path, which is similar to the switched-capacitor integrator. Therefore, the second part of (2) is the difference between two instants under the switched-capacitor response, where τ is the time constant of the LF that is inversely proportional to the bandwidth of the OPAMP in the LF. Finally, (2) indicates the total difference between two instants of the LF output, which is the sampling error in the proposed PSQ technique.

Furthermore, the sample error is also affected by the slope and the polarity of the input signal. Next, we use a sinusoidal input as an example to show their influence. The response of the LF leads to different $\varepsilon_{\rm SAM}$ when the input is at the peak and zero crossing. As shown in Fig. 9(a), at zero crossing, the response polarity is reversed between the BW limited and

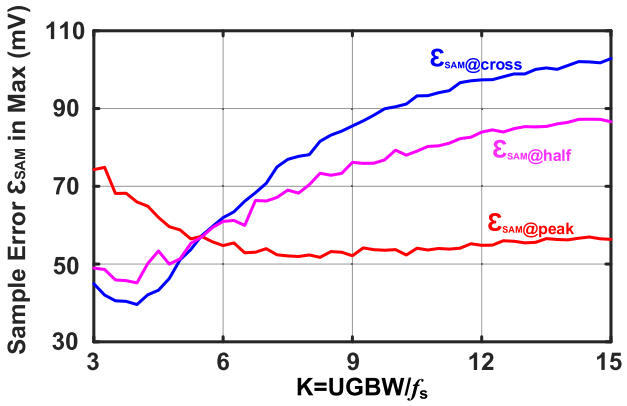


Fig. 10. Maximum sample error versus the bandwidth of the OPAMP in the zero crossing, half, and peak of the sine wave, respectively.

the input tracking regions. Then, $\varepsilon_{\mathrm{SAM}}$ caused by the input variation and the LF finite response counteracts with each other which can be indicated by the following equation:

$$\varepsilon_{\mathrm{SAM@cross}} \propto |\varepsilon_{\mathrm{input}}| - \left|D_{\mathrm{out}}(1-z^{-1})\left(e^{-t/\tau} - e^{-(t+0.25T_s)/\tau}\right)\right| \tag{3}$$

where the error from the input variation ($\varepsilon_{\mathrm{input}}$) is subtracted of the LF response. Compared with the ideal integrator, the real LF experiences a smaller $\varepsilon_{\mathrm{SAM}}$ under this condition. This trend can also be confirmed by the behavioral simulation results of Fig. 10. As the OPAMP bandwidth is proportional to τ, we plot the sampling error versus the bandwidth which generalizes the required OPAMPs' bandwidth consideration. As shown, $\varepsilon_{\mathrm{SAM@cross}}$ increases with the OPAMP bandwidth and becomes closer to the ideal integrator condition. $\varepsilon_{\mathrm{SAM@cross}}$ is almost saturated when the UGBW of the OPAMP is close to $15F_s$, but the minimum $\varepsilon_{\mathrm{SAM@cross}}$ appears when the UGBW of the OPAMP is $\sim$3–4F_s. Fig. 10 also shows the sampling error of the intermedia cases when the input of the QTZ is close to the 1/4 or 3/4 location of the sine wave ($\varepsilon_{\mathrm{SAM@half}}$). Its originated sampling error is bounded between the zero-crossing and peak conditions. Indeed, the signal behavior of the half-value case is similar to the zero-crossing one, as shown in Fig. 9(a), but with different amount of errors induced from the input-dependent part ($\varepsilon_{\mathrm{input}}$).

On the other hand, as shown in Fig. 9(b), the response polarity is the same between the BW limited and input tracking region at the peak. Then, $\varepsilon_{\mathrm{SAM}}$ caused by the input variation and the LF finite response accumulates which can be expressed as follows:

$$\varepsilon_{\mathrm{SAM@peak}} \propto |\varepsilon_{\mathrm{input}}| + \left|D_{\mathrm{out}}(1-z^{-1})\left(e^{-t/\tau} - e^{-(t+0.25T_s)/\tau}\right)\right| \tag{4}$$

where $\varepsilon_{\mathrm{input}}$ adds to the LF response error. Compared with the ideal integrator, the real LF experiences a larger $\varepsilon_{\mathrm{SAM@peak}}$ under this condition. While it is similar with the zero-crossing condition, as the bandwidth of the OPAMP increases, $\varepsilon_{\mathrm{SAM@peak}}$ also gets closer to the ideal integrator response, as shown in Fig. 10. $\varepsilon_{\mathrm{SAM@peak}}$ is at its minimum value when the UGBW of the OPAMP is $>6F_s$. Based on the above analysis, since $\varepsilon_{\mathrm{SAM@cross}}$ and $\varepsilon_{\mathrm{SAM@peak}}$ have different characteristics versus the integrator bandwidth, both errors need to be considered. In this design, we choose a $4F_s$ UGBW to balance $\varepsilon_{\mathrm{SAM}}$ and OPAMP power with a margin for stability.

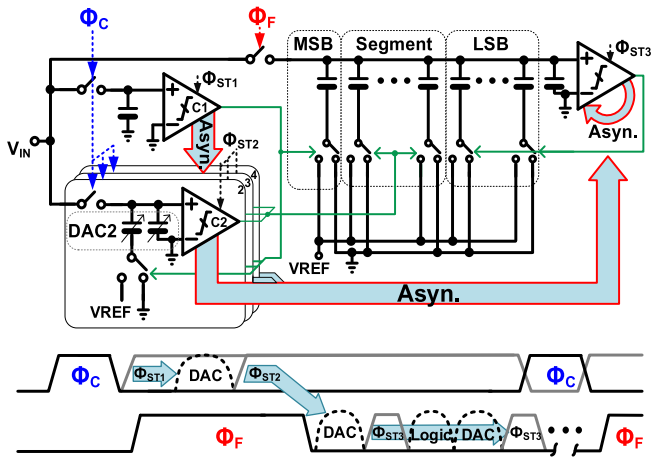


Fig. 11. Block diagram of the 6 bit coarse–fine QTZ and timing.

V. Circuit Implementation

A. Coarse–Fine QTZ With PSQ Technique

Fig. 11 shows the simplified schematic of the QTZ in a single-ended configuration while the actual design is differential. The coarse QTZ, indeed, is a subranging architecture where the MSB is resolved directly with the comparator C1 at Φ_{ST1} after the coarse sampling Φ_C. The decision from C1 then controls the bottom-plate switch of the capacitance ratio-adjusted DAC2-4 that generates the reference voltages for C2-4. C2-4 is triggered at Φ_{ST2} which leads to 2 more bit decisions and then together with the result from C1 will be fed to the segmented DAC of the fine SAR ADC. Finally, the fine QTZ resolves the remaining 4 bits while the fine sampling Φ_{F} is conducted during the coarse QTZ conversion. In this design, all the propagations on the comparators' decisions between subranging coarse and coarse-to-fine do not require any decoding logic and extra latch circuit, thus ensuring a high-speed operation. The conversion of the coarse QTZ takes about $0.25T_s$ (125 ps), which benefits from the direct control strategy, the small DACs (3 fF unit), and the common-mode shifting operation.

The input common-mode voltage of the second stage of the coarse QTZ and fine QTZ ($V_{\mathrm{cm,in}}$) is shifted from an initial value of 500–700 mV to speed up the whole quantization process. The level shift is implemented by the switched-capacitor shifter where certain parts of the sample capacitor are used as the shifting capacitors. In the sample period of the coarse QTZ, the bottom plate of the second stage shifter capacitors is connected to the ground. When the sampling finishes and the first stage is comparing, the bottom plate is connected to the power supply of the QTZ to shift $V_{\mathrm{cm,in}}$ of the QTZ. In the fine QTZ, during the sample, the bottom plate of the MSB DAC is connected to the ground. When the MSB DAC is switched based on the coarse data, a part of the MSB DAC bottom switches is connected to the power supply to rise $V_{\mathrm{cm,in}}$.

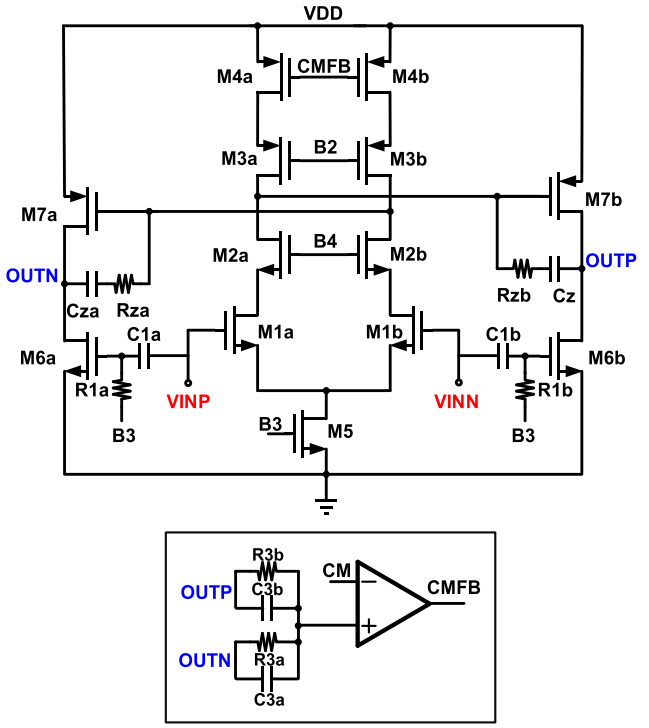


Fig. 12. Two-stage feedforward OPAMP.

The offset of the comparators in the first stage is calibrated in the foreground to a 4 bit level through an extra pair adjustment [21] in the comparator, where the residual error is addressed by the redundancy in the fine QTZ. With the multi-step QTZ architecture, metastability from the QTZ is a concern. In order to avoid a large error magnitude caused by the metastability, asynchronous clocking scheme is adopted. The whole conversion is running in an asynchronous manner while the first comparison (C1) of the fine SAR ADC is triggered until all decisions of C2-4 are ready. Noted that with small error magnitude, the metastability error can be tolerated, and the LF can be recovered within a few cycles. On the other hand, a large metastable error magnitude easily causes the modulator being unstable. As all the comparators' clock signals are propagated in an asynchronous manner, it greatly reduces the error rate of the large magnitude metstability error. In addition, the time constant of the comparators is also improved by the common-mode shifting scheme. The conversion time of the fine QTZ is close to $0.65T_s$ (325 ps) as we adopt a small DAC (9.6 fF) and dynamic logics. The input swing of the QTZ is $1.4V_{\text{pp}}$, which is also the output swing of the last OPAMP. The LSB of the fine SAR QTZ is about 22 mV. The coarse and fine QTZ take about 125 and 325 ps, respectively, which in total utilizes about 90% of T_s. Benefitting from the PSQ technique, the extra coarse conversion contributes around 12 dB effective additional SQNR with only small power and area overhead. As a result, a 7 bit subranging ADC with 6 b effective resolution can run in 2 GHz while only consuming ~1.4 mW power.

B. Two-Stage Feedforward Miller Compensation OPAMP

Fig. 12 shows the OPAMP adopted in the first integrator. A two-stage topology is utilized with feedforward path and Miller compensation techniques [14], [22] due to its outstanding power efficiency in the wideband specification. The first stage of the OPAMP is with a telescopic architecture to ensure a high dc gain. A feedforward path from the input (VIN) to M6a/b and M5 is inserted, where VIN is ac coupled to M6 through C1, to push the UGBW of the OPAMP close to the ideal two-stage OPAMP. The dc bias of the M6a/b and M5 is supplied by the same bias circuit, and the W/L of M6a/b and M5 matches with each other, which is similar to current mirror circuits. In such a way, M5 and M6 can be tracked under PVT variations. The second stage OPAMP exhibits a Class-AB-like topology that is chosen to supply enough output headroom and linearity to the OPAMP. In wideband OPAMP designs, the speed of the common-mode feedback (CMFB) is also critical; therefore, a pair of parallel resistors (R2a/b) and capacitors (C2a/b) are connected to the output of the OPAMP to detect the common voltage, and the CMFB circuit controls M4 to boost the CMFB bandwidth by introducing a zero in the feedback loop. The UGBW of the OPAMP is 7.6 GHz, and it consumes about 5.3 mW.

C. Segmented Feedback DACs

In order to alleviate the power, area, and routing overhead, we reduce the number of unit cells and drivers in the 7 b DAC by utilized a segmented scheme. The DAC is segmented into 3 bit MSB and 4 bit LSB, which matches with the bit arrangement in the coarse–fine QTZ to avoid the extra decoder for high speed. The unit cell of the MSB and LSB DACs has different size that saves 56 DAC drivers comparing with only single LSB unit cell design. An NRZ DAC is necessary to suppress the jitter sensitivity which is critical as the design is targeting a 100-MHz bandwidth. Fig. 13 shows the circuit schematic of the adopted DAC cell, where the MSB and LSB segments use the same architecture and work under a 1.5-V power supply for a better noise performance. For a high output impedance, a cascaded current source structure is used to maintain a more stable voltage at the virtual ground of the OPAMP. The parasitic capacitance of A and B is small due to the small sizing unit cell that alleviates the dynamic error of the DAC. The low-pass filters, R1a/b and C1a/b, suppress the thermal noise as well as high interferences.

VI. Measurement Results

The CT $\Delta\Sigma$ modulator is realized in 28-nm CMOS which has an active area of 0.19 mm^2 as shown in Fig. 14. The power supply of the QTZ is 1.1 V and the NRZ DAC is 1.5-V supply for the low noise considerations. The other parts are working under a 1-V supply. The sampling frequency of the modulator is 2 GHz with 10 OSR. The $0.65T_s$ ELD and $0.25T_s$ are realized by inverters' delay, which vary under PVT. In this design, we make only the fine sampling instant tunable for the best speed performance. The bandwidth is 100 MHz. Fig. 15 shows the output spectrum of the modulator with a -2 dBF_S, $1.4V_{\text{pp}}$ single-tone signal at ~18 MHz input frequency. The SNDR, SNR, and SFDR are 72.6, 73.2, and 83.6 dB, respectively, after the DAC mismatch calibration [19].

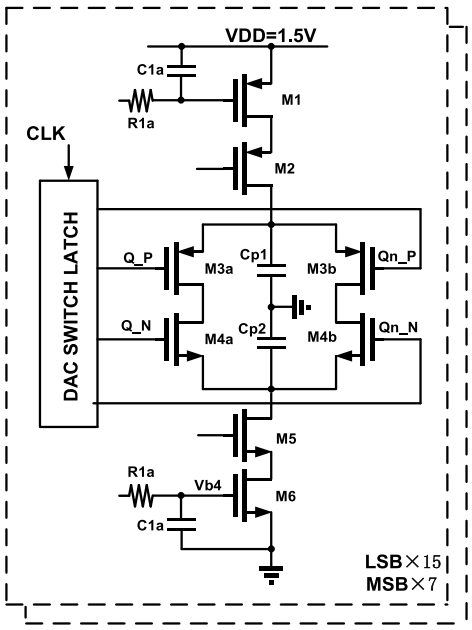


Fig. 13. DAC cell.

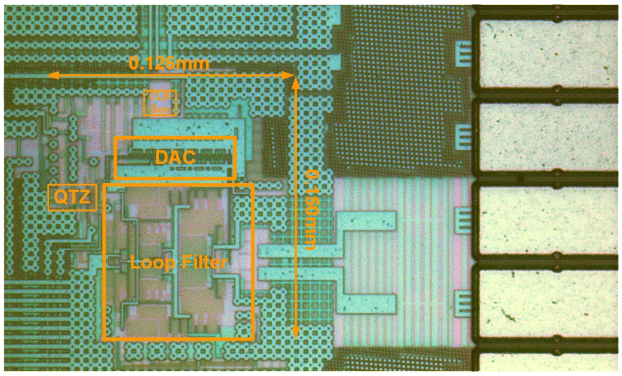


Fig. 14. Die photograph.

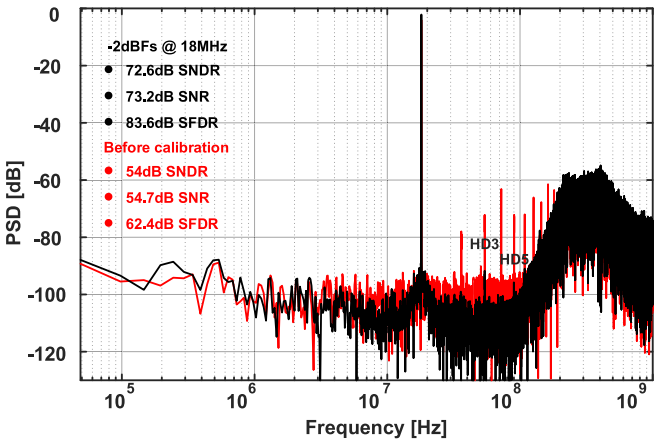


Fig. 15. Single-tone output spectrum.

The 80 dB/decade spectral slope validates the 4th-order noise shaping realized by the SAB and two conventional integrators.

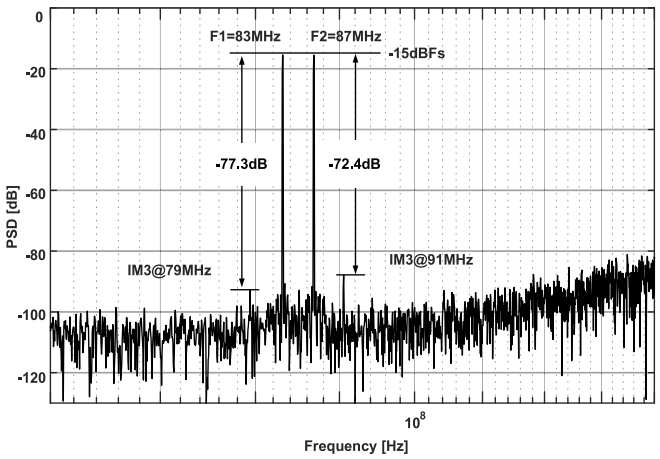


Fig. 16. Two-tone IMD.

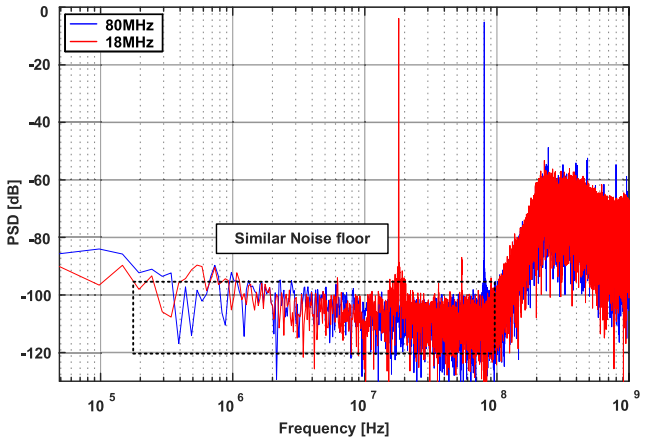


Fig. 17. Measured spectra 18 MHz versus 80-MHz input.

Fig. 16 shows the two-tone intermodulation distortion (IMD) measurement results. The input signal frequency is ∼83 and 87 MHz with ∼ −15 dBF_s and their corresponding IMD3 is 77.3 and 72.4 dB, respectively. It is worth noting that other measured samples show a less than 3 dB variation on the IMD3 with a full swing two-tone test case. Fig. 17 shows the comparison of the fast Fourier transforms (FFTs) of the modulator with 18- and 80-MHz input. They both have a similar noise floor due to the enough error correction range left in the fine QTZ. Fig. 18 shows the measured SNR/SNDR versus the input amplitude. The proposed design obtains a DR of 76.3 dB with 18-MHz input signal. Fig. 19 shows the measured STF of our modulator, and the maximum peaking is around 11.7 dB at around 230 MHz which is caused by the adopted CIFF architecture.

Fig. 20 shows the measured power consumption breakdown of the modulator. The total power consumption is 16.3 mW composed of 4.4 and 14.3 mW from the analog and digital circuits, respectively. The analog part comprises the OPAMPs, DAC, and QTZ, and the digital part includes the clock generator, the logic buffer, and control circuits. The first OPAMP consumes the largest power due to its strength thermal noise requirement with the heavy load. While the second OPAMP

TABLE I
SUMMARY OF PERFORMANCE AND BENCHMARK WITH STATE OF THE ART

	Huang ISSCC 2017[4]	Wu JSSC 2016[8]	Wu ISSCC 2016[3]	Ho JSSC 2015[2]	Bolatkale JSSC 2011[23]	This work
Area (mm^2)	0.217	0.16	0.155	0.1	0.9	0.019
Technology (nm)	16	65	16	20	45	28
OSR	8.6	10	9	13.7	16	10
Fs (GHz)	2.15	0.9	2.88	2.184	4	2
Bandwidth (MHz)	125	45	160	80	125	100
Power (mW)	54	24.7	40	23	256	16.3
Peak SNDR (dB)	71.9	75.3	65.33	67.5	65	72.6
DR (dB)	74.8	82.5	72.1	73	70	76.3
FOMSch/SNDR (dB)	165.7	167.9	161.4	162.9	151.9	170.5/170.1*
FOMSch/DR (dB)	168.4	175.1	168.1	168.4	156.9	174.2/173.8*
FoMWa (fJ/conv.step)	67.2	57.7	82.8	74.2	704.7	23.4/25.4*
STF peak	Yes	Yes(9.1dB)	Yes	Yes	Yes	Yes(11.7dB)

*Included the estimated power of the DAC calibration (1.4mW)

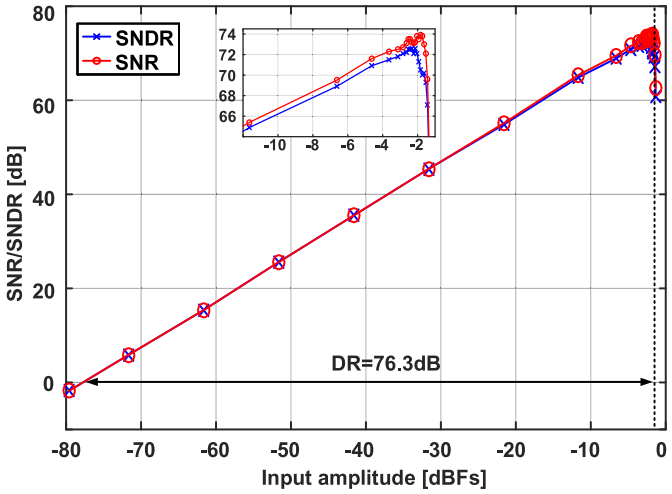


Fig. 18. Measured SNDR and SNR versus input amplitude.

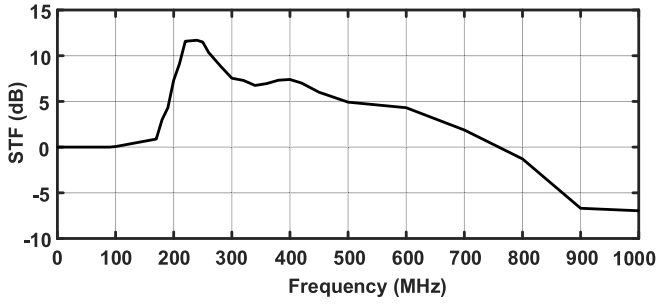


Fig. 19. Measured STF.

should maintain enough bandwidth for the notch of the NTF that causes influence on the SQNR on the low OSR design, it together with the last OPAMP has a relatively smaller power

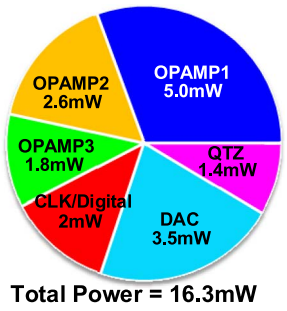


Fig. 20. Power breakdown.

benefiting from their smaller load. The power consumption of the 7 b, 2 GS/s coarse–fine QTZ is 1.4 mW which is only 8.6% of the total, benefiting from the PSQ technique-based two-step QTZ. The SAR directly uses the supply and ground as references; therefore, no reference buffer is adopted in this design, and its power is included in the breakdown of the QTZ power. Table I shows the measured performance and compares this article with state-of-the-art CT $\Delta\Sigma$ designs with similar BW and SNDR. The modulator achieves a peak SNDR of 72.6 dB and a DR of 76.2 dB, resulting in an excellent Schreier FoM 170.5 dB (SNDR) or 174.2 dB (DR) and a Walden FoM 23.4 fJ/conversion step.

VII. CONCLUSION

This article presented a 4th-order CT $\Delta\Sigma$ modulator with PSQ. It allowed a small area and power-efficient modulator architecture with coarse–fine QTZ. The coarse–fine QTZ realized a 7 bit with 1 bit error correction range running at 2 GHz but consuming only about 1.4 mW. This article also discussed the influence of sample error between the coarse QTZ and fine QTZ and presented the design considerations of the coarse and

fine sampling instant. Moreover, in order to improve the power efficiency of the OPAMPs and address the jitter and power in the DAC, it used the SAB integrator and segment 3-4 NRZ DAC in the modulator. These techniques implemented in a CT ΔΣ modulator led to an SNDR of 72.6 dB and a Schreier FoM of 170.5 dB with 100-MHz signal bandwidth.

REFERENCES

[1] C. Briseno-Vidrios, A. Edward, A. Shafik, S. Palermo, and J. Silva-Martinez, "A 75-MHz continuous-time sigma-delta modulator employing a broadband low-power highly efficient common-gate summing stage," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 657–668, Mar. 2017.

[2] S. Ho, C.-L. Lo, J. Ru, and J. Zhao, "A 23 mW, 73 dB dynamic range, 80 MHz BW continuous-time delta-sigma modulator in 20 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 908–919, Apr. 2015.

[3] S. Wu, T. Kao, Z. Lee, P. Chen, and J. Tsai, "A 160 MHz-BW 72 dB-DR 40 mW continuous-time ΔΣ modulator in 16 nm CMOS with analog ISI-reduction technique," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Jan./Feb. 2016, pp. 280–281.

[4] S. Huang, N. Egan, D. Kesharwani, F. Opteynde, and M. Ashburn, "A 125 MHz-BW 71.9 dB-SNDR VCO-based CT ΔΣ ADC with segmented phase-domain ELD compensation in 16 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. (ISSCC) Tech. Papers*, San Francisco, CA, USA, Feb. 2017, pp. 470–471.

[5] R. Zanbaghi *et al.*, "An 80-dB DR, 7.2-MHz bandwidth single opamp biquad based CT ΔΣ modulator dissipating 13.7-mW," in *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 487–501, Feb. 2013.

[6] W. Wang, C. Chan, Y. Zhu, and R. P. Martins, "A 72.6 dB-SNDR 100 MHz-BW 16.36 mW CTDSM with preliminary sampling and quantization scheme in backend subranging QTZ," in *IEEE Int. Solid-State Circuits Conf. Dig. (ISSCC) Tech. Papers*, San Francisco, CA, USA, Feb. 2019, pp. 340–342.

[7] W. Wang, Y. Zhu, C. Chan, and R. P. Martins, "A 5.35-mW 10-MHz single-opamp third-order CT ΔΣ modulator with CTC amplifier and adaptive latch DAC driver in 65-nm CMOS," in *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 2783–2794, Oct. 2018.

[8] B. Wu, S. Zhu, B. Xu, and Y. Chiu, "A 24.7 mW 65 nm CMOS SAR-assisted CT ΔΣ modulator with second-order noise coupling achieving 45 MHz bandwidth and 75.3 dB SNDR," in *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2893–2905, Dec. 2016.

[9] B. Wu *et al.*, "A 24.7 mW 45 MHz-BW 75.3 dB-SNDR SAR-assisted CT ΔΣ modulator with 2nd-order noise coupling in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. (ISSCC) Tech. Papers*, Jan./Feb. 2016, pp. 270–271.

[10] I.-H. Jang *et al.*, "A 4.2-mW 10-MHz BW 74.4-dB SNDR continuous-time delta-sigma modulator with SAR-assisted digital-domain noise coupling," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1139–1148, Apr. 2018.

[11] T. Kim, C. Han, and N. Maghari, "A 7.2 mW 75.3 dB SNDR 10 MHz BW CT delta-sigma modulator using Gm-C-based noise-shaped quantizer and digital integrator," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1840–1850, Aug. 2016.

[12] N. Maghari and U. K. Moon, "A third-order DT ΔΣ modulator using noise-shaped bi-directional single-slope quantizer," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2882–2891, Dec. 2011.

[13] T. Kim, C. Han, and N. Maghari, "A 4th-order continuous-time delta-sigma modulator using 6-bit double noise-shaped quantizer," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3248–3261, Dec. 2017.

[14] C. Y. Ho *et al.*, "A 4.5 mW CT self-coupled ΔΣ modulator with 2.2 MHz BW and 90.4 dB SNDR using residual ELD compensation," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2870–2879, Dec. 2015.

[15] Z. Li and T. S. Fiez, "A 14 bit continuous-time delta-sigma A/D modulator with 2.5 MHz signal bandwidth," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1873–1883, Sep. 2007.

[16] G. Wei, P. Shettigar, F. Su, X. Yu, and T. Kwan, "A 13-ENOB, 5 MHz BW, 3.16 mW multi-bit continuous-time ΔΣ ADC in 28 nm CMOS with excess-loop-delay compensation embedded in SAR quantizer," in *Proc. Symp. VLSI Circuits (VLSI)*, Kyoto, Japan, Jun. 2015, pp. C292–C293.

[17] Y. Dong *et al.*, "A 72 dB-DR 465 MHz-BW continuous-time 1-2 MASH ADC in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2917–2927, Dec. 2016.

[18] M. Ortmanns and F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion*. Berlin, Germany: Springer-Verlag, 2006, pp. 94–113.

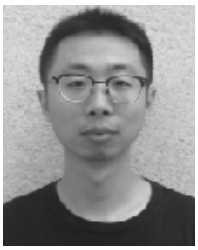
[19] M. De Bock, X. Xing, L. Weyten, G. Gielen, and P. Rombouts, "Calibration of DAC mismatch errors in ΔΣ ADCs based on a sine-wave measurement," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 9, pp. 567–571, Sep. 2013.

[20] H. Zhu, W. Yang, G. Engel, and Y.-B. Kim, "A two-parameter calibration technique tracking temperature variations for current source mismatch," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 4, pp. 387–391, Apr. 2017.

[21] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Fukuoka, Japan, Nov. 2008, pp. 269–272.

[22] D.-Y. Yoon, S. Ho, and H.-S. Lee, "A continuous-time sturdy-MASH ΔΣ modulator in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2880–2890, Dec. 2015.

[23] M. Bolatkale, L. J. Breems, R. Rutten, and K. A. A. Makinwa, "A 4 GHz continuous-time ΔΣ ADC with 70 dB DR and −74 dBFS THD in 125 MHz BW," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2857–2868, Dec. 2011.



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