A 16-mW 1-GS/s With 49.6-dB SNDR TI-SAR ADC for Software-Defined Radio in 65-nm CMOS

Lei Qiu, Kai Tang, Yuanjin Zheng, *Senior Member, IEEE*, Liter Siek, Yan Zhu, *Member, IEEE*, and Seng-Pan U, *Fellow, IEEE*

***Abstract*— This paper presents a 10-bit 1-GS/s four-channel time-interleaved (TI) successive approximation register (SAR) analog-to-digital converter (ADC). To suppress the time skew, the full rate master clock-based sampling technique is adopted. The effect of sampling switch mismatches on time skew is addressed. The measured time skew spurs caused by the sampling switch mismatches are around −52 to −55 dB at Nyquist input. Then, a tap-interpolating fractional delay filters-based digital background time skew calibration technique is proposed. Also, a full analysis of the effects of the various parameters on the time skew generated spur levels is presented, which indicates that the time skew error level is related to the length of calibration filters, calibration range, and bandwidth penalty. The subchannel ADC exploits a 250-MS/s SAR ADC with a low-cost high-speed subradix-2 searching technique. The reference interference of nonbinary TI ADCs is discussed and tolerated by the subradix-2 searching scheme. The proposed adders-based encoding circuit is optimized with lower propagation delay to meet high-speed requirements. The prototype was fabricated in a 65-nm CMOS technology. The measurement results show that the ADC achieves a signal-to-noise-plus-distortion ratio of 49.6 dB with a power of 15.95 mW and a figure of merit of 63 fJ/conversion step when operating at 1-GS/s and 458.1-MHz Nyquist input. The ADC core achieves an area of 0.158 mm^2.**

***Index Terms*— Digital background calibration, subradix-2, successive approximation register (SAR) analog-to-digital converters (ADCs), time interleaved (TI), time skew.**

I. Introduction

THE scaling of CMOS technology has fuelled the emergence of high-performance analog-to-digital converters (ADCs) with lower power consumption and smaller silicon area [1]–[6]. The power and area efficient high-performance ADCs, instead of traditional ADCs with hundreds of milliwatts power consumption [7]–[11], facilitate software-defined radio, and wideband communication implementations. Also, portable testing instruments (e.g., portable oscilloscopes, spectrum analyzers) could be further developed by leveraging such low-power high-performance ADCs.

Manuscript received June 17, 2017; revised August 22, 2017 and October 3, 2017; accepted November 6, 2017. Date of publication December 4, 2017; date of current version February 22, 2018. This work was supported by Infineon Technologies Asia Pacific Pte. Ltd., Singapore. *(Corresponding author: Lei Qiu.)*

L. Qiu, K. Tang, Y. Zheng, and L. Siek are with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798 (e-mail: qiul0002@e.ntu.edu.sg; KTANG@ntu.edu.sg).

Y. Zhu and S.-P. U are with the Analog and Mixed Signal VLSI Laboratory, University of Macau, Macao 0000, China and also with the Faculty of Science and Technology, University of Macau, Macao 0000, China.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TVLSI.2017.2771811

It is known that pipelined ADCs are suitable for implementations with high-resolution and high-speed sampling at gigahertz frequencies [12]–[15]. However, to achieve low power consumption, power efficient amplifiers are needed. Some techniques were reported [15]–[19] to overcome the design challenges (low intrinsic device gain and low-power supply). However, the calibration techniques introduce complicated circuits requiring additional silicon area and power consumption [15]. Successive approximation register (SAR) ADCs are power and area efficient [1]–[6]. However, due to the serial comparison nature and accuracy requirement for each comparison cycle, the sampling rates of prior high-speed SAR ADCs [1], [20], [21] are limited. Complex arithmetical unit-based subradix-2 algorithm has been discussed in [32] and [35]. They were not suitable for high-speed implementations due to the long SAR logic loop propagation delay. To achieve higher sampling rate with SAR architecture, time-interleaved (TI) SAR ADCs were presented [5], [9]–[11], [22]–[24]. However, the power and area overhead in terms of clock distribution increase heavily. The power efficiency of a 24-way TI SAR ADC in [24] was improved as compared with traditional TI ADCs [9]–[11]. However, the time-interleaving overhead of clock distribution is still non-negligible. Another eight-way TI SAR ADC [22] consumes large area of 0.78 mm^2 with off-chip timing calibration, with one flash ADC degrading the system power efficient. The state-of-the-art TI SAR ADC [23] with fully digital background time skew calibration utilized the differentiating finite-impulse response (FIR) filter to estimate and compensate the timing offset, which consumes large power and has large bandwidth penalty.

In this paper, we present a 1-GS/s 10-bit four-channel TI SAR ADC consuming only 15.95-mW power and 0.158-mm^2 core area [40]. To constrict the time skews in a small range, a time skew suppressed sampling technique with full rate clock for TI ADCs is utilized and the mismatch of sampling switches is considered. To further compensate the time skew, a tap-interpolating fractional delay (TIFD) FIR correction filter-based calibration technique is proposed, which consumes less computation units and drops less bandwidth in digital domain. A full analysis of parameter effect on time skew spurs is presented, which indicates that the time skew error level is related to the length of calibration filters [interpolation filter (IF) and fractional delay filter], calibration range, and bandwidth penalty. In addition, the reference interference in redundant TI SAR ADC is addressed. This paper implements a high-speed subradix-2 searching technique, with only

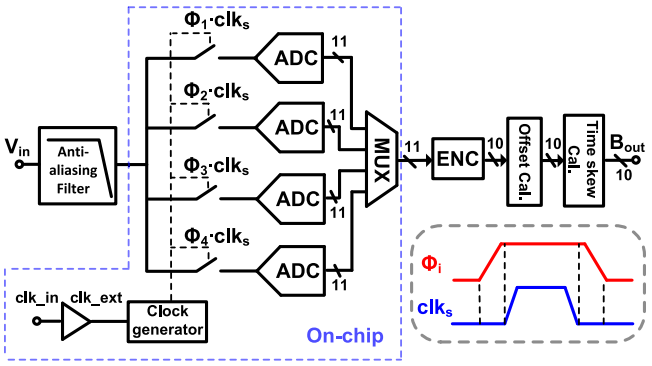


Fig. 1. Proposed architecture of the four-channel TI-ADC with sampling rate at 1 GS/s.

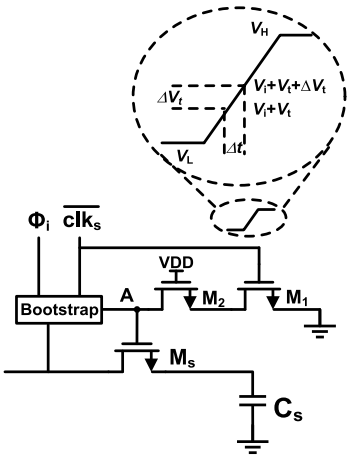


Fig. 2. Effect of threshold mismatch on time skew.

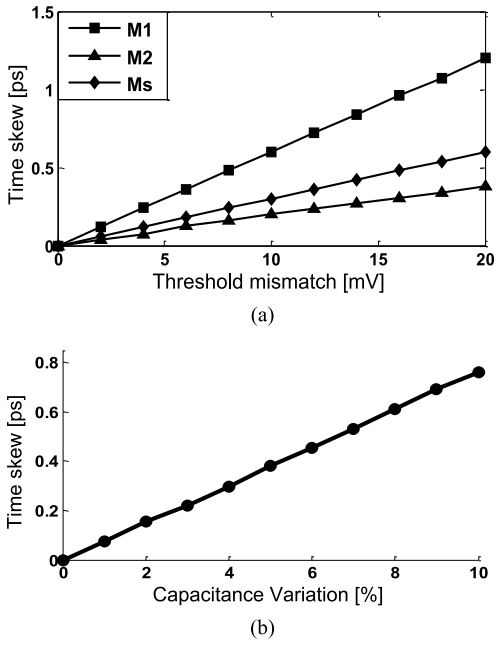


Fig. 3. Relation between time skew and (a) offset of transistors M_1, M_2, and Ms and (b) capacitance variation at node A.

adder-based encoding (ENC) scheme for SAR ADCs. The proposed adders-based ENC circuit is optimized with lower propagation delay to meet high-speed requirement.

This paper is organized as follows. Section II introduces the proposed TI SAR ADC architecture, including sampling scheme, subradix-2 high-speed sub-SAR ADC, and the proposed digital background time skew calibration technique. The detailed circuit implementations are described in Section III. Section IV shows the measurement results. Finally, the conclusion is drawn in Section V.

II. Proposed TI-ADC Architecture

The overall ADC architecture is shown in Fig. 1, which consists of four sub-SAR ADCs operating at 250 MS/s with total 1 GS/s [40]. An antialiasing filter, which is implemented off-chip, is inserted in front of the ADC to filter noise and interference out of the band of interest. To reduce the time skew, the sampling instant of each channel is only determined by the falling edge of the 1-GS/s master clock clk_s, while the corresponding TI clock signals Φ_i ($i = 1, 2, 3, 4$) are used to perform the channel selection [13]. In sub-ADCs, one redundant bit is implemented in the proposed subradix-2 searching technique. After multiplexing, the digital outputs are decimated by a factor of 45 for testing purpose. The selection of decimation factor should equal $n \cdot M + 1$ to ensure the decimated output rotating equally across all interleaved channels. Variable n is an integer and the M is the number of channels. The decimated outputs of ADC are followed by an ENC circuit to encode the outputs from 11-bit to 10-bit. The offset errors are extracted and compensated by averaging and accumulation in digital domain [7].

A. Sampling Network

Although each channel is sampled by the same clock signal clk_s, there are still some time skew error sources, including threshold mismatches of the sampling switches (transistors M_1, M_2, and Ms in Fig. 2) and size mismatches after fabrication. The effect of threshold mismatch of transistor M_1 is explained in Fig. 2. The time skew Δt can be derived as

$$\Delta t = \frac{t_{\text{fall}}}{V_H - V_L} \Delta V_t \tag{1}$$

where t_{fall} is the falling (rising) time of the clock. From (1), it can be concluded that making the falling edge sharper and reducing threshold mismatch ΔV_t of transistor M_1 could decrease the time skew. To reduce threshold mismatches of sampling switches (transistors M_1, M_2, and Ms) shown in Fig. 2, the size of sampling switch could be increased properly according to [36], which states that the standard deviation of threshold mismatch is

$$\sigma_{\Delta V_t} = \frac{A_{V_t}}{\sqrt{WL}} \tag{2}$$

where A_{Vt} is the matching constant. To evaluate the effect of process variation on time skew, we set the falling time of clk_s as 70 ps, the size of M_1 and M_2 as 4 μm/60 nm and the size of the Ms as 15 μm/60 nm. The simulation results of threshold mismatch and capacitance mismatch at node A (Fig. 2) versus time skew are illustrated in Fig. 3, where M_1 has a more

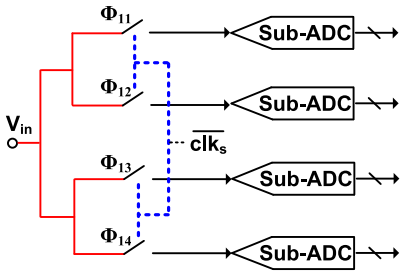


Fig. 4. Layout guidance of input and clock signal for the four-channel TI-ADC.

significant effect on time skew. The time skew is proportional to the capacitance variation at node A. To suppress the error caused by unmatched routing, the routing of clock signal clk_s and input signal V_{in} are illustrated in Fig. 4. The "binary tree" connection is utilized to guarantee the routings of clk_s and V_{in} to each channel identical. Assuming that the time skew error is treated as Gaussian distributed variable, the relation between signal-to-noise-plus-distortion ratio (SNDR) and time skew standard deviation σ_t with given input frequency f_{in} is [37]

$$\text{SNDR} = 20\log\frac{1}{2\pi f_{\text{in}}\sigma_t} - 10\log\left(\frac{M-1}{M}\right). \tag{3}$$

Therefore, to satisfy an SNDR of 60 dB at a 500-MHz input frequency, the time skew deviation σ_t between channels should be less than 0.37 ps, which is difficult to achieve without additional calibration even with perfect matching layout.

B. TIFD Filter-Based Time Skew Calibration

Fractional delay filters (FDF) [27], [28] could be utilized to compensate the time skew error in digital domain. Supposing T is the overall ADC sampling period, and $T_d = \alpha T$ represents the fractional delay, where α is the normalized fractional delay. Because of the presented time skew suppressed sampling technique, the range of fractional delay in this design could be constrained into $[-0.002T, +0.002T]$. The calibration of time skew is divided into two parts: detection and correction. The time skew detection technique in [29] is employed, which compares the mean value (by accumulation and average) of the multiplication of signals $x_m(n)$ $(m = 0, 1, 2, \ldots, M-1)$ in two adjacent channels to detect the polarity of time skew error $p(t_m)$ and updates the coefficients of fractional delay FIR filter $F(a_m)$ adaptively as shown in Fig. 5 [40]. For time skew correction, the proposed fractional delay FIR filter architecture is shown in Fig. 6, where only the second channel $(m = 1)$ is illustrated and the length of FIR correction filter is $2N + 1$ $(N = 2, 4, \ldots)$ $(N = 2$ in Fig. 6). The α indicates the time error to be calibrated. $C = [c_{0,0}, c_{0,1}, c_{1,0}, c_{1,1}, c_{2,0}, c_{2,1}, c_{3,0}, c_{3,1}, c_{4,0}, c_{4,1}]$ are the coefficients of fractional delay filters. $I_{m,m+1}(n)$ is the IF to generate the interpolated tap between channel m and channel $m + 1$. The input of the IF is the sampled raw data from the all subchannels.

To update the coefficients of the fractional delay filters with the detected time skew error α, the coefficients are approximated by first-order polynomials of α (shown in Fig. 6).

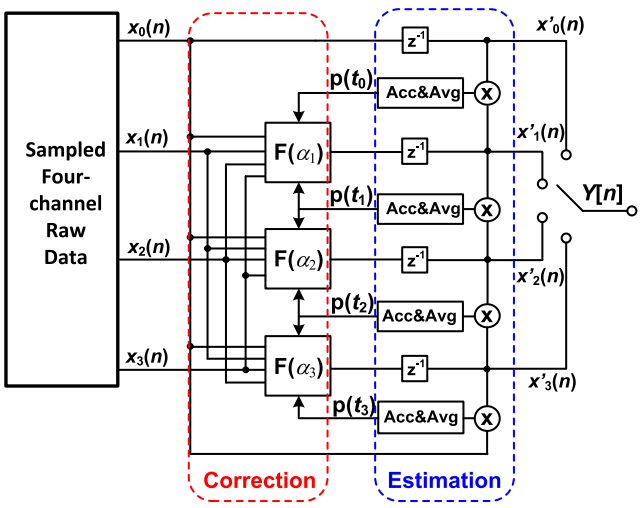


Fig. 5. Calibration architecture for the time skew error.

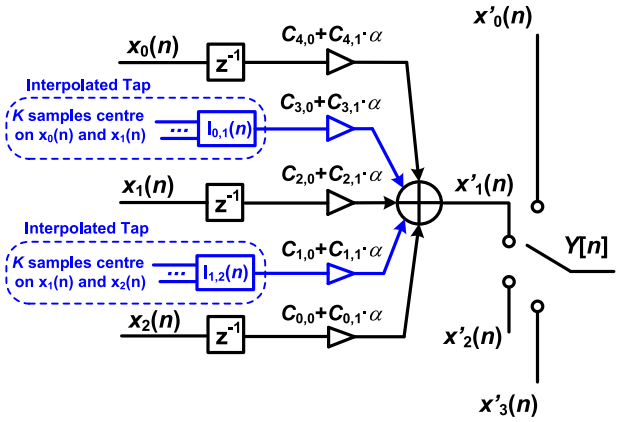


Fig. 6. Structure of FIR correction filter of a subchannel with $N = 2$ and $M = 4$.

The approximation error is

$$e(\omega, \alpha) = F(\omega, \alpha) - D(\omega, \alpha) \tag{4}$$

where

$$F(\omega, \alpha) = \sum_{n=0}^{N}(c_{2n,0} + \alpha c_{2n,1})e^{-j\omega(n+\frac{K-N}{2})T} + \sum_{n=0}^{N-1}(c_{2n+1,0} + \alpha c_{2n+1,1})\sum_{k=0}^{K-1} e^{-j\omega(k+n)T} \tag{5}$$

and

$$D(\omega, a) = e^{-j\omega\left(\alpha+\frac{K}{2}\right)T}. \tag{6}$$

$F(\omega, \alpha)$ and $D(\omega, \alpha)$ are the transfer function of the TIFD filter and the ideal fractional delay function, respectively. Variable K $(K = 2, 4, \ldots)$ is the length of IF. For the ideal fractional delay filter, α and $K/2$ are the fractional (time skew) and integral delay (middle tap of IF), respectively. The coefficients of FDF $C_{n,m} = [c_{0,0}, c_{0,1}, c_{1,0}, c_{1,1}, \ldots, c_{2N,0}, c_{2N,1}]$, whose length is $4N + 2$, are to be optimized. The transfer function $F(\omega, \alpha)$ of the FIR filter can be rewritten as [43]

$$F(\omega, a) = C_{n,m} \cdot (c(\omega, a) - js(\omega, a))^{\text{T}} \tag{7}$$

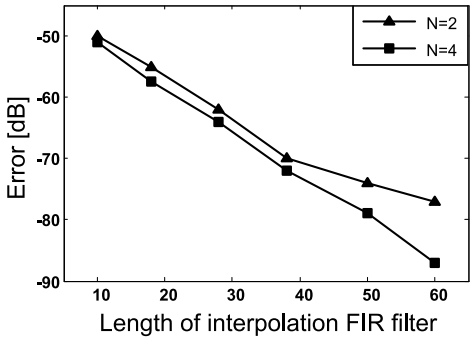


Fig. 7. Error level versus the length of interpolation FIR filters (bandwidth penalty = 5%, calibration range is [−0.002T, 0.002T]).

where

$$c(\omega) = \left[\cos\left(\frac{K-2}{2}\omega\right), a\cos\left(\frac{K-2}{2}\omega\right), \sum_{k=0}^{K-1}\cos\ (k\omega)\right.$$
$$a\sum_{k=0}^{K-1}\cos\ (k\omega), \ldots \sum_{k=0}^{K-1}\cos\ ((k+N-1)\omega)$$
$$a\sum_{k=0}^{K-1}\cos\ ((k+N-1)\omega), \cos\left(\left(\frac{K}{2}-1+N\right)\omega\right)$$
$$\left. a\cos\left(\left(\frac{K}{2}-1+N\right)\omega\right)\right]$$

and

$$s(\omega) = \left[\sin\left(\frac{K-2}{2}\omega\right), a\sin\left(\frac{K-2}{2}\omega\right), \sum_{k=0}^{K-1}\sin\ (k\omega),\right.$$
$$a\sum_{k=0}^{K-1}\sin\ (k\omega), \ldots \sum_{k=0}^{K-1}\sin\ ((k+N-1)\omega),$$
$$a\sum_{k=0}^{K-1}\sin\ ((k+N-1)\omega), \sin\left(\left(\frac{K}{2}-1+N\right)\omega\right),$$
$$\left. a\sin\left(\left(\frac{K}{2}-1+N\right)\omega\right)\right].$$

The error level of the proposed TIFD filters-based time skew calibration technique is related to four parameters, which are the length of IF, the length of FDF, calibration range, and bandwidth penalty. Fig. 7 shows the error level versus different lengths of IF. As the length of IF increases, the error level could be achieved by 5-tap ($N = 2$) FDF is limited to be −80 dB. If a 9-tap ($N = 4$) FDF is chosen, the error level could be suppressed to be −90 dB. The error level versus calibration range is illustrated in Fig. 8. It indicates that with smaller the targeted calibration range, the error level could be less. Fig. 9 shows the relation between error level and bandwidth penalty. As the bandwidth penalty increases, the error level could be suppressed significantly. Similar with the scenario in Fig. 7, the error level is limited to be around −80 dB when 5-tap FDF is selected. In this paper, the lengths of IF and FDF are set to be 38 tap and 5 tap, respectively. And a calibration range of ±0.002 T with 5% bandwidth penalty is selected. The optimization results are shown in Fig. 10.

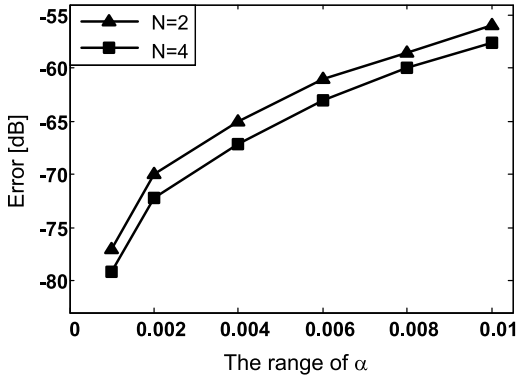


Fig. 8. Error level versus the range of fractional delay α (bandwidth penalty = 5% and length of IF = 38 tap).

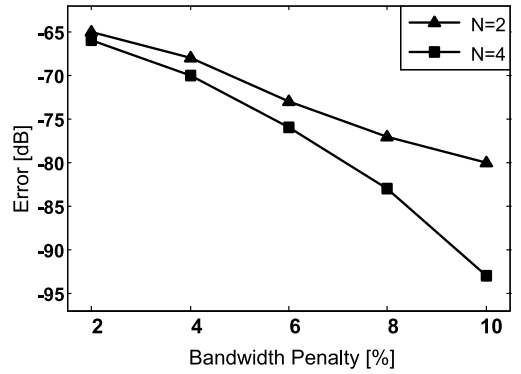


Fig. 9. Error level versus the bandwidth penalty (length of IF = 38 tap, calibration range is $[-0.002T, 0.002T]$).

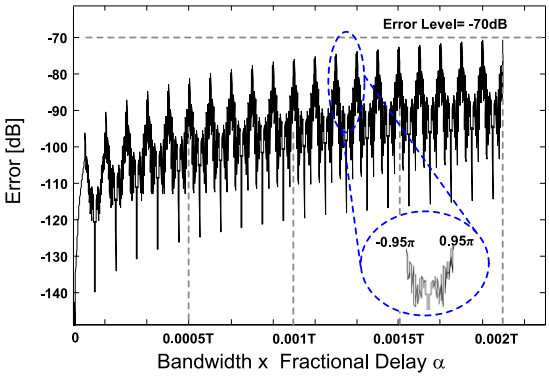


Fig. 10. Optimized error level versus bandwidth × fractional delay (length of IF = 38 tap, length of FDF = 5 tap, bandwidth penalty = 5%, and calibration range is $[-0.002T, 0.002T]$).

It shows that a −70-dB error level could be achieved. The advantage of the proposed calibration technique is that it can achieve background time skew error calibration with shorter tap fractional delay filters and less bandwidth penalty compared to [25] and [26]. Since the tap-interpolation is adopted in fractional correction filter design, it equivalently doubles the Nyquist band. Therefore, a smaller bandwidth penalty could be achieved. To save calibration cost, multiplier-less realization of digital filters [39] is employed. For instance, a 38-tap IF could be realized by using only 55 adders. The word length of all the optimized coefficients is 12 bits. As shown in Table I, with 38-tap IF and 5-tap TIFD filter, a −70-dB error level could be

TABLE I
PERFORMANCE COMPARISON OF DIGITAL CALIBRATION

	Filter Length (taps)	Bandwidth Penalty	Error (dB)	Adaptive	Cal. Range
[25]	60	10%	-72	No	$0.15T$
[26]	75+30	33%	-72	Yes	-
[23]	-	9.25%	-70	No	-
This work	**38+5**	**5%**	**-70**	**Yes**	**$0.002T$**

obtained with only 5% bandwidth scarified. The coefficients optimization of the 38-tap IF is depicted in the Appendix.

C. High-Speed Custom Weighted Subradix-2 SAR ADC

To design a 10-bit SAR ADC using conventional binary weighted digital-to-analog converter (DAC) array, it requires ten conversion cycles with each cycle satisfying the same settling accuracy requirement as

$$V_{\text{ref}} \cdot e^{-t/\tau} < V_{\text{ref}}/2^{M+1} \tag{8}$$

where M is the resolution of ADC, τ is the RC time constant of DAC settling. It means the required settling time for 10-bit resolution is $t > 7.6\tau$. Otherwise, the comparison error occurs. With presence of the custom weighted subradix-2 DAC [34], the settling accuracy requirements for the MSBs are significantly relieved. Taking a 4% redundancy range as an example, the required settling time is

$$V_{\text{ref}} \cdot e^{-t/\tau} < 4\% \cdot V_{\text{ref}} \Rightarrow t > 3.2\tau. \tag{9}$$

Therefore, the settling time of DAC could be shorter. Due to the large capacitance of MSB branches, the significant drop of reference voltage can also be covered by proper subradix-2 weights setting. For a DAC array with a 0.25-pF capacitance and a conversion time of 3.3 ns, it can be shown in Fig. 11(a) that to satisfy the precision requirement of reference voltage recovering in single-channel SAR ADC, the decoupling capacitance C_{dc} between positive and negative of reference voltage should be around 300 pF. With the presence of subradix-2 searching, the size of decoupling capacitor could be significantly reduced. Fig. 11(b) shows the reference voltage settling in TI SAR ADC. Since all the subchannels share the same reference voltage, the conversion phase of any channel will be interrupted by the other channels. The worst case happens at sampling and MSB settling of other channels. The analysis of reference interference on TI SAR ADCs has been addressed in [42]. The reference error caused by sampling and MSB settling could easily influence the conversion of other channels. To tolerate the shared reference voltage interference, the minimum redundant value ε_r should be larger than the maximum reference voltage ripple [shown in Fig. 11(b)], which means

$$\frac{C_{\text{DAC}}}{C_{\text{dc}}} < \varepsilon_r. \tag{10}$$

The redundant value ε_r should cover the sampling phase of all the subchannels.

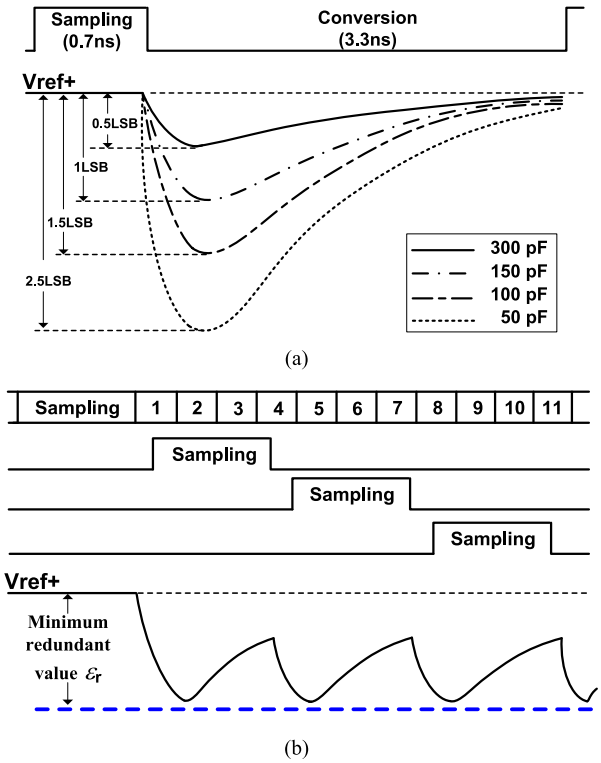


Fig. 11. Reference voltage settling. (a) In single-channel SAR ADC with different decoupling capacitances. (b) In a four-channel time-interleaved SAR ADC.

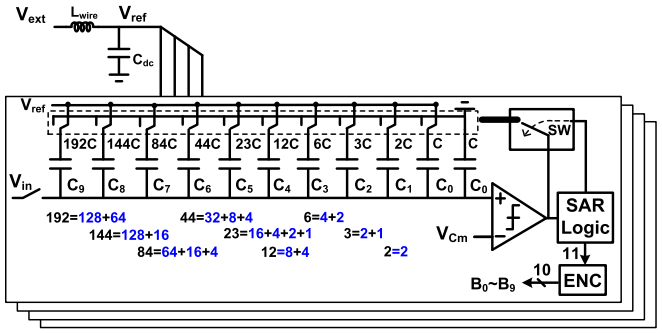
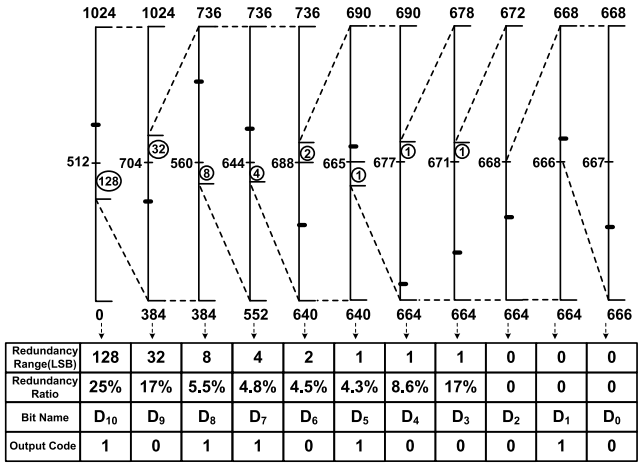


Fig. 12. Subradix-2 high-speed SAR ADC architecture, where only single end is shown.

In the TI SAR ADC, the subradix-2 weights are embedded into DAC array directly [34], resulting in high-speed conversions. The architecture of the subradix-2 SAR ADC is shown in Fig. 12. The off-chip reference voltage V_{ext} goes through the bonding wire L_{wire} and is decoupled by C_{dc} to generate V_{ref}. For sub-SAR ADC successive approximation, 11 conversion cycles are needed including one redundant bit. The subradix-2 weights $D_{10} \sim D_0$ are

$$\begin{aligned} D_{10} &= 2^9 - d_1 \\ D_9 &= 2^8 + \frac{d_1}{2} - d_2 \\ D_8 &= 2^7 + \frac{d_1}{2^2} + \frac{d_2}{2} - d_3 \\ &\cdots\cdots \\ D_0 &= 2^{-1} + \frac{d_1}{2^{10}} + \frac{d_2}{2^9} + \cdots + \frac{d_{10}}{2} - d_{11} \end{aligned} \tag{11}$$



Redundancy Range(LSB)	128	32	8	4	2	1	1	1	0	0	0
Redundancy Ratio	25%	17%	5.5%	4.8%	4.5%	4.3%	8.6%	17%	0	0	0
Bit Name	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Output Code	1	0	1	1	0	1	0	0	0	1	0

Fig. 13. Illustration of the subradix-2 algorithm operation with 666.5 LSB input.

TABLE II
TIME ALLOCATION FOR ONE SAR CONVERSION

	Each cycle	Number of cycles
DAC settling time	100 ps	10
Logic delay	50 ps	11
Comparison time	150 ps	11
Sampling	700 ps	
Total	3.9 ns	

which are 384, 288, 168, 88, 6, 24, 12, 6, 4, 2, 1 [34]. The redundancy ratios of the all the cycles are set to be larger than 4% to tolerate errors caused by the incomplete settling of the control switches. The last two redundant values are set to 1 LSBs to adjust the number of unit capacitors as integers to facilitate the floor planning of the DAC array. In Fig. 13, the subradix-2 algorithm is illustrated with a 666.5 LSBs' input. The numbers in circles are the redundant values of each cycle. With the different constraints of error tolerance range, the redundant value of each cycle and the number of redundant cycles could be properly changed. The total settling time requirement is shortened from 76τ ($7.6\tau \times 10$ cycles) to 35.2τ ($3.2\tau \times 11$ cycles) by using the proposed subradix-2 algorithm. The time allocation for one SAR conversion is depicted in Table II.

To convert the redundant ADC output codes to binary codes, the adder-based ENC circuit illustrated in Fig. 14 is adopted. $D_{10} \sim D_0$ represent the redundant outputs, and $B_9 \sim B_0$ represent the binary codes. The ENC operation is realized by adders instead of multiplier-based FIR filters [33]. Compared with [20], no subtraction and extra unit capacitors are required. Although the hardware overhead [12 full adders (FA), 8 half adders (HA), 1 OR gate] is as the same as the ENC circuit in [34], the propagation delay is significantly improved. In the improved ENC circuit shown in Fig. 14, the delay of worst case includes four HAs and five FAs, which is from D_1 (e.g., toggling from 0 to 1) to B_9. However, the delay of from D_1 to B_9 in the ENC circuit in [34] could include up to 5 HAs

Weight	512	256	128	64	32	16	8	4	2	1
		D_{10} D_9	D_{10} D_8	D_7	D_9 D_8 D_6	D_7 D_5	D_8 D_7 D_6 D_5 D_4	D_6 D_4 D_3 D_2	D_6 D_3 D_1	D_0
+										
Binary out	B_9	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0

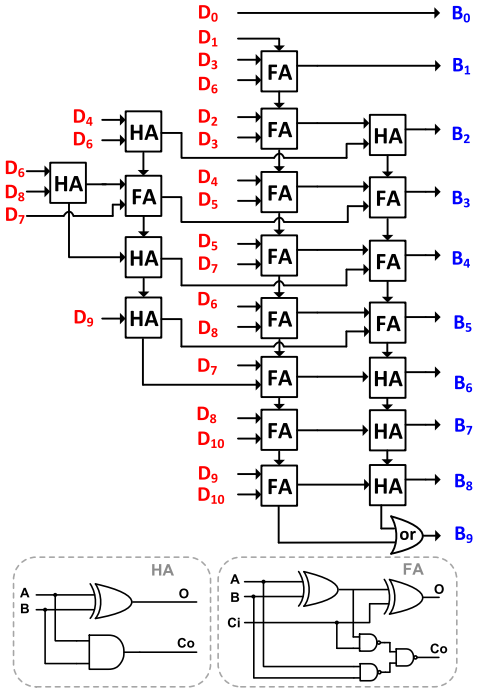


Fig. 14. Mapping table and schematic of ENC circuit from D_i ($i = 0 \sim 10$) to B_j ($j = 0 \sim 9$).

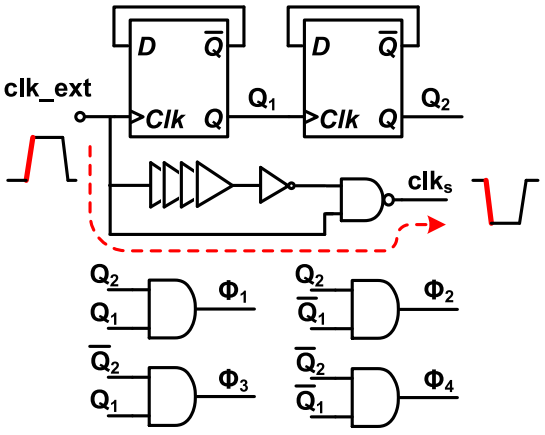


Fig. 15. Schematic of internal clock generator.

and 11 FAs. The ENC circuit are built with only adders (FA) and HA, resulting in low-power consumption.

III. CIRCUIT DESIGN

A. Internal Clock Generator

To suppress the time skew in TI SAR ADCs, a clock signal with Nyquist sampling rate is needed. The schematic of internal clock generator is shown in Fig. 15, where *clk_ext* is the external clock input. Signal Q_1 and Q_2 are generated

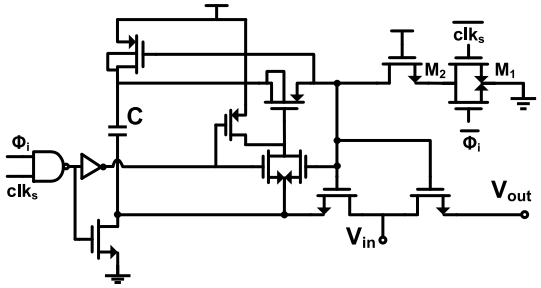


Fig. 16. Schematic of sampling switch.

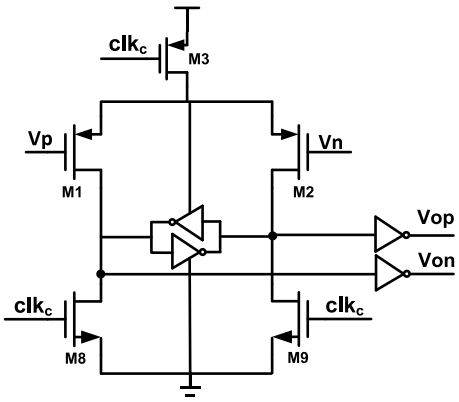


Fig. 17. Schematic of comparator circuit.

by divide by 2 and divide by 4, respectively. The signal clk_s is obtained from *clk_ext* with duty cycle changed. When clk_s is high, one of four subchannels operates in sampling phase. Using Q_1 and Q_2, Φ_i $(i = 1, 2, 3, 4)$ can be generated through AND gates. In this design, the rising edge of the buffered *clk_ext* goes through only one NAND gate to generate the falling edge of clk_s, introducing less additional jitter through internal clock path. The power supply for clk_s generation is separated from other logic circuit to reduce power supply noise interference. The schematic of bootstrapped switch for the proposed sampling technique is drawn in Fig. 16. Φ_i is the control signal mentioned before. When Φ_i is high, the corresponding bootstrapped switch is activated. clk_s is the full rate sampling clock, dominating the sampling instant.

B. Single-Channel SAR ADC

The monotonic DAC switching [31] is adopted for sub-ADC. The schematic of dynamic comparator is shown in Fig. 17. The pMOS transistors are adopted as the input pair. When *clk_c* is high, the comparator is in reset phase. It enters comparison phase when *clk_c* is low. Two inverters follow the *Vop* and *Von* to prevent hysteresis effect caused by the following latch circuit. The programmable synchronous timing generator providing local timing with process corner sensing function is shown in Fig. 18. The generator is an oscillation circuit with an enable signal clk_s. When clk_s is low, the oscillation loop is activated. A duplicated dynamic comparator is inserted into the loop to sense the process variation of regeneration time. *t_sel* is to tune the load capacitance of the comparator, which means changing the period of clk_c. The duty cycle adjustment block is used

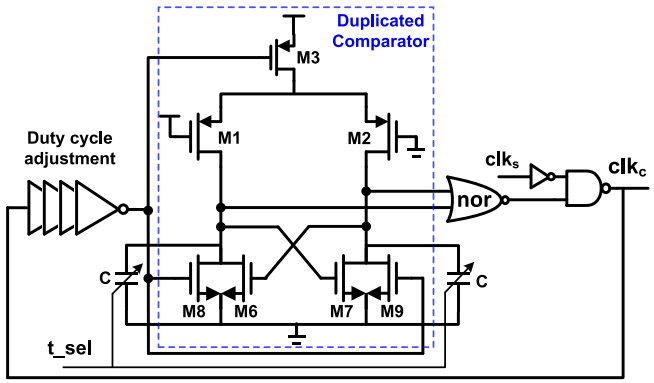


Fig. 18. Schematic of local synchronous timing generator.

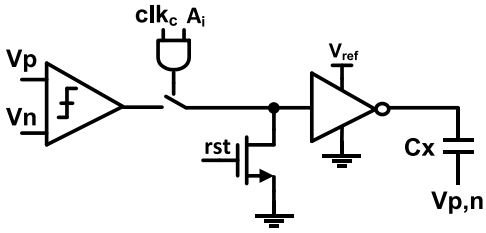


Fig. 19. Schematic of control logic circuit.

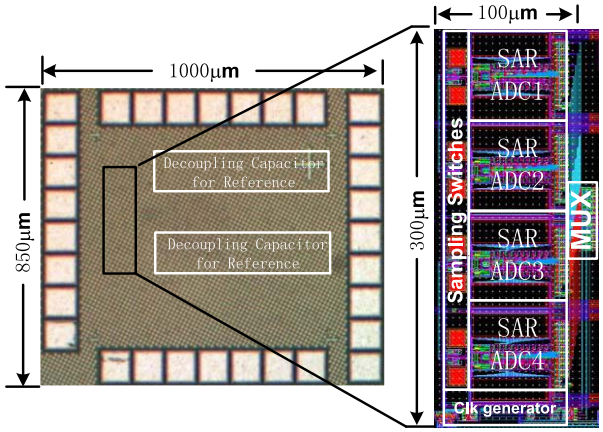


Fig. 20. Chip micrograph and layout.

to change the duty cycle of clk_c to balance the duration of comparison and DAC settling. The proposed dynamic control logic shortens the delay between comparator output and DAC array, which just equals to the delay of one transmission gate and an inverter. The schematic of DAC control logic is shown in Fig. 19. In the sampling phase, the reset signal *rst* is high, and all the unit capacitors in DAC array are connected to V_{ref}. During the conversion phase, the DAC array is controlled by *clk_c* under certain state A_i. The control logic is controlled by a state machine-based shift register. The unit capacitor is realized with five-stacked metal layer.

IV. Measurement Results

The ADC chip is fabricated in a 1P9M 65-nm CMOS process with low-V_{th} option. The die photograph is shown in Fig. 20, and the ADC core occupied 0.158 mm^2. Instead of using power hungry reference buffer, a decoupling

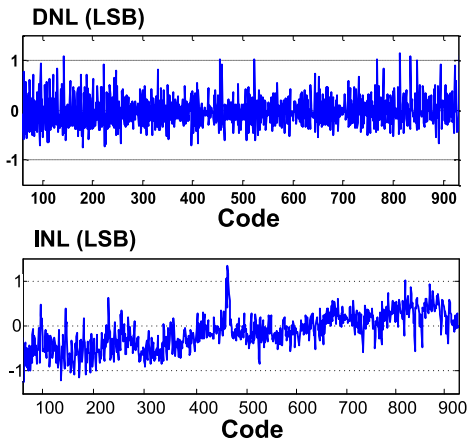


Fig. 21. Measurement results of DNL and INL.

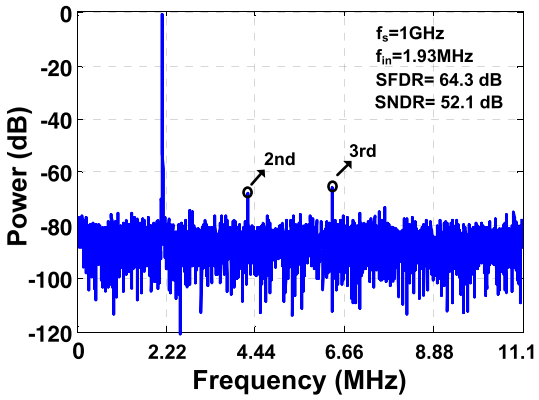


Fig. 22. Measured 8192-point FFT (digital output is decimated by 45) with $f_{\text{in}} = 1.9$ MHz.

capacitor C_{dc} of 100 pF, which occupies 0.09 mm^2, is used to guarantee a sufficient error coverable range for the successive approximation comparisons. The measurement is conducted in room temperature. The power consumption is 7.95 mW (excluding off-chip time skew calibration) at 1.2-V power supply when operating at 1 GS/s, with each subchannel SAR ADC consuming 1.85 mW, and 0.4 mW for the internal clock generation and multiplexing. The ENC block is designed off-chip, of which the estimated power is 0.15 mW and its area is 110 μm^2. The offset mismatch and background time skew calibration are done off-chip, of which the estimated power consumption is 8 mW and area is 0.038 mm^2 with 39 600 gate count. The capacitance of each single-end input sampling DAC array is 240 fF (512C, each unit capacitor C of 0.47 fF) excluding parasitic capacitance. To reduce the effect of parasitic inductor of bonding wire, double input pads are used with the parasitic capacitance of 2 pF. The impedance of input is matched to be 50 Ω on board, resulting in a 3-GHz input bandwidth. In this design, the differential input range is 2 V_{p-p} at 1.2-V supply.

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are shown in Fig. 21. The peak DNL is +1.2/−0.7 LSBs and peak INL is +1.3/−1.2 LSBs. Fig. 22 shows the measured output spectrum of 1.9 MHz. The SNDR is 52.1 dB, which is limited by large measured input-referred noise of comparator. Before offset calibration,

TABLE III
SUMMARY OF THREE TESTED CHIPS

Chip sample	Time error (SFDR @458.1 MHz)	Offset error (Average)	Gain error (Average)
No.1	52.1 dB	26mV	0.0008
No.2	55.3 dB	17mV	0.0005
No.3	53.4 dB	28mV	0.0006

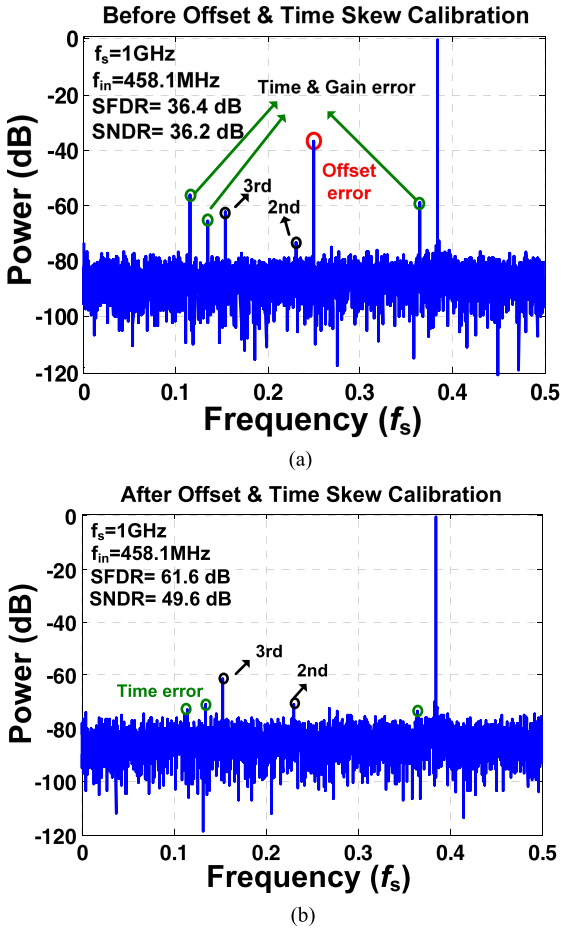


Fig. 23. Measured 8192-point FFT (digital output is decimated by 45) with $f_{\text{in}} = 458.1$ MHz (a) before and (a) after offset and time skew calibration.

TABLE IV
OPTIMIZED FILTER COEFFICIENTS

$C_{n,m}$	m=0	m=1
n=0	-3.5e-7 (0)	0.2675
n=1	4.1e-6 (0)	-1.4925
n=2	1	-7.3e-13 (0)
n=3	4.1e-6 (0)	1.4925
n=4	-3.5e-7 (0)	-0.2675

the SNDR and spurious-free dynamic range (SFDR) are degraded mainly by offset mismatch. It is found that the gain mismatch is small enough with negligible effect on the SNDR and SFDR. Without time skew calibration, the SFDR caused

TABLE V
COMPARISON OF STATE-OF-THE-ART GIGAHERTZ ADCS

	ISSCC 2016[41]	JSSC 2013[15]	JSSC 2014[13]	ISSCC 2013[5]	ISSCC 2014[23]	ISSCC 2014[22]	This Work	
Architecture	TI-SAR	Pipe-line	Pipe-line	TI-SAR	TI-SAR	TI-SAR	TI-SAR	
Time skew calibration	Off-chip	Off-chip	No	No	On-chip	Off-chip	No	Off-chip
Technology (nm)	40	65	65	40	40	65	65	
Supply voltage(V)	1.1	1.0	1.0	1.2	1.1	1.0	1.2	
Power (mW)	18.4(1)	19.0	7.1	10.8	93	18.9	7.95	15.95(2)
Fs (GS/s)	2.6	0.8	1.0	0.9	1.6	1.0	1.0	
Resolution(bit)	10	10	9	9	9	10	10	
SNDR@ Nyquist(dB)	50.6	52.2	47.7	51.2	48.0	51.4	48.3	49.6
FoM (fJ/con-step)	25.6(1)	71.4	35.6	40.5	283	62.3	36.7	63(2)
Active Area (mm^2)	0.825(1)	0.18	0.1	0.038	0.83	0.78	0.03	0.158(2)(3)

(1) Digital calibration is not included.
(2) Including estimated power and active area used for the offset and time skew calibrations.
(3) Decoupling capacitors are included.

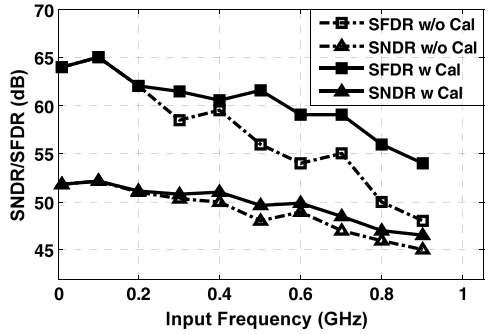


Fig. 24. SFDR and SNDR before and after time skew calibration versus input frequency at $f_s = 1$ GHz and $V_{dd} = 1.2$ V.

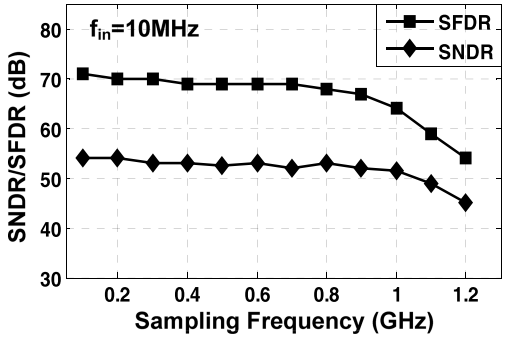


Fig. 25. SFDR and SNDR versus sampling frequency at $f_{in} = 10$ MHz and $V_{dd} = 1.2$ V.

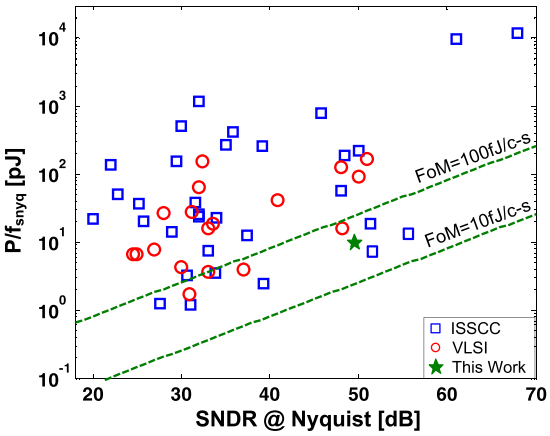


Fig. 26. Energy per conversion for all ADCs with published at ISSCC and VLSI conferences from 1997 to 2016.

by time error at 458.1-MHz input is around 52–55 dB (0.6-ps rms equivalently) with W/L of M_2 (Fig. 16) being around 4 μm/60 nm. The summary of measurement for the three sample chips is listed in Table III. In Fig. 23, after offset and time skew calibration, the measured SFDR at a 458.1-MHz input are improved to 61.6 dB (harmonic dominated), with all the time skew spurs less than -70 dB. The corresponding effective number of bit is 7.96 bits at Nyquist input frequency. The length of time skew correction filter and IF is set as 5 and 38, respectively, which calibrate the time skew spurs to be lower than -70 dB. The coefficients of correction filter are listed in Table IV. Assuming the first channel as the reference channel, the measured time skew of other three channels in one chip are -0.6, 0.1, and -1.5 ps. The iterative time step T_{step} is set to 0.1 ps. Fig. 24 shows the SFDR and SNDR (before and after time skew calibration) versus input frequency from 10 to 900 MHz. Fig. 25 shows the SFDR and SNDR versus sampling frequency at 10-MHz input frequency. Compared with the state-of-the-art ADCs (Table V), the proposed ADC achieves a low figure-of-merit value of 36.7 fJ/conversion step (63 fJ/conversion step with time skew compensation) and a die size of 0.03 mm^2 (0.158 mm^2 including time skew calibration and decoupling capacitors). In terms of energy per conversion, this paper achieves 15.9 pJ per conversion. A comparison with the prior state-of-the-arts ADCs faster

TABLE VI
COEFFICIENTS OF INTERPOLATION FILTER

n	IF(*z*)	*n*	IF(*z*)	*n*	IF(*z*)
0	0.00375	13	-0.05225	26	0.03500
1	-0.00500	14	0.06600	27	0.02900
2	0.00650	15	-0.08725	28	-0.02450
3	-0.00800	16	0.12475	29	0.02050
4	0.00975	17	-0.21075	30	-0.01725
5	-0.01200	18	0.63600	31	0.01425
6	0.01425	19	0.63600	32	-0.01200
7	-0.01725	20	-0.21075	33	0.00975
8	0.02050	21	0.12475	34	-0.00800
9	-0.02450	22	-0.08725	35	0.00650
10	0.02900	23	0.06600	36	-0.00500
11	-0.03500	24	-0.05225	37	0.00375
12	0.04225	25	0.04225		

than 1 GS/s published at ISSCC and VLSI conference from 1997 to 2016 [38] is shown in Fig. 26.

V. CONCLUSION

A test chip of a four-channel 10-bit SAR ADC with sampling rate up to 1 GS/s, adopting time skew suppressed sampling technique, is presented. By utilizing the power and area efficient subradix-2 high-speed sub-SAR ADCs, the TI-ADC achieves a low-power consumption (15.95 mW) at 1 GS/s and small silicon area of 0.158 mm^2 including time skew calibration and decoupling capacitors. Moreover, the remaining time skew error could be compensated readily to be lower than -70 dB by TIFD filters-based digital background time skew calibration. The custom designed subradix-2 DAC array improves the error tolerance capability during the conversion. Additionally, the adders-based ENC logic provides a power and area efficient error-tolerant SAR ADC architecture.

APPENDIX

The Appendix describes the optimization of coefficients of IF. The approximation error is

$$e_{IF}(\omega) = F_{IF}(\omega) - D_{IF}(\omega) \tag{12}$$

where

$$F_{IF}(\omega) = \sum_{k=1}^{K} c_k \cdot e^{-j\omega kT} \tag{13}$$

and

$$D_{IF}(\omega) = e^{-j\omega\left(\frac{1}{2}+\frac{K}{2}\right)T}. \tag{14}$$

$F_{IF}(\omega)$ and $D_{IF}(\omega)$ are the approximation function and the ideal half delay, respectively. Variable K ($K = 2, 4, \ldots$) is the length of interpolation FIR filter. The coefficients c_k ($k = 1, 2, \ldots$ K) are to be optimized. The min–max criterion is adopted to optimize the coefficients of IF, and the optimization problem is solved by standard second-order cone programming solver [43]. The coefficients of the 38-tap IF are listed in Table VI. The coefficients are symmetric about the two central taps (tap-18 and tap-19). The word-length of the coefficients is 12 bits.

REFERENCES

[1] G.-Y. Huang, S.-J. Chang, Y.-Z. Lin, C.-C. Liu, and C.-P. Huang, "A 10b 200 MS/s 0.82 mW SAR ADC in 40 nm CMOS," in *IEEE ASSCC Dig. Tech. Papers*, Nov. 2013, pp. 289–292.

[2] C. H. Chan, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "A 3.8 mW 8b 1 GS/s 2b/cycle interleaving SAR ADC with compact DAC structure," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2012, pp. 86–87.

[3] B. Verbruggen, M. Iriguchi, and J. Craninckx, "A 1.7 mW 11b 250 MS/s 2x interleaved fully dynamic pipelined SAR ADC in 40 nm digital CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 466–467.

[4] L. Kull *et al.*, "A 3.1 mW 8b 1.2 GS/s single-channel asynchronous SAR ADC with alternate comparators for enhanced speed in 32 nm digital SOI CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3049–3058, Dec. 2013.

[5] H.-K. Hong *et al.*, "An 8.6 ENOB 900 MS/s time-interleaved 2b/cycle SAR ADC with a 1b/cycle reconfiguration for resolution enhancement," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 470–471.

[6] Y.-C. Lien, "A 4.5-mW 8-b 750-MS/s 2-b/step asynchronous subranged SAR ADC in 28-nm CMOS technology," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2012, pp. 88–89.

[7] C.-C. Hsu *et al.*, "An 11b 800 MS/s time-interleaved ADC with digital background calibration," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2007, pp. 464–465.

[8] S. K. Gupta, M. A. Inerfield, and J. Wang, "A 1-GS/s 11-bit ADC with 55-dB SNDR, 250-mW power realized by a high bandwidth scalable time-interleaved architecture," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2650–2657, Dec. 2006.

[9] S. M. Louwsma, A. J. M. van Tuijl, M. Vertregt, and B. Nauta, "A 1.35 GS/s, 10b, 175 mW time-interleaved AD converter in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 778–786, Apr. 2008.

[10] V. H.-C. Chen and L. Pileggi, "A 69.5 mW 20 GS/s 6b time-interleaved ADC with embedded time-to-digital calibration in 32 nm CMOS SOI," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 380–381.

[11] L. Kull *et al.*, "A 90 GS/s 8b 667 mW 64 x interleaved SAR ADC in 32 nm digital SOI CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 378–379.

[12] B. D. Sahoo and B. Razavi, "A 10-b 1-GHz 33-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1442–1452, Jun. 2013.

[13] S. Hashemi and B. Razavi, "A 7.1 mW 1 GS/s ADC with 48 dB SNDR at Nyquist rate," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1739–1750, Aug. 2014.

[14] Y. Zhu, C.-H. Chan, S.-W. Sin, S.-P. U, and R. P. Martins, "A 34fJ 10b 500 MS/s partial-interleaving pipelined SAR ADC," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2012, pp. 90–91.

[15] S.-H. W. Chiang, H. Sun, and B. Razavi, "A 10-Bit 800-MHz 19-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 935–949, Apr. 2014.

[16] E. Iroaga and B. Murmann, "A 12-bit 75-MS/s pipelined ADC using incomplete settling," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 748–756, Apr. 2007.

[17] J. Hu, N. Dolev, and B. Murmann, "A 9.4-bit, 50-MS/s, 1.44-mW pipelined ADC using dynamic source follower residue amplification," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1057–1066, Apr. 2009.

[18] Y. Chai and J.-T. Wu, "A 5.37 mW 10b 200 MS/s dual-path pipelined ADC," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 462–463.

[19] Y.-C. Huang and T.-C. Lee, "A 10b 100 MS/s 4.5 mW pipelined ADC with a time sharing technique," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2010, pp. 300–301.

[20] C.-C. Liu *et al.*, "A 10b 100 MS/s 1.13 mW SAR ADC with binary-scaled error compensation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2010, pp. 386–387.

[21] Y. Zhu *et al.*, "A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.
[22] S. Lee, A. P. Chandrakasan, and H.-S. Lee, "A 1 GS/s 10b 18.9 mW time-interleaved SAR ADC with background timing-skew calibration," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 384–385.
[23] N. Le Dortz *et al.*, "A 1.62 GS/s time-interleaved SAR ADC with digital background mismatch calibration achieving interleaving spurs below 70 dBFS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 386–387.
[24] D. Stepanović and B. Nikolić, "A 2.8 GS/s 44.6 mW time-interleaved ADC achieving 50.9 dB SNDR and 3 dB effective resolution bandwidth of 1.5 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 971–982, Apr. 2013.
[25] C. H. Law, P. J. Hurst, and S. H. Lewis, "A four-channel time-interleaved ADC with digital calibration of interchannel timing and memory errors," *IEEE J. Solid-State Circuit*, vol. 45, no. 10, pp. 2091–2103, Oct. 2010.
[26] V. Divi and G. W. Wornell, "Blind calibration of timing skew in time-interleaved analog-to-digital converters," *IEEE J. Sel. Topics Signal Process.*, vol. 3, no. 3, pp. 509–522, Jun. 2009.
[27] G. D. Cain, N. P. Murphy, and A. Tarczynski, "Evaluation of several variable FIR fractional-sample delay filters," in *Proc. IEEE Int. Conf. Acoust., Speech, Signal Process. (ICASSP)*, vol. 3. Apr. 1994, pp. 621–624.
[28] C. W. Farrow, "A continuously variable digital delay element," in *Proc. IEEE Int. Symp. Circuits and Syst.*, vol. 3. Jun. 1988, pp. 2641–2645.
[29] Q. Lei, Y. Zheng, D. Zhu, and L. Siek, "A statistic based time skew calibration method for time-interleaved ADCs," in *Proc. IEEE Int. Symp. Circuits Syst.*, Jun. 2014, pp. 2373–2376.
[30] P. J. A. Harpe *et al.*, "A 26 μW 8 bit 10 MS/s asynchronous SAR ADC for low energy radios," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, Jul. 2011.
[31] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.
[32] F. Kuttner, "A 1.2V 10b 20MSample/s non-binary successive approximation ADC in 0.13-μm CMOS," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2002, pp. 176–177.
[33] S.-W. Chen and R. W. Brodersen, "A 6b 600 MS/s 5.3 mW asynchronous ADC in 0.13 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 2350–2359.
[34] L. Qiu, K. Tang, Y. Zheng, and L. Siek, "A flexible-weighted non-binary searching technique for high-speed SAR-ADCs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 8, pp. 2808–2812, Aug. 2016.
[35] T. Ogawa *et al.*, "SAR ADC that is configurable to optimize yield," in *Proc. IEEE Asia–Pacific Conf. Circuits Syst. (APCCAS)*, Dec. 2010, pp. 374–377.
[36] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. SSC-24, no. 5, pp. 1433–1440, Oct. 1989.
[37] M. El-Chammas and B. Murmann, "General analysis on the impact of phase-skew in time-interleaved ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 5, pp. 902–910, May 2009.
[38] B. Murmann. *ADC Performance Survey 1997–2016 Stanford Univ*. Accessed: 2016. [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html
[39] A. G. Dempster, S. S. Dimirsoy, and I. Kale, "Designing multiplier blocks with low logic depth," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2002, pp. 773–776.
[40] L. Qiu, T. Kai, Y. Zhu, L. Siek, Y. Zheng, and U. Seng-Pan, "A 10-bit 1 GS/s 4-way TI SAR ADC with tap-interpolated FIR filter based time skew calibration," in *IEEE ASSCC Dig. Tech. Papers*, Nov. 2016, pp. 77–80.
[41] C.-Y. Lin, Y.-H. Wei, and T.-C. Lee, "A 10b 2.6 GS/s time-interleaved SAR ADC with background timing-skew calibration," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 468–469.
[42] J. Zhong, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "Thermal and reference noise analysis of time-interleaving SAR and partial-interleaving pipelined-SAR ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2196–2206, Sep. 2015.
[43] S. H. Zhao and S. C. Chan, "Design and multiplierless realization of digital synthesis filters for hybrid-filter-bank A/D converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 10, pp. 2221–2233, Oct. 2009.

Lei Qiu received the B.Sc. and M.Sc. degrees in electrical engineering from Southeast University, Nanjing, China, in 2009 and 2011, respectively, and the Ph.D. degree in electrical and electronics engineering from Nanyang Technological University, Singapore, in 2016.

Since 2015, he has been with Infineon Technologies Asia Pacific Pte Ltd., Singapore. His current research interests include high-speed high-resolution low-power A/D converters design.

Dr. Qiu was a recipient of the Student Travel Grant Award at ASSCC 2016.

Kai Tang received the B.S. degree in information and computing science, the M.S. degree in software engineering (IC design), and the Ph.D. degree in circuits and system from Southeast University, Nanjing, China, in 2005, 2008, and 2014, respectively. During his master and Ph.D. pursuit, he was involved in ultrahigh-speed ADC (sampling rate > 10 GS/s) design and implementation.

From 2013 to 2014, he was with the School of Electrical and Electronic Engineering, Nanyang Technological University (NTU), Singapore, as a Ph.D. International Exchange Student. He is currently a Research Fellow with Virtus, IC Design Center of Excellence, NTU, Singapore, where he is involved in analog circuits and data converter design for CMOS radar chip.

Yuanjin Zheng (SM'16) received the B.Eng. (honors) and M. Eng. degrees from Xian Jiaotong University, Xian, China, in 1993 and 1996, respectively, and the Ph.D. degree from Nanyang Technological University, Singapore, in 2001.

From 1996 to 1998, he was with the National Key Lab of Optical Communication Technology, University of Electronic Science and Technology, Chengdu, China. In 2001, he joined the Institute of Microelectronics, A∗STAR, Singapore, and became a Group Technical Manager. Since then, he has led in developing various wireless systems and CMOS integrated circuits, such as Bluetooth, WLAN, WCDMA, UWB, RF SAW/MEMS Radar, and wireless capsule imager. Most of the projects collaborated with industries. Since 2009, he has been an Assistant Professor with Nanyang Technological University, where he is involved in various radar system developments and hybrid circuit and device (GaN, SAW, MEMS) designs. He has authored or coauthored over 220 international journal and conference papers and five book chapters, and holds 22 filed patents. He has conducted and completed projects with total funding over $18 million.

Dr. Zheng was a recipient of the Best Graduate Student Thesis Award. He has served as guest editor and associate editor. He has been organizing several conferences as TPC Chair and Session Chair.

Liter Siek received the B.A.Sc. degree from the University of Ottawa (OU), Ottawa, ON, Canada, the M.Eng.Sc. degree from the University of New South Wales, Sydney, NSW, Australia, and the Ph.D. degree from Nanyang Technological University (NTU), Singapore.

From 1981 to 1983, he was employed in a couple of companies in the area of automation and control. From 1983 to 1985, he was an IC Design Engineer with European semiconductor Powerhouse, SGS (now known as ST Microelectronics), Milan, Italy, where he was involved in the central Research and Development Laboratories for Linear IC, designing ICs for cordless telephone and motor regulator. From 1985 to 1987, he was with the same company situated in Asia Pacific Design Centre, SGS, where he was involved in IC design for monolithic power ICs in bipolar technology. Since 1987, he has been with the School of Electrical and Electronic Engineering, NTU. His current research interests include the analog/mixed signal ICs especially low-voltage low-power circuits, power management ICs, PLLs, and data converters.

Dr. Siek has received numerous of teaching excellence awards as well as the Nanyang Award for Excellence in Teaching. He was the Director of VIRTUS, IC Design Center of Excellence from 2012 to 2015 as well as the Director for the Joint NTU-TUM MSc(IC Design) Program from 2007 to 2015. He is currently the Lead for the Joint NTU-TUM PhD Program. He has conducted numerous Analog/Mixed Signal IC design short courses as well as providing technical consultancy for the industry. He is actively involved in the IEEE SSCS Singapore Chapter.

Yan Zhu (S'10–M'16) received the B.Sc. degree in electrical engineering and automation from Shanghai University, Shanghai, China, in 2006 and the M.Sc. and Ph.D. degrees in electrical and electronics engineering from the University of Macau, Macao, China, in 2009 and 2011, respectively.

She is currently an Assistant Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. She has authored more than 30 technical journal and conference papers in her field of interests, and holds three U.S. patents. Her current research interests include low-power and wideband high-speed Nyquist A/D converters as well as digitally assisted data converter designs.

Dr. Zhu was a recipient of the Best Paper Award in ESSCIRC 2014, the Student Design Contest Award in A-SSCC 2011, the Chipidea Microelectronics Prize and Macao Scientific and Technological Research and Development Awards in 2012 and 2014 for outstanding Academic and Research achievements in Microelectronics.

Seng-Pan (Ben) U (S'94–M'00–SM'05–F'16) received the B.Sc. and M.Sc. degrees from the University of Macau (UM), Zhuhai, China, in 1991 and 1997, respectively, and the joint Ph.D. degree (honors) in high-speed analog IC design from UM and the Instituto Superior Técnico (IST), Lisbon, Portugal, in 2002.

He has been with the Faculty of Science and Technology, UM, since 1994, and is currently Professor and Deputy Director of State Key Laboratory of Analog and Mixed-Signal (AMS) VLSI. From 1999 to 2001, he was a Visiting Research Fellow with the Integrated CAS Group, Center of Microsystems, IST. In 2001, he co-founded the Chipidea Microelectronics (Macau), Ltd., as the Engineering Director, and since 2003, the corporate VP-IP Operations Asia Pacific for devoting in advanced AMS Semiconductor IP product development. The company was acquired in 2009 by the world leading EDA & IP provider Synopsys Inc. (NASDAQ: SNPS), currently as Synopsys Macau Ltd. He is also the corporate Senior Analog Design Manager and Site General Manager. He has authored or co-authored 140+ publications, four books in Springer and China Science Press in the area of VHF SC filters, analog baseband for multistandard wireless transceivers and very high-speed TI ADCs. He co-holds nine U.S. patents.

Dr. U was a recipient of 30 research and academic/teaching awards and was a co-recipient of 2014 ESSCIRC Best Paper Award. He is also the Advisor of 30 various international student paper award recipients, e.g., SSCS Pre-doc Achievement Award, ISSCC Silk-Road Award, A-SSCC Student Design Contest, IEEE DAC/ISSCC Student Design Contest, ISCAS, MWSCAS, and PRIME. He was the Macau Founding Chairman received the 2012 IEEE SSCS Outstanding Chapter Award. Both at the first time from Macau, he received the Science & Technology (S&T) Innovation Award of Ho Leung Ho Lee Foundation in 2010, and also The State S&T Progress Award in 2011, the 2012 and 2014 Macau S&T Invention and Progress Awards. In recognition of his contribution in academic research & industrial development, he was awarded by Macau SAR government the Honorary Title of Value in 2010. He was also elected as the "Scientific Chinese of the Year 2012." He is currently the Industrial Relationship Officer of the IEEE Macau Section, Chairman of the IEEE SSCS and CAS/COMM Macau chapter. He was the IEEE SSCS Distinguished Lecturer from 2014 to 2015. He was an A-SSCC 2013 Tutorial Speaker for Energy-Efficient SAR-Type ADCs and has also been with technical review committee of various IEEE journals, e.g., JSSC, TCAS, and TVLSI. He was the Chairman of the LOC of the IEEJ AVLSIWS'04, the TPC Co-Chair of the IEEE APCCAS'08, ICICS'09, and PRIMEAsia'11. He is currently a Financial Chair of the IEEE ASP-DAC'16, TPC of ISSCC, A-SSCC, RFIT, Analog subcommittee chair of VLSI-DAT, and an Editorial Board Member of the *Journal AICSP*.