A 7.8-mW 5-b 5-GS/s Dual-Edges-Triggered Time-Based Flash ADC

Chi-Hang Chan, *Member, IEEE*, Yan Zhu, *Member, IEEE*, Sai-Weng Sin, *Senior Member, IEEE*, U. Seng-Pan (Ben), *Fellow, IEEE*, Rui P. Martins, *Fellow, IEEE*, and Franco Maloberti, *Life Fellow, IEEE*

***Abstract*— This paper proposes a 5-b 5-GS/s time-based flash ADC in 65-nm digital CMOS technology, which utilizes both rising and falling edges of the clock for sampling and quantization. A dual-edge-triggered scheme reduces the dynamic power consumption of a voltage-to-time converter and the clock buffers by half. We doubled both the reset and the available regeneration times by interleaving the time comparators. The ADC has a low input capacitance and the calibration circuit is included on-chip for suppressing various mismatches. The prototype running at 5 GS/s consumes 7.8 mW from a 1-V supply and achieves a signal-to-noise and distortion ratio of 26.19 dB at Nyquist. The resulting figure of merit is 94.6 fJ/conversion-step and the core area is only 0.004 mm^2.**

***Index Terms*— Analog-to-digital converter (ADC), flash, time-based dual-edge-triggered.**

I. Introduction

THE required bandwidth of communication systems has grown rapidly, and applications such as the serial links need GS/s ADCs with great power efficiency and small area. Flash ADC is known as the fastest single channel ADC architecture which relies on the parallel operation of comparators. However for higher resolution, the number of comparators increase exponentially, which not only leads to a large area occupation but also significant amount of power consumption [1]. Another type of ADC architecture relying on massively parallel operation is the time-based ADC which mainly consists of time-to-digital converters (TDCs). The simplest form of a TDC is a digital counter. Thus, both the speed and the energy efficiency are greatly limited by the number of bit counters that also expand rapidly with the bit resolution. While time-domain converters have been widely adopted in sigma delta ADCs for their 1st order noise shaping characteristic [2], [3], in multi-bit SAR ADC for replacing multiple comparators [4] or in the digital slope SAR-assisted ADC, the required long counting period [5] limits their operation in GHz applications.

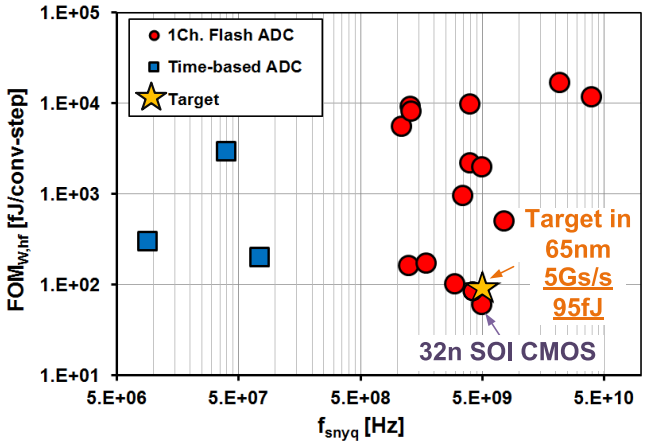

Fig. 1. Time-based and single channel full flash ADCs in state-of-the-art survey.

Thanks to technology scaling, both flash and time-based architectures experienced significant advancements on both speed and energy efficiency due to the small device size and less logic gate delay. The paper in [6] reports a 5 GS/s flash ADC with offset calibration in 32nm SOI CMOS technology achieving a Walden figure of merit (FoM) [7] of 59 fJ/conversion-step. Furthermore, with massively parallel time-domain sub-converters in [8] the sampling speed of the time-based ADC can reach up to 4 GHz; however, the signal bandwidth is only 20 MHz and the SNDR greatly limited by the mismatch between the sub ADCs.

It can be observed from the state-of-the-art ADC survey in Fig. 1, the limitation of the FoM of the single channel full flash ADC designs is mostly within 10 pJ-100 fJ/conversion-step. The Nyquist sampling rate (f_{snyq}) can reach 8 GS/s at high values of the FoM. On the other hand, time-based ADC designs have greater limitation on speed and are only able to achieve 75 MS/s with a 200 fJ/conversion-step FoM. In this work, we would like to explore the possibility of time-based ADC operation beyond GS/s (∼5GS/s) achieving a competitive FoM when compared with other designs in the voltage domain.

Manuscript received July 20, 2016; revised October 6, 2016, December 14, 2016, January 17, 2017, and February 22, 2017; accepted March 6, 2017. Date of publication April 12, 2017; date of current version July 26, 2017. This work was supported by the Research Committee of University of Macau and Macao Science and Technology Development Fund - FDCT under Grant FDCT/053/2014/A1, Grant MYRG2015-00086-AMSV, and Grant SKL/AMS-VLSI/SSW/13-Y3/FST. This paper was recommended by Associate Editor A. M. A. Ali.

C.-H. Chan and Y. Zhu are with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao 999078, China (e-mail: ivorchan@ieee.org).

S.-W. Sin is with the State Key Laboratory of Analog and Mixed-Signal VLSI and Department of ECE, University of Macau, Macao 999078, China.

U. Seng-Pan is with the State Key Laboratory of Analog and Mixed-Signal VLSI and Department of ECE, University of Macau, Macao 999078, China, and also with Synopsys Macau Ltd, Macao 999078, China.

R. P. Martins is with the State Key Laboratory of Analog and Mixed-Signal VLSI and Department of ECE, University of Macau, Macao 999078, China, on leave from the Instituto Superior Técnico/Universidade de Lisboa, 1000-260 Lisbon, Portugal (e-mail: rmartins@umac.mo).

F. Maloberti is with the University of Pavia, 27100 Pavia, Italy.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2017.2682268

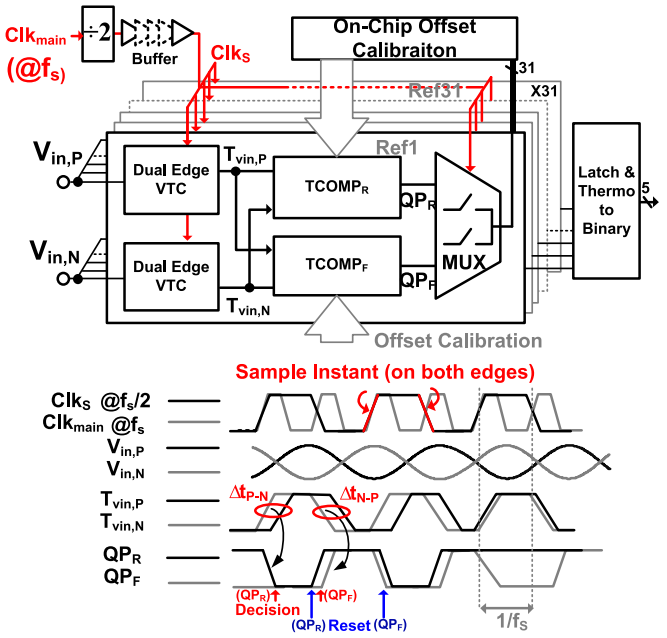

Fig. 2. Proposed ADC architecture and timing diagrams.

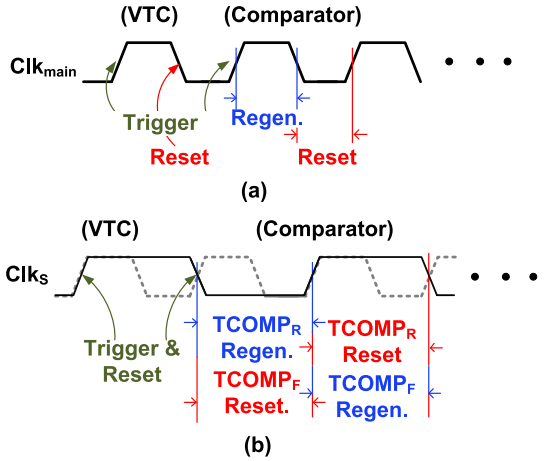

Fig. 3. Timing diagram of a TDC: (a) Conventional and (b) Proposed.

In this paper, we propose a time-based flash ADC which utilizes both raising and falling edges of the clock to sample and quantize the input signal, thus reducing by half the required clocking frequency to save power. The mismatches induced by routings and different clock edges are handled by careful layout and calibration technique. Besides, rather than utilizing the digital counter, the quantization process obtained by time-based comparators in a flash manner can greatly enhance the speed. Further, we embed the time references in each time comparator with accuracy ensured by an on-chip calibration circuit. The prototype realizes in 65nm CMOS technology and achieves 5 GS/s at 1 V supply with a core area of only 0.004 mm^2. The Nyquist SNDR is 26.19 dB and it consumes 7.8 mW power, yielding a Walden FoM at Nyquist of 94.6 fJ/conversion-step. The proposed ADC achieves the highest sampling rate among the time-based ADCs. When comparing with the other flash ADCs in a similar resolution (5-6b), the prototype achieve a competitive FoM in 3-5 GHz sampling rate.

The paper is organized as follows. We first introduce the proposed time-based ADC architecture in section II. Section III describes the circuit implementations of the main building blocks. Next, we present a design analysis in detail in Section IV. Finally, we discuss the measurement results in Section V.

II. Proposed Time-Based ADC Architecture

Fig. 2 illustrates the functional block and timing diagrams of the ADC. The 5b prototype consists of a frequency divider, 31 dual-edge-triggered voltage-to-time converters (VTCs), 31 rising and falling edge time comparators (T_{COMPR} and T_{COMPF}) followed by 2-to-1 multiplexers (MUX) at their outputs, a latch, a thermometer-to-binary decoder and an on-chip calibration circuit. Instead of being processed in the voltage domain, the differential inputs ($V_{in,P}$ and $V_{in,N}$) are first sampled and converted simultaneously to time ($T_{vin,P}$ and $T_{vin,N}$), by 31 VTCs during both the rising and falling edges of the sampling sub-clocks (Clk_S). Clk_S is at half the frequency of the main clock (Clk_{main} = 5 GHz) from the frequency divider. The racing condition between $T_{vin,P}$ and $T_{vin,N}$ as a time difference on both the rising and falling edges ($\Delta t_{P-N}/\Delta t_{N-P}$) can be detected and regenerated into a logic decision (QP_R/QP_F) by T_{COMPR} and T_{COMPF}, respectively. All the 62 time comparators in each slice embed their corresponding time references. The MUX multiplexes both time comparators' outputs which follows by a thermometer-to-binary decoder to decode to 5b from the total 31 units' outputs. Furthermore, we adopt on-chip foreground calibration to suppress the mismatches from the VTCs and time comparators. The decoder is a logic-based gray-encoding in a t-gate with 2 layers of pipeline-latches [9] to reduce the bit error rate (BER).

Fig. 3 (a) shows the timing diagram for a conventional TDC or voltage comparator, where they utilize only single edge of the clock (rising in this example) to trigger and obtain the decision while the other edge serves to activate the reset procedure. This not only reduces the regeneration time but also induces an extra switching activity with no quantization information. Both the available conversion time and power are wasted in the reset phase. In the proposed design (Fig. 3 (b)), we adopt both edges to trigger and reset the VTCs, and their corresponding comparators to give decisions. This provides an relaxed regeneration time for the comparators and reduces the switching frequency of the VTCs and their following buffers by half, thus saving dynamic power. Also, two interleaved comparators, triggered between the rising and falling edge of the Clk_S, have their regenerative and reset times doubled.

A simulation is setup to show the power saving of the proposed architecture comparing with conventional approach. Two cases are depicted in Fig. 4 (a) and (b) respectively. Both cases adopts the same $TCOMP_R$ but the VTCs in conventional approach (Fig. 4 (b)) are reconfigured to single-edge while all the size of transistors are kept the same. Furthermore, the clock generator in the presented design consists of a frequency divider while the conventional approach

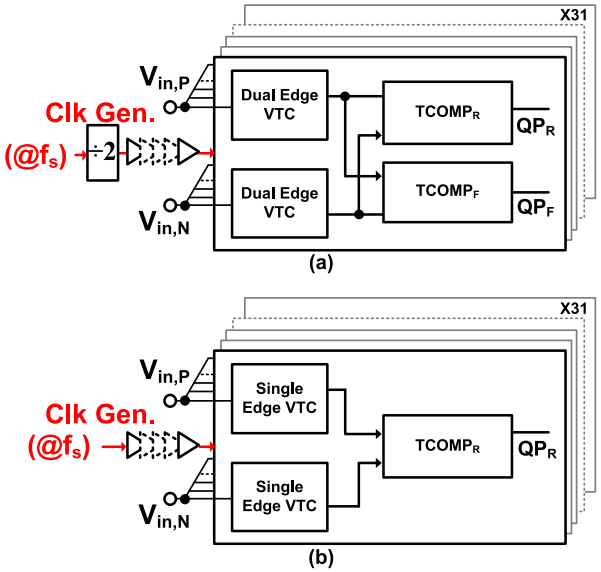

Fig. 4. Simulation comparison setup of (a) Proposed dual-edge and (b) conventional single-edge scheme.

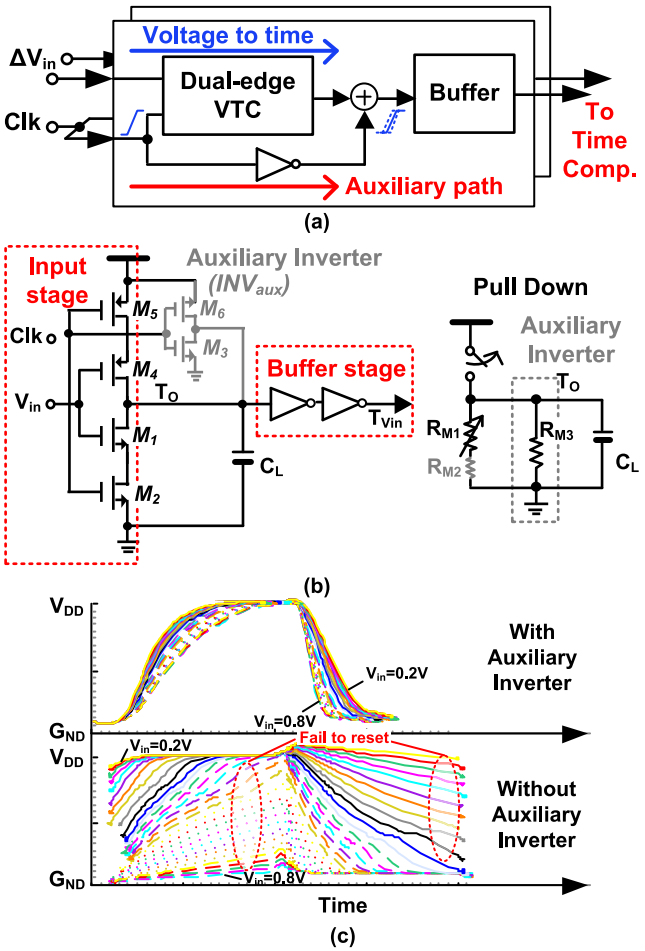

Fig. 5. (a) Conceptual block diagram, (b) Schematic and (c) output signal behavior of dual-edges-trigger VTC with and without the auxiliary inverter.

only needs an inverter chain. From the pre-layout simulation with $f_S = 5$ GHz, the power saving of the dual-edge scheme is around 2.16 times from the conventional one in total, where the clock generator save around 3.8 times and VTC+TCOMP save around 1.5 times. The clock generator save more than 50% power as its power also relate to switching frequency. While only VTC's power is saved and the TCOMP's power is the same in both case, the saving is less than 50%. But when considering the clock generation and buffer circuits, the total power saving is more than 50%.

III. Circuit Implementation and Layout Considerations

A. Dual-Edge-Triggered Voltage-to-Time Converter

Fig. 5 (a) depicts the conceptual block diagram of a key block of the architecture that is the dual-edge-triggered VTC. This circuit contains both sampling and voltage-to-time (V-to-T) conversion functions, and should simultaneously provide a high speed operation with enough driving capability to the following stage. During both the rising and the falling edges of the clock signal (Clk), a pull-up and pull-down network converts the voltage input difference (ΔV_{in}) to a time difference at the output of the dual-edge-triggered VTC. An assisted path from the inverted version of the clock signal feedforwarded to the VTC's output helps to speed up the V-to-T process. Then, the time difference is buffered to drive the following stage for time comparison.

Fig. 5 (b) illustrates a circuit schematic (single-ended) of the dual-edge-triggered VTC. The input stage includes two pull down transistors (M1 and M2) and pull up transistors (M4 and M5) with gates connected to the input (V_{in}) and the clock (Clk), respectively. M2 size is 4× larger than M1 for high speed, and INV_{aux} is induced in parallel to the input stage with clock (Clk) control to further increase the VTC's speed and eliminate the inter-symbol interference (ISI). Unlike the clocked-comparator, Clk signal is connected to both M2 & M5 to pull up and then down the output (T_O) alternatively; while, V_{in} modulates the pulling resistance thus changing the rise/fall time.

Fig. 5 (c) illustrates the difference between the VTC's outputs with and without the auxiliary inverter (INV_{aux}). Without INV_{aux}, the voltage-to-time conversion can occupy a long period dependent on the input voltage. Furthermore, the output of the VTC fails to reset when the input voltage is 0.4 V. With INV_{aux}, the conversion speed is enhanced with a penalty of smaller LSB time difference. While time comparators are often adopted in high resolution ADCs [10] with more than 10b resolution due to their low noise nature, the finer LSB step is not problematic in this 5b design.

When the input stage is in a pull down condition without auxiliary inverter, the discharging time constant τ mainly depends on the equivalent on-resistance of M1 (when M2>>M1) and the capacitive load (C_L), which can be expressed as (ignoring the channel length modulation) [11],

$$\tau = R_{eq,M1} \cdot C_L \approx \frac{3}{4} \frac{C_{L1} V_{DD}}{(W/L)_1 (\mu C_{ox})_n \left(V_{in} - V_{th_n} - V_{DSAT_n}/2\right) V_{DSAT_n}} \quad (1)$$

where $V_{D,SATn}$ is the drain source voltage when the velocity saturation occurs, W_1 and L_1 are the width and length

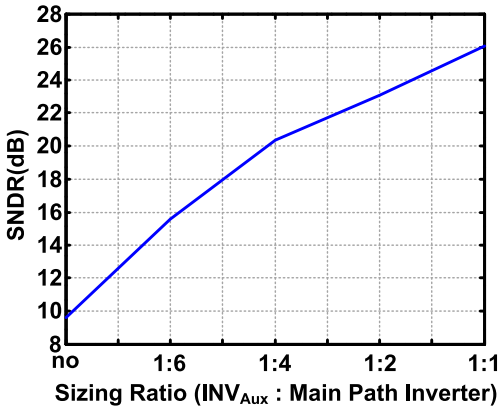

Fig. 6. SNDR degradation due to ISI issue.

of M_1, μ_n and C_{oxn} are the mobility and the oxide capacitance of the NMOS transistor, respectively. V_{in} and V_{thn} are the input voltage and the threshold voltage of M1, respectively. V_{DD} is the supply voltage. When a small input swing is used, the overdrive voltage (V_{in}-V_{thn}) of M1 is small which makes it not able to fully turn-on and leads to slow discharging speed. At high speed, the output is unable to reach ground/supply before the next sampling edge arrives (falling edge in this case) which induces inter-symbol-interference (ISI) in the next subsequent input. Such error is input-dependent with the worst case at the Nyquist rate. On the other hand, with the auxiliary inverter, M3 assists M1 in parallel where the equivalent resistance of M3 does not depend on the input; therefore, T_O can still be reset by M3 when M1 is weak and INV_{aux} also enhances the linearity of the VTC for a large input swing.

The memory effect of the above ISI issue can be explained by the following analysis. The delay (measured at $V_{DD}/2$) control by the V_{in} at the output of the VTC can be expressed as (2) based on (1):

$$V_{DD}/2 = V_O e^{-t/\tau} \Rightarrow t = \ln(2V_O/V_{DD})\tau \qquad (2)$$

where V_O is the initial voltage at T_O,t is the delay and $V_{DD}/2$ is the charge/discharge voltage difference. τ is the discharge time constant. If To is fail to reset correctly, Vo will depend on the previous input which makes t not only relate to current input. Simulation results with different size of INV_{aux} are provided in Fig. 6 to demonstrate impact of the ISI effect on the proposed architecture. Without proper reset of the VTC's output, the current conversion is affected by previous symbols, which gives rise of the overall noise level of the ADC. It can be observed from the simulation results depicted in Fig. 6 that the SNR gradually reduce from 26.03 dB to 9.62 with smaller size of INV_{aux}.

With the extra auxiliary inverter, equation (1) is revised as (assumed M1 and M3 have the same length (L)):

$$\tau \approx \frac{3}{4}\frac{C_L V_{DD} L}{(V_{DSAT}\mu C_{ox})_n} \times \frac{1}{\left[(W_1 V_{in} + W_3 V_{DD}) - \left(V_{th_n} - V_{DSAT_n}/2\right)(W_1 + W_3)\right]} \qquad (3)$$

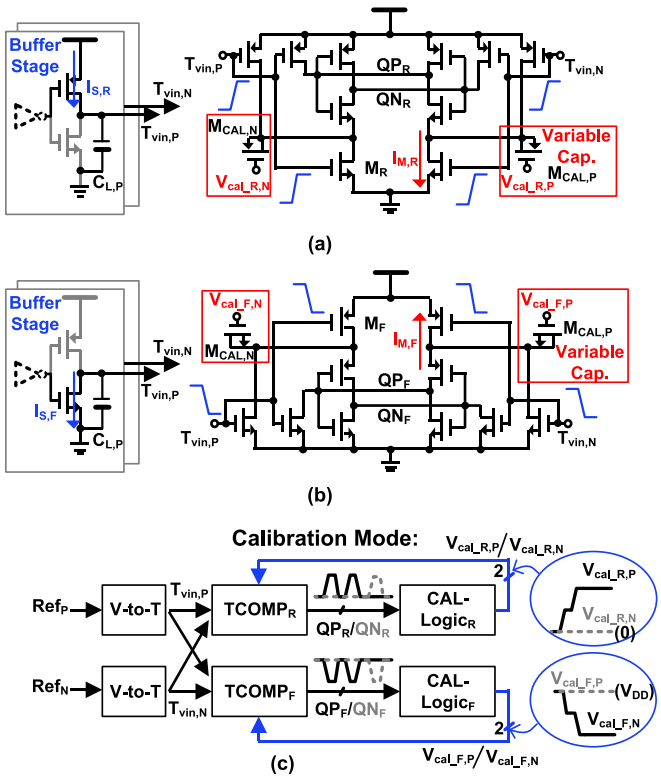

Fig. 7. Circuit schematics of the time comparators (a) rising (b) falling-edge-triggered and (c) calibration scheme.

where W3 is the width of M3. It can be observed from (3) that now the delay has less dependence on the overdrive voltage of M1; This can improve the linearity as now the VTC can still well reset with small or even negative overdrive voltage, but it also reduces the size of the LSB of the converter. While this design only targets for 5b resolution and time comparators can achieve high resolution in deep submicron technology [10], the LSB time step can be reasonably designed in a few pico second range. In this prototype, a 2 ps LSB time step is retained by choosing the size of the auxiliary inverter being 1:1 of the main path. This ratio is chosen mainly based on the ISI issue shown in Fig. 6 above then with careful time comparator design to fulfill the quantization requirement.

B. Reference-Embedded Time Comparators and Calibration

Fig. 7 (a) and (b) presents the circuit schematics of the time comparators, that use two separated comparators which simultaneously provide time comparison and latch function. The rising- and falling-edge-triggered ($TCOMP_R$ & $TCOMP_F$) time comparators mainly consist of back-to-back NAND and NOR gate, respectively. The operation of the time comparator can be described as follows, while only $TCOMP_R$ is discussed and $TCOMP_F$ works similarly with the falling edge condition. After the voltage difference is converted to a time difference at the rising edge of the clock signal, the time leading output ($T_{inv,N}$/$T_{inv,P}$) enables the corresponding half-circuit NMOS transistor (e.g. M_R). One of the outputs of the back-to-back inverter is pulled to ground faster than the other (due to the time difference) and the outputs eventually regenerate to a

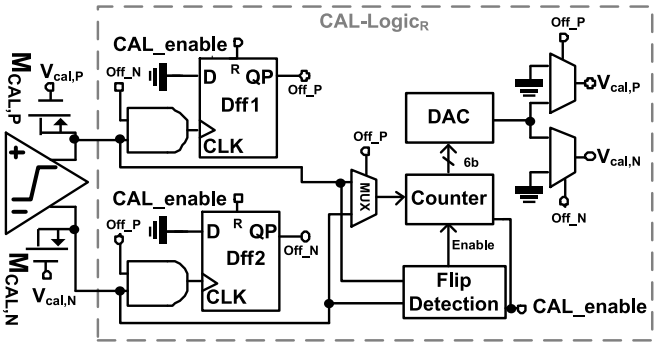

Fig. 8. Circuit schematics of calibration logic.

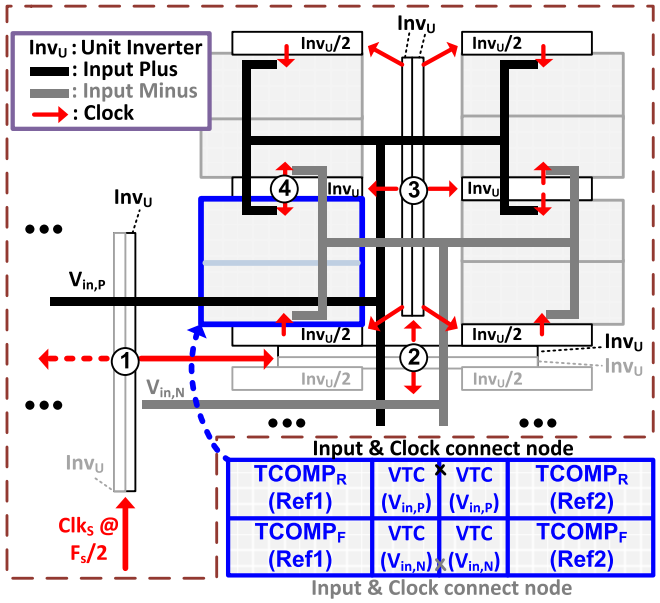

Fig. 9. Layout floorplan.

valid-logic-level. The regeneration speed depends mainly on the time constant (τ) of the comparator which is crucial in order to achieve high speed. In this design, τ is around 8.5 ps (for both $TCOMP_R$ and TCOMP) at TT and 27° C and the available regeneration time is around 20 τ.

The 31 comparators' time references are embedded through the variation of the size of the input pairs based on the following equations ((4) for $TCOMP_R$ and (5) for $TCOMP_F$),

$$t_{ref,R} = \frac{C_L}{I_{S,R}} \cdot \frac{I_{M,R}}{g_{m,MR}} \cdot \frac{\Delta W_R}{W_R} \cdot i \ , (-15 < i < 15) \quad (4)$$

$$t_{ref,F} = \frac{C_L}{I_{S,F}} \cdot \frac{I_{M,F}}{g_{m,MF}} \cdot \frac{\Delta W_F}{W_F} \cdot i, (-15 < i < 15) \quad (5)$$

where C_L is the output load and $I_{S,R/F}$ is the charge/discharge current of the previous buffer stage. $I_{M,R/F}$ is the current drawn from the time comparator and g_m is the transconductance of the latch's input pair, W is the width difference between the input pair and W is the nominal width. It is worth noting that both $I_{S,R/F}$ and $I_{M,R/F}$ vary under different corners, and the accuracy of time references needs to be guaranteed by calibration.

As these time references can drift significantly under process and mismatch variations, calibration is necessary. The calibration schemes must minimal effect the speed of operation while compensating the errors below the quantization level. During the calibration period as Fig. 7 (c) shows, we calibrate the references at the input of the corresponding VTCs. Then, the outputs of the edge-time comparator under calibration are kept feeding back and controlling the voltage of $V_{cal_R,N}/V_{cal_R,P}$ and $V_{cal_R,N}/V_{cal_R,P}$ through the CAL-logic. The CAL-logic consists of a 6b DAC and a logic-flip-detection circuit similar to [12] as shown in Fig. 8 for CAL-$logic_R$. The calibration operation can be explained as following. During calibration (CAL_enable = 1), the first comparison tells the offset polarity of the comparator and either off_P or off_N will become 0. The comparator's output then trigger the counter which controls the DAC to generate the calibration voltage. Depend on the offset polarity, this calibration voltage is applied to either voltage-control-capacitance at the output of the comparator. As the time offsets are adjusted toward the input through the variable capacitor ($M_{CAL,P}$ and $M_{CAL,N}$), the outputs of the comparators flip completing the calibration and the calibration voltage is held. The adopted voltage-controlled-capacitor offset adjustment scheme can reduce calibration bits routing within the core thus saving area. The same scheme is applied to all 62 comparators one-by-one in sequence to calibrate the mismatches on the separated edges path in different time comparators ($TCOMP_R$ and $TCOMP_F$). The calibration range is designed to cover 5 ps time offset (equivalently ~300mV input-referred offset) and its accuracy needs to be up to 1/2 LSB of 5b. A 6b DAC is adopted in the calibration to adjust the calibration voltage of the voltage-variable-capacitor to achieve the target range and the accuracy requirement. The DAC consists of a resistive ladder and a mux tree. The 2 ladders are shared between the 62 calibration and each has their own mux tree and logic circuits. Since the sensing path of the calibration includes the VTC and the time comparators, the variation on the time reference and VTCs are all calibrated.

C. Layout Consideration

The layout floorplan is illustrated in Fig. 9. The differential inputs ($V_{in,P}$ and $V_{in,N}$) are allotted as an H-tree fashion and routed with a grid-shifted based on the unit VTC+TCOMP cell connection. All the overlapped routings are sealed with ground to avoid undesired crosstalk. This maintains a constant distance between the differential inputs and each VTC thus reducing the routing mismatch. The clocks are planned in a grid form and distributed with buffer inverters to each unit VTC+TCOMP cell. The size of the inverters is large for high speed buffering as well as better matching. The unit sized inverter (Inv_U) is a tall cell with only two fingers in the PMOS and NMOS transistors which not only helps to provide a buffering function as well as to distribute the clock signal. The clock distribution grid with its buffers is planned along with the differential inputs to keep the same routing distance to each VTC.

The estimation of the total variation due to routing can be obtained in the following: The length of the input routing

(the longest in this design) is about 77 μm long and 0.6 μm wide in the top thick metal layer which has a nominal resistance R_{nor} and capacitance of ~60 Ω and ~50 fF, respectively. While the standard deviation of the parasitic capacitance due to the interconnection can be as small as 0.1%, the resistance often can be up to around 0.2% (structure B in [13]). Even the wiring structure in [13] is different from this design, it can be found that the mismatches are mainly depended on the number of VIAs and area in [13]. We pick the worst reported structure in [13] as our reference which has >13× R_{nor} than our design for worst case consideration. When, we consider the variation on the routing resistance which can be found as,

$$\sigma_{R,con} = R_{nor} \cdot 0.2\% = 60\Omega \cdot 0.2\% = 0.012\Omega \qquad (6)$$

where R_{nor} is the nominal routing resistance, W and L is the routing width and length, respectively. The variation induced by routing is only 0.088 Ω which is very small when comparing it with device mismatch. Thus, this contribution on the overall mismatch is negligible.

IV. Circuit Non-Idealities

Various circuit non-idealities, such as clock skew, bandwidth mismatch and VTC's nonlinearity affect the performance of high-speed data converters. The clock skew and bandwidth mismatch error is mainly induced by clock distributions, mismatch between the basic cells and in our specific case by the different rising and falling voltage-to-time sampling paths. We minimize the clock routing mismatches through a symmetrical floorplan, a careful layout of basic cells and their common centroid placement alleviate mismatches. However, the timing error due to the utilization of different clock edges can be problematic. Therefore, the clock circuit design and relative considerations are one of the most challenging considerations of the converter. Despite the limited resolution at very high speed the above errors can be substantial and in order to limit their effect it is necessary to adopt calibration.

A. Clock Skew and Aperture Error

Even though the floorplan can ensure a certain level of matching between the clock and the input routing to the VTCs, the process and device mismatches can induce both timing and bandwidth mismatches similar to voltage domain interleaved sampling. Besides, the variation on sampling instant in different VTCs causes aperture error similar to flash ADC without sampling. First, we discuss the clock skew error.

The sampling clock is generated from a frequency divider whose output passes through a chain of buffers to reach different VTCs. The process and mismatch variation yields an unsymmetrical rising and falling time deviation, thus leading to image spurs in the spectrum. Since the proposed design targets are 5 GS/s with 5b, the clock skew error between the rising and falling edge as well as among the VTCs must have a standard deviation less than [14],

$$\sigma_{skew} = \sqrt{\frac{M}{M-1} \cdot \frac{2}{3} \cdot \frac{1}{2^N \cdot 2\pi f_{in}}} = 2.3\text{ps} \qquad (7)$$

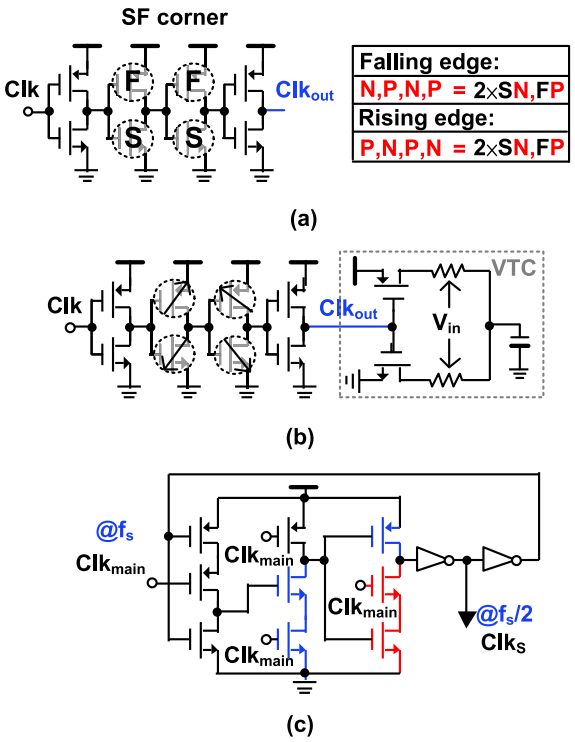

Fig. 10. Clock skew effect on the proposed design: (a) SF Corner, and (b) devices mismatch, (c) circuit schematic of the frequency divider.

where M is the number of channels, N is the bit resolution and f_{in} is the Nyquist input frequency. This imposes a boundary of ~1% error on the 50% duty cycle. Under process and mismatch variation, both the frequency divider and the buffer chain suffer and we will analyze them separately next.

Fig. 10 (a) shows an example in the SF (N-slow-P-fast) corner with 4 inverters in series. Both rising and falling edges of the clock (Clk) pass through 2 slow corner NMOS (S) and 2 fast corner PMOS transistors; therefore, they experience similar variations under the corner condition. On the other hand, the rising and falling edge of Clk passes through various transistors with different device mismatch, all devices in the clock path induce mismatch as illustrated in Fig. 10 (b). Such mismatch error can only be suppressed by enlarging the size of the devices or reducing the number of buffers from the source clock to the VTC. However, the former solution can lead to large power consumption and the latter is not practical due to large routing parasitics. Based on a double-edge-trigger technique, the power consumption from the buffers is inherently reduced by two, and enlarging the devices' size becomes acceptable. It is worth noting that the most problematic scenario is when the NMOS and PMOS transistors are in the SS corner. The slope of both edges are the gentlest thus having the highest sensitivity to the mismatch. The scenario discussed above is not only applicable to the edges mismatch between rising and falling edges but also among the VTCs. In the proposed design, the clock source passes through 4 inverters to the VTC and each has a fan-out of 2. The standard deviation of the sampling time difference between rising and falling edges and among the VTCs under the SS corner should be within the target obtained in (5),

TABLE I
SUMMARY OF TIME-SKEW CONTRIBUTIONS

Absolute time difference from ideal					
@ Corner:	SS	FF	FS	SF	
Divider only	3.4	3.1	2.4	3.3	ps
Inverters only	1.0	0.5	0.7	0.7	ps
Standard deviation σ_{td}					
@Corner(MC):	SS	FF	FS	SF	
Divider only	2.1	1.3	1.5	1.7	ps
Inverters only	1.4	0.9	1.1	1.3	ps

namely,

$$\sigma_{td} = 0.69 \cdot \sigma_{Req} \cdot C_L < 2.3ps \tag{8}$$

where 0.69 is Elmore value scaled by ln(2) to estimate the 50% delay point, C_L is the buffer output load and $\sigma_{Req,R-F}$ is the standard deviation of the equivalent resistance. Since all the fan-outs are constant, the total variation is mainly dependent on the drift of the resistance. For simplicity, assuming that the PMOS and NMOS have the same standard deviation of the equivalent resistance (as PMOS and NMOS have a sizing ratio around 1:2 in the design). Based on 100 samples MonteCarlo simulation results, for a normal biasing (Vgs = $\sim$0.5V_{DD}) 2/0.65 μm LVT NMOS transistor in the adopted process, σ_{Req} is about 200Ω and C_L is 7.6 fF; therefore, the σ_{td} is around 1.06 ps.

Except the buffer chain, the frequency divider also induces mismatch; however, as it is shared among all the channels, it only leads to mismatch between the rising and falling edges. Fig. 10 (c) shows the schematic of the frequency divider which is simply a TSPC D-flip-flop with its output feedback to the input. The transistors in blue and red are the devices that the falling and rising edge of Clks experience through, respectively. It can be noticed that the rising and falling edges pass through an unsymmetrical number as well as type of transistors from the input to the output; therefore, the mismatch can be large especially under corner condition. Table I summarizes the mismatch contributions with post-layout Monte-Carlo simulation results to verify the above assumptions. It can be observed that a significant timing error is generated by the process variation and mostly from the frequency divider circuit. The absolute sampling instant deviation between the rising and falling edges is as large as 3.4 ps at SS corner which would limit the SFDR of the ADC to around 40 dB. The standard deviation of the timing variation under the SS corner is 2.1 ps. We obtain all the Monte Carlo simulation results from 100 samples and the worst case SFDR under process and mismatch variation is 34.5 dB.

As the timing error between rising and falling path limited the SFDR of the ADC, the aperture jitter from time error among the VTCs does not cause interleaving spur at particular frequency. The effect is more spread over the entire Nyquist band and eventually leads to higher noise level. Such error limits the SNR of the ADC which can be demonstrated with

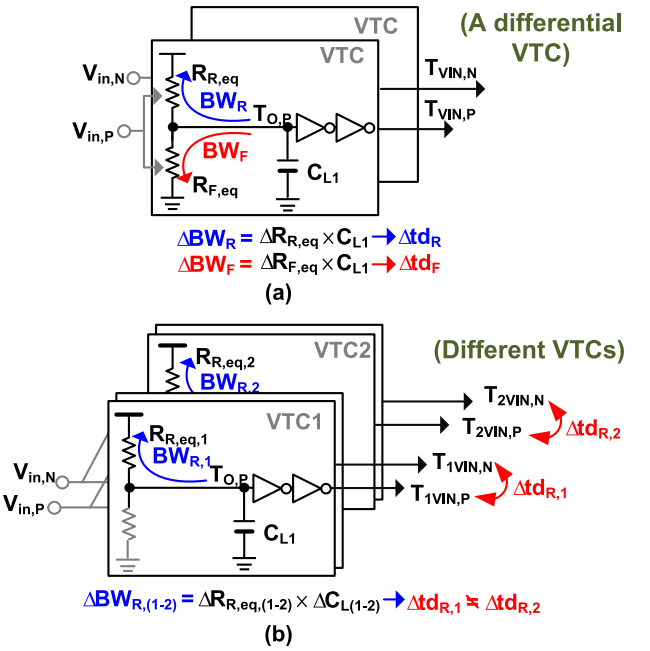

Fig. 11. Bandwidth mismatch effect on the proposed design (a) between the rising and falling edge of a differential VTC (b) among a common edge of different VTCs.

the following equation [15].

$$SNR = -20\log(2\pi f_{in} t_{rms}) \tag{9}$$

where f_{in} is the input frequency and t_{rms} is the root mean square clock jitter. With a front-end sampler, such jitter often limited by the thermal noise. However, as there is no S/H, the aperture jitter is limited by the mismatch on the clock distribution in this design. While the devices mismatch from the clock buffer for each VTC is suppressed by enlarging the size of the transistors, the routing is handled by a symmetrical floorplan. From post-layout MC simulation, the aperture jitter is $\sim$3.5 ps_{rms} which limits the SNR of the ADC at 2.5 GHz input frequency to around 25 dB.

B. Bandwidth Mismatch

Since the VTC's sampling is based on signal-modulated resistance at the charge/discharge path as indicated in (1), the bandwidth mismatch between both paths is directly reflected as different time constants among the rising and falling edges of the VTC (case 1), and among the VTCs in different slices (case 2). Fig. 11 (a) depicts the bandwidth mismatch between the rising and falling edges within a differential VTC pair (case 1). The rising and falling path bandwidth mismatches (BW_R/BW_F) are mainly due to the device mismatch causing variation on the equivalent on-resistance of the input transistors ($R_{R,eq}/R_{F,eq}$). Such mismatches can be considered simply as a delay (td_R/td_F) since they are originated from the RC time constant. Such delay variations are equivalent to time offset and possible to be corrected by the calibration circuit.

Fig. 11 (b) illustrates the bandwidth mismatch among different VTCs with the common edge ($BW_{R,(1-2)}$) (case 2), caused by the variation of the equivalent on-resistance ($R_{R,eq,\ (1-2)}$)

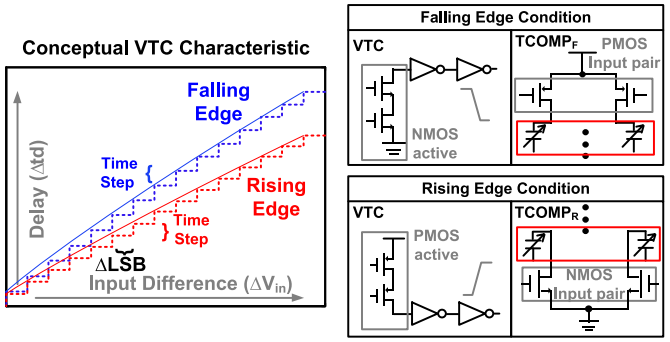

Fig. 12. VTC's nonlinearity and calibration scenario.

and the loading capacitance ($C_{L(1-2)}$). Only the rising edge analysis is shown while the falling edge is similar. Bandwidth mismatch across different VTCs leads to variation on the converted time difference among the VTCs ($td_{R,1} \neq td_{R,2}$). Similarly to the previous case, this difference can be corrected by the calibration circuit as it simply acts as offset of the time comparator. While the rising edge mismatch is corrected by $TCOMP_R$, $TCOMP_F$ calibrates the corresponding mismatch in the falling edge.

C. VTC Nonlinearity

Nonlinearity of the VTC limits the performance of the conversion accuracy. Therefore, the VTC is often placed in the backend of a sub-ranging type of ADC which handles a smaller input range [4]. Due to the calibration circuit and the auxiliary inverter, this design has better tolerance to the nonlinearity of the VTC. As the auxiliary inverter greatly reduces the ISI, the nonlinearity of the VTC can be addressed by the calibration circuit. Fig. 12 shows the conceptual voltage-to-time characteristic of the rising and falling paths of the VTC and their corresponding adjustment circuit. Since the rising and falling edges utilize different transistors for conversion, their V-to-T curves are different. With large input voltage difference (V_{in}), the time difference (t_d) is monotonically increased but the time step is highly nonlinear. The nonlinear time step (in the same edge and also between the different edges) is corrected at the time comparator ($TCOMP_R$ and $TCOMP_F$) which can be explained as following. During calibration, calibration reference voltages is apply at the input of the VTC. Then, the reference voltages convert to delay by the nonlinear VTC. The time comparator adjusts its time reference according to the delay from the VTC's output. This procedure repeats 62 times for all the time comparators. Therefore, the time references embedded in the time comparators is adaptively adjusted to best fit the nonlinear trip-points caused by the VTC.

V. Experimental Results

Fig. 13 shows the microphotograph and layout of the ADC fabricated in ST 65 nm CMOS. It has a core area of 0.004 mm^2 and a total area of 0.096 mm^2 including calibration. The ADC full-scale input is 0.6 V_{pp} with a common-mode voltage of 0.7 V. With 1 V supply, the power consumption is

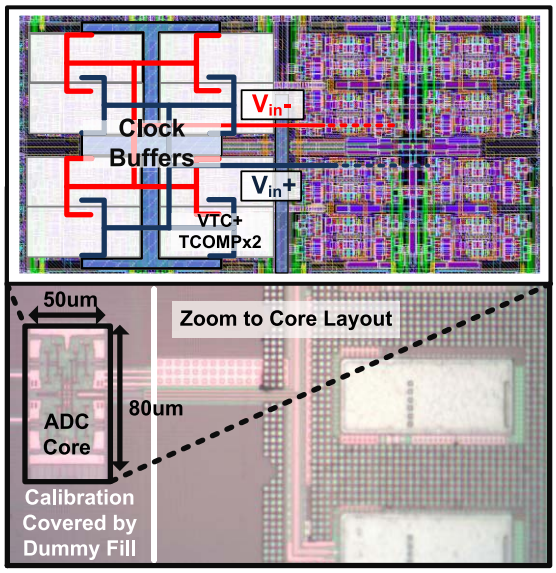

Fig. 13. Chip microphotograph and layout view.

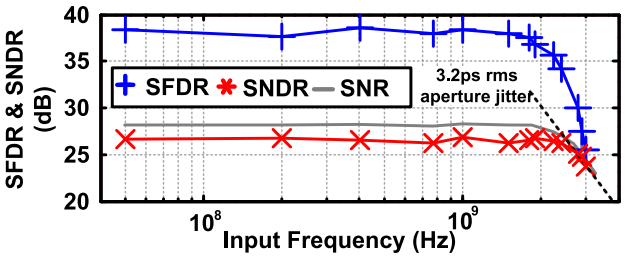

Fig. 14. SNDR and SFDR across different input frequencies.

7.8 mW operating at 5 GS/s (27% in clock buffers, 58% in VTCs and time comparators, and 15 % in the output buffers, latches, decoder and calibration DAC). The calibration is in the foreground and on-chip at the operating frequency (5 GHz). Fig. 14 illustrates the measured SNDR and SFDR versus the input frequency. The SNDR stays above 26.19 dB up to the Nyquist input and drop to 24.23 dB at 3 GHz input frequency. The estimated aperture jitter is around 3.2 ps_{rms}. The SFDR also stays quite flat up to Nyquist input even without the S/H circuit. This is due to the sharp rising and falling edges of the clock for VTC as well as the symmetrical routings. The ADC full swing is also carefully chosen to avoid a large 3rd harmonic in the design. The maximum DNL/INL are suppressed from 4.3/3.5 LSB to 0.83/0.79 LSB, respectively, with calibration depicted in Fig. 15. Fig. 16 shows the frequency spectrum with and without calibration at near-Nyquist-tone. The sampling frequency (f_S) is 5 GS/s, the input frequency (f_{in}) is 2.41 GHz and the output is decimated by 625x. The highest tone that appears in the spectrum is the image spur which is due to the mismatch between VTCs' rising and falling edges as explained in section IV-A. Other tones are caused by the residue offsets in the comparators. The performance of the ADC is mainly limited by SNR which causes by thermal noise of the VTC and time comparator as well as aperture jitter. The input-referred noise of the VTC+TCOMP is around 0.4 LSB, limiting the SNR to around

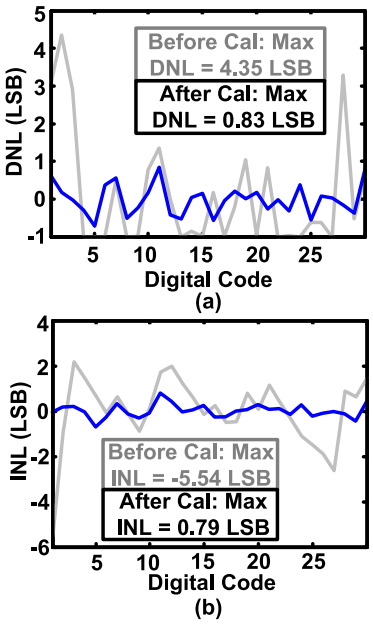

Fig. 15. (a) DNL and (b) INL before and after calibration.

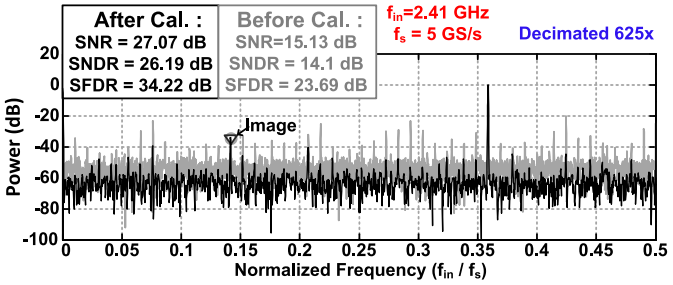

Fig. 16. Output spectrum of the ADC at Nyquist input.

27 dB at low frequency input. At high input frequency, the aperture jitter with 3.2ps$_{rms}$, which is from the noise of the clock generator and the mismatch amount the VTC from front-end, the limits the SNR. Such jitter is estimated from the trend of the degradation on the SNR of the ADC at high frequency input. With technology scaling, the rising and falling time are improved which can benefit this architecture in terms of speed and linearity. Table II summarizes the ADC's performance and compares it with the state-of-the-art. We implement the core with all transistors without passive device but having low input capacitance 66.6 fF with the calibration implemented on-chip, resulting in a Walden FoM of 94.6 fJ/conversion-step. This prototype demonstrates a competitive FoM and achieves the best energy efficiency among high speed (>GS/s) time-based ADCs. Comparing with other time-based ADCs [15], [18] in term of design philosophy, the proposed ADC utilizes clock edges to generate time difference and directly latch this different in flash fashion which enhances the speed of the time-based ADC. While [15] performs the quantization in two steps and [18] quantizes the time difference with counter, their achieved speed or resolution is limited. Besides, both edges of the clock signal are utilized for conversion in this prototype that can save power comparing with conventional voltage-domain flash ADC designs [17].

TABLE II
PERFORMANCE SUMMARY AND BENCHMARK

	VLSI'13[16]	A-SSCC'15[17]	CICC'13[18]	This Work
Architecture	**T-Based	Flash	**T-Based	**T-Based
Technology(nm)	130	65	65	65
Resolution(bit)	13	6	4	5
Sampling Rate(GS/s)	70	3.4	5	5
Supply Voltage(V)	1.3	1.0	1.0	1.0
ENOB@Nyquist (Bit)	10.5	5.39	2.8	4.06
Calibration Type	Gain	Mismatch	Process	Mismatch
Calibration On-chip	N	N	N	Y
Power (mW)	6.38	12.6	34.6	7.8
*FoM (fJ/conv.-step)	38.6	89	1000	94.6
Input Cap. (single) (fF)	N/A	120	N/A	66.6
Core Area (mm^2)	0.5	0.034	0.08	0.004
Core + Cal. (mm^2)	*Off-chip Cal.*	0.025	*Off-chip Cal.*	0.096

*FoM = power/(ENOB@Nquist)×f_s **Time-based

VI. CONCLUSIONS

This paper presented a time-based flash ADC which shows the potential of utilizing time domain conversion in very high speed ADC designs. With the proposed dual-edge-triggered scheme, the power consumption of the VTCs and the clock buffer circuits are greatly reduced; therefore, the prototype can achieve competitive energy efficiency when compared with other voltage domain ADC designs. Through the cooperation among the calibration circuit and the interleaved rising and falling edges comparators, the design is able to operate at 5 GS/s with a 26.19 dB SNDR at Nyquist input. The achieved SFDR is 34.22 dB which is little bit worse than the simulation result in Table I. While results in Table I only considers the variation in the active components of the clock, the routing of the input and the clock signal can induce small overhead thus leading to a bit worse measurement result. The proposed architecture is also suitable for technology scaling due to its pure dynamic power characteristic and the utilization of only CMOS devices.

REFERENCES

[1] H. Chung, A. Rylyakov, Z. T. Deniz, J. Bulzacchelli, G.-Y. Wei, and D. Friedman, "A 7.5-GS/s 3.8-ENOB 52-mW flash ADC with clock duty cycle control in 65 nm CMOS," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2009, pp. 268–269.

[2] A. Iwata, N. Sakimura, M. Nagata, and T. Morie, "The architecture of delta sigma analog-to-digital converters using a voltage-controlled oscillator as a multibit quantizer," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 7, pp. 941–945, Jul. 1999.

[3] S. Zaliasl, S. Saxena, P. K. Hanumolu, K. Mayaram, and T. S. Fiez, "A 12.5-bit 4 MHz 13.8 mW MASH ΔΣ modulator with multirated VCO-based ADC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 8, pp. 1604–1613, Aug. 2012.

[4] J. P. Mathew, L. Kong, and B. Razavi, "A 12-bit 200-MS/s 3.4-mW CMOS ADC with 0.85-V supply," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2015, pp. C66–C67.

[5] C. C. Liu, "27.4 A 0.35 mW 12b 100 MS/s SAR-assisted digital slope ADC in 28 nm CMOS," in *ISSCC Dig. Tech. Papers*, Jan. 2016, pp. 462–463.

[6] V. H.-C. Chen and L. Pileggi, "An 8.5 mW 5 GS/s 6b flash ADC with dynamic offset calibration in 32 nm CMOS SOI," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2013, pp. 264–265.

[7] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Sel. Areas Commun.*, vol. 17, no. 4, pp. 539–550, Apr. 1999.

[8] Y.-G. Yoon and S. Cho, "A 1.5-GHz 63dB SNR 20 mW direct RF sampling bandpass VCO-based ADC in 65 nm CMOS," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2009, pp. 270–271.
[9] C. L. Portmann and T. H. Y. Meng, "Power-efficient metastability error reduction in CMOS flash A/D converters," *IEEE J. Solid-State Circuits*, vol. 31, no. 8, pp. 1132–1140, Aug. 1996.
[10] A. Agnes, E. Bonizzoni, P. Malcovati, and F. Maloberti, "A 9.4-ENOB 1V 3.8 μW 100 kS/s SAR ADC with time-domain comparator," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 246–610.
[11] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits*, 2nd ed. Upper Saddle River, NJ, USA: Pearson Education, 2003, pp. 144–189.
[12] C.-H. Chan, Y. Zhu, S.-W. Sin, S.-P. U, R. P. Martins, and F. Maloberti, "A 5-bit 1.25-GS/s 4x-capacitive-folding flash ADC in 65-nm CMOS," in *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2154–2169, Sep. 2013.
[13] J. Deveugele, L. Yao, M. Steyaert, and W. Sansen, "Mismatch characterisation of chip interconnect resistance," in *Proc. Int. Conf. Microelectron. Test Struct. (ICMTS)*, Apr. 2005, pp. 183–186.
[14] M. El-Chammas and B. Murmann, "General analysis on the impact of phase-skew in time-interleaved ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 5, pp. 902–910, May 2009.
[15] N. D. Dalt, M. Harteneck, C. Sandner, and A. Wiesbauer, "On the jitter requirements of the sampling clock for analog-to-digital converters," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 49, no. 9, pp. 1354–1360, Sep. 2002.
[16] T. Oh, H. Venkatram, and U.-K. Moon, "A 70MS/s 69.3dB SNDR 38.2fJ/conversion-step time-based pipelined ADC," in *Proc. Symp. VLSI Circuits*, Jun. 2013, pp. C96–C97.
[17] J. Liu, C.-H. Chan, S.-W. Sin, U. Seng-Pan, and R. P. Martins, "A 89 fJ-FOM 6-bit 3.4 GS/s flash ADC with 4x time-domain interpolation," in *Proc. IEEE A-SSCC*, Jul. 2015, pp. 1–4.
[18] A. R. Macpherson, J. W. Haslett, and L. Belostotski, "A 5 GS/s 4-bit time-based single-channel CMOS ADC for radio astronomy," in *Proc. IEEE CICC*, Sep. 2013, pp. 1–4.

Chi-Hang Chan (S'12–M'15) was born in Macau, China, in 1985. He received the B.S. degree in electrical engineering from the University of Washington, Seattle, USA, in 2008, and the M.S. and Ph.D. degrees from the University of Macau, Macao, China, in 2012 and 2015, respectively. He was an Intern with Synopsys, Macau, during his undergraduate studies. He currently serves as a Research Assistant Professor with the University of Macau. His research interests include Nyquist ADC and mixed signal circuits. His current research mainly focuses on the comparator offset calibration, Flash, and multi-bit SAR ADC. He received the Chipidea Microelectronics Prize and the Macau Science and Technology Development Fund (FDCT) Postgraduates Award (Master Level) in 2012 and 2011, respectively. He also received the Macau FDCT Award for Technological Invention (Second Class) and the Macao Scientific and Technological R&D for Postgraduates Award (Ph.D. Level) in 2014 for outstanding Academic and Research achievements in microelectronics. He was a recipient of the 2015 Solid-State-Circuit-Society (SSCS) Pre-Doctoral Achievement Award. He was also a co-recipient of the 2011 ISSCC Silk Road Award and the Student Design Contest Award in A-SSCC 2011.

Yan Zhu (S'10–M'12) received the B.Sc. degree in electrical engineering and automation from Shanghai University, Shanghai, China, in 2006, and the M.Sc. and Ph.D. degrees in electrical and electronics engineering from the University of Macau, Macao, China, in 2009 and 2011, respectively. She is currently an Assistant Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. She has involved over 15 research projects for low-power and high-performance ADC. She has authored over 30 technical journals and conference papers in her field of interests and holds four U.S. patents. Her research interests include low-power and wideband high-speed Nyquist A/D converters and digitally assisted data converter designs. She received the Chipidea Microelectronics Prize, the Macao Scientific and Technological R&D for Postgraduates Award–Postgraduate Level in 2012 for outstanding Academic and Research achievements in microelectronics, and the Student Design Contest Award in A-SSCC 2011.

Sai-Weng Sin (S'98–M'06–SM'13) received the B.Sc., M.Sc., and Ph.D. degrees in electrical and electronics engineering from the University of Macau, Macao, China, in 2001, 2003, and 2008, respectively. He is currently an Associate Professor with the Faculty of Science and Technology, University of Macau, and the Coordinator of the Data Conversion and Signal Processing Research Line with the State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. He has authored one book *Generalized Low-Voltage Circuit Techniques for Very High-Speed Time-Interleaved Analog-to-Digital Converters* (Springer), holds six U.S. and two Taiwan patents, and over 100 technical journals and conference papers in the field of high performance data converters and analog mixed-signal integrated circuits.

Dr. Sin is/has been a member of Technical Program Committee of the 2013–2016 IEEE Asian Solid-State Circuits Conference, the 2015 International Wireless Symposium, the IEEE Sensors 2011, and the IEEE RFIT 2011–2014 Conference, the Track Chair in TPC of the IEEE TENCON 2015, a Review Committee Member of PrimeAsia 2009 Conference and Technical Program and Organization Committee of the 2004 IEEJ AVLSI Workshop, and the Special Session Co-Chair and a Technical Program Committee Member of the 2008 IEEE APCCAS Conference. He is currently the Secretary of the IEEE Solid-State Circuit Society (SSCS) Macau Chapter (with 2012 IEEE SSCS Outstanding Chapter Award) and the IEEE Macau CAS/COM Joint Chapter (with 2009 IEEE CAS Chapter of the Year Award). He co-supervised the student that got the 2015 SSCS Pre-Doctoral Achievement Award. He was a co-recipient of the 2011 ISSCC Silk Road Award, the Student Design Contest Award in A-SSCC 2011, and the 2011 State Science and Technology Progress Award (second class), China.

U. Seng-Pan (Ben) (S'94–M'00–SM'05–F'16) received the B.Sc. and M.Sc. degrees from the University of Macau (UM), Macau, China, in 1991 and 1997, respectively, and the dual Ph.D. degrees (Hons.) in high-speed analog IC design from UM and the Instituto Superior Técnico (IST), Portugal, 2002 and 2004, respectively.

From 1999 to 2001, he was on leave to the Integrated CAS Group, Center of Microsystems, IST, as a Visiting Research Fellow. He has been with the Faculty of Science & Technology, UM, since 1994, and is currently a Professor and the Deputy Director of the State-Key Laboratory of Analog & Mixed-Signal (AMS) VLSI.

In 2001, he co-founded the Chipidea Microelectronics (Macau), Ltd., as the Engineering Director, and since 2003, the corporate VP-IP Operations Asia Pacific for devoting in advanced AMS Semiconductor IP product development. The company was acquired in 2009 by the world leading Synopsys Macau Ltd. He is also the Corporate Senior Analog & Mixed-Signal Design Manager and the Site General Manager.

He has authored or co-authored over 140 publications and four books in Springer and China Science Press in the area of VHF SC filters, analog baseband for multi-standard wireless transceivers, and very high-speed TI ADCs. He co-holds ten U.S. patents.

Dr. Seng-Pan received approximately 30 research & academic/teaching awards and was a co-recipient of the 2014 ESSCIRC Best Paper Award. He is also the Advisor for approximately 30 various international student paper award recipients, such as SSCS Pre-doc Achievement Award, ISSCC Silk-Road Award, A-SSCC Student Design Contest, IEEE DAC/ISSCC Student Design Contest, ISCAS, MWSCAS, and PRIME. He received the 2012 IEEE SSCS Outstanding Chapter Award as the Macau Founding Chairman. Both at the first time from Macau, he received the Science & Technology (S&T) Innovation Award of Ho Leung Ho Lee Foundation in 2010, and also the State S&T Progress Award in 2011. He also received both the 2012 and 2014 Macau S&T Invention and Progress Awards. In recognition of his contribution in academic research & industrial development, he received the Macau SAR Government Honorary Title of Value in 2010. He was also elected as the Scientific Chinese of the Year 2012.

He is currently the Founding Chairman of the IEEE SSCS and the Chairman of CAS/COMM Macau Chapter. He is appointed a member of the S&T Commission of China Ministry of Education. He was an IEEE SSCS Distinguished Lecturer from 2014 to 2015 and an A-SSCC 2013 Tutorial Speaker. He has also been with the Technical Review Committee of various IEEE journals, such as JSSC, TCAS, and TVLSI. He was the Program Committee/Chair of the IEEJ AVLSIWS, the IEEE APCCAS, the ICICS, the PRIMEAsia, and the IEEE ASP-DAC'16. He is currently TPC of ISSCC, A-SSCC, RFIT, Analog Sub-Committee Chair of VLSI-DAT and an Editorial Board member of the Journal AICSP.

Rui P. Martins (M'88–SM'99–F'08) was born in 1957. He received the bachelor's, master's, Ph.D. and Habilitation degrees for Full Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), University of Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively. He has been with the Department of Electrical and Computer Engineering/IST, University of Lisbon, since 1980.

Since 1992, he has been on leave from IST, University of Lisbon, and is also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he is currently a Chair-Professor since 2013. In FST, he was the Dean of the Faculty from 1994 to 1997, and he has been a Vice-Rector of UM since 1997. Since 2008, after the reform of the UM Charter, he was nominated after open international recruitment, and reappointed in 2013, as a Vice-Rector (Research) until 2018. Within the scope of his teaching and research activities, he has taught 21 bachelor's and master's courses and has supervised (or co-supervised) 40 theses, Ph.D. (19) and master's (21). He has co-authored six books and nine book chapters, holds 16 U.S. and two Taiwan patents, 355 papers, in scientific journals (104) and in conference proceedings (251), and other 60 academic works, in a total of 448 publications. He was a Co-Founder of Synopsys, Macao, in 2001/2002, and created in 2003 the Analog and Mixed-Signal VLSI Research Laboratory of UM, elevated in 2011 to the State Key Laboratory of China (the 1st in Engineering in Macao), being its Founding Director.

Dr. Martins was the Founding Chairman of the IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications from 2005 to 2008 [2009 World Chapter of the Year of IEEE CASS]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on CAS-APCCAS'2008, and was the Vice-President for the Region 10 (Asia, Australia, and the Pacific) of the IEEE CAS Society from 2009 to 2011. He was a member of the IEEE CASS Fellow Evaluation Committee in 2013 and 2014, and the CAS Society Representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS) - the Director of the IEEE. He is currently the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference–ASP-DAC'2016. He was the recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In 2010 was elected, unanimously, as a Corresponding Member of the Portuguese Academy of Sciences (in Lisbon), being the only Portuguese Academician living in Asia. Since then, he was the Vice-President (World) Regional Activities and Membership of the IEEE CAS Society from 2012 to 2013, and an Associate Editor of the IEEE TRANSACTIONS ON CAS II from 2010 to 2013, nominated Best Associate Editor of T-CAS II from 2012 to 2013.

Franco Maloberti (A'84–SM'87–F'96–LF'15) received the Laurea (*summa cum laude*) degree in physics from the University of Parma, Parma, Italy, in 1968, and the Dr. Honoris Causa degree in electronics from the Instituto Nacional de Astrofisica, Optica y Electronica (INAOE), Puebla, Mexico, in 1996. He was a Visiting Professor with ETH-PEL, Zurich, in 1993, and EPFL-LEG, Lausanne, in 2004. He was the TI/J.Kilby Analog Engineering Chair Professor with Texas A&M University and the Distinguished Microelectronic Chair Professor with The University of Texas at Dallas. He is currently a Professor with the University of Pavia, Italy, and an Honorary Professor with the University of Macau, China. His professional expertise is in the design, analysis, and characterization of integrated circuits and analogue digital applications, mainly in the areas of switched capacitor circuits, data converters, interfaces for telecommunication and sensor systems, and CAD for analogue and mixed A-D design. He has written over 500 published papers, six books, and holds 34 patents. He was a recipient of the XII Pedriali Prize for his technical and scientific contributions to national industrial production in 1992. He was a co-recipient of the 1996 Institute of Electrical Engineers (U.K.) Fleming Premium. He has been responsible at both technical and management levels for many research programs, including ten ESPRIT projects and has served the European Commission as an ESPRIT Projects' Evaluator, a Reviewer, and a European Union expert in many European Initiatives. He served the Academy of Finland on the assessment of electronic research in Academic institutions and on the research programs' evaluations. He served the National Research Council of Portugal on a Board for the research activity assessment of Portuguese Universities. He was a member of the Advisory Board of INESC-Lisbon, Portugal. He is the Chairman of the Academic Committee of the Microelectronics Key Laboratory, Macau, China.

Dr. Maloberti was the President of the IEEE CAS Society. He was VP Region 8 of the IEEE CAS from 1995 to 1997, an Associate Editor of the IEEE-TCAS-II, the President of the IEEE Sensor Council from 2002 to 2003, the IEEE CAS BoG Member from 2003 to 2005, and VP Publications IEEE CAS from 2007 to 2008. He was DL of the IEEE SSC Society from 2009 to 2010 and DL IEEE CAS Society from 2006 to 2007 and from 2012 to 2013. He received the 1999 IEEE CAS Society Meritorious Service Award, the 2000 CAS Society Golden Jubilee Medal, and the IEEE 2000 Millenium Medal. He received the 1996 IEE Fleming Premium, the ESSCIRC 2007 Best Paper Award, and the IEEJ Workshop 2007 and 2010 Best Paper Award. He received the IEEE CAS Society 2013 Mac Van Valkenburg Award.