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Systematic analysis and cancellation of kickback noise in a dynamic latched comparator

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Abstract A dynamic latched comparator can suffer from three non-idealities: offset voltage, random noise and kickback noise. Specifically in an analog-to-digital converter (ADC) the kickback noise of a comparator can noticeably affect the settling time and accuracy of the decision. This work offers an analytical treatment of kickback noise generation, and proposes a synchronized kickback noise cancellation technique, which is achieved via placing clocked NMOS-PMOS capacitors at the proper nodes to cancel out effectively those unwanted charges (electrons or holes) under different operating regions of the MOS devices. The technique is clock-rate insensitive and particularly suitable for the SAR-type ADC as it will not alter the charge stored in the capacitor array. Optimized in 65-nm CMOS the kickback noise is $<\pm 0.3$ mV in 30× Monte–Carlo simulations at both 50- and 500-MHz clock rates. For 10-bit resolution in a full scale of 1 V_{pp}, the kickback noise of the proposed comparator comparing with the conventional one is improved by 48×, from 6.27 to 0.13 LSB.

Keywords Analog-to-digital converter (ADC) · CMOS · Dynamic latched comparator · Kickback noise

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1 Introduction

The comparator plays a key role in many types of analog-to-digital converters (ADCs). Its non-idealities can limit the achievable conversion speed and effective number of bits. The fundamental non-idealities are the offset voltage, thermal noise and kickback noise. The offset voltage due to process variation and mismatch can be effectively calibrated [1–3]. Although upsizing the input MOS pair of the comparator can reduce the thermal noise [4], it will contradictorily generate more kickback noise that is proportional to the drain-gate parasitic capacitance of the input MOS pair. Such a kickback noise is dynamic as the input MOS pair in the whole comparison process can operate over a number of regions (i.e., cutoff, saturation and triode), significantly influencing the accuracy of the decision. Figure 1 shows how the kickback noise affects the settling time and accuracy of a 3-bit SAR ADC. Generally, the effect of kickback noise can be significantly reduced by using a differential structure. However, for those applications that need a massive number of ADCs, a single-ended design is more preferable for power and area savings [5, 6] and kickback noise cancellation technique is required.

This paper provides an in-depth analytical treatment of kickback noise in a dynamic latched comparator. The analysis guides the design of a robust synchronized kickback noise cancellation technique, eliminating those unwanted charges at the gate of the input MOS pair at different time intervals. This technique is favorable over [7] that cannot be commonly utilized in SAR-type ADCs because the two inputs have to be shorted together at the instant of kickback noise rejection (i.e., neutralized the charge stored at the capacitance array). Here, the charge is conserved, allowing an efficient utilization of the comparator in all types of ADC.

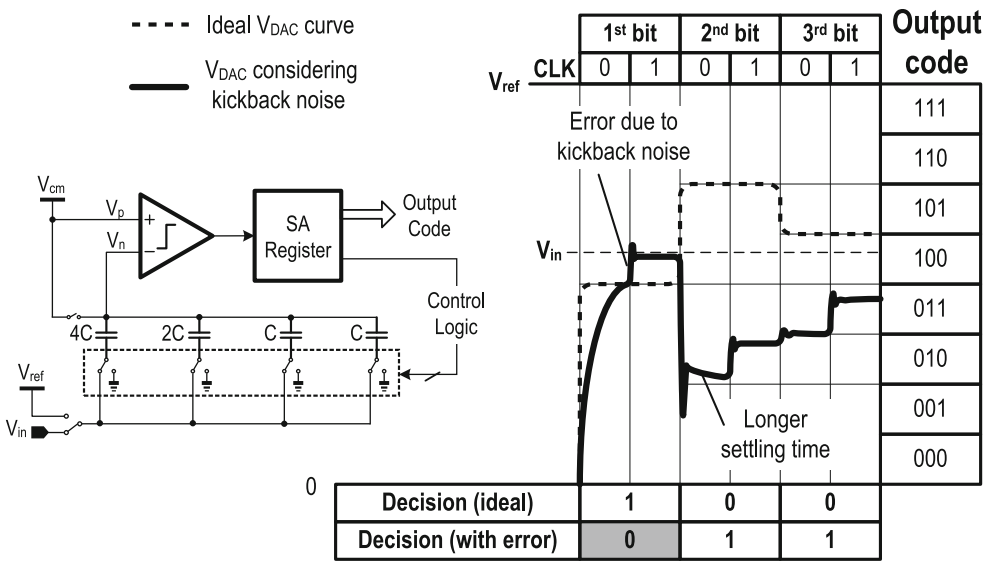

Fig. 1 SAR-type ADC with error code and longer settling time due to kickback noise

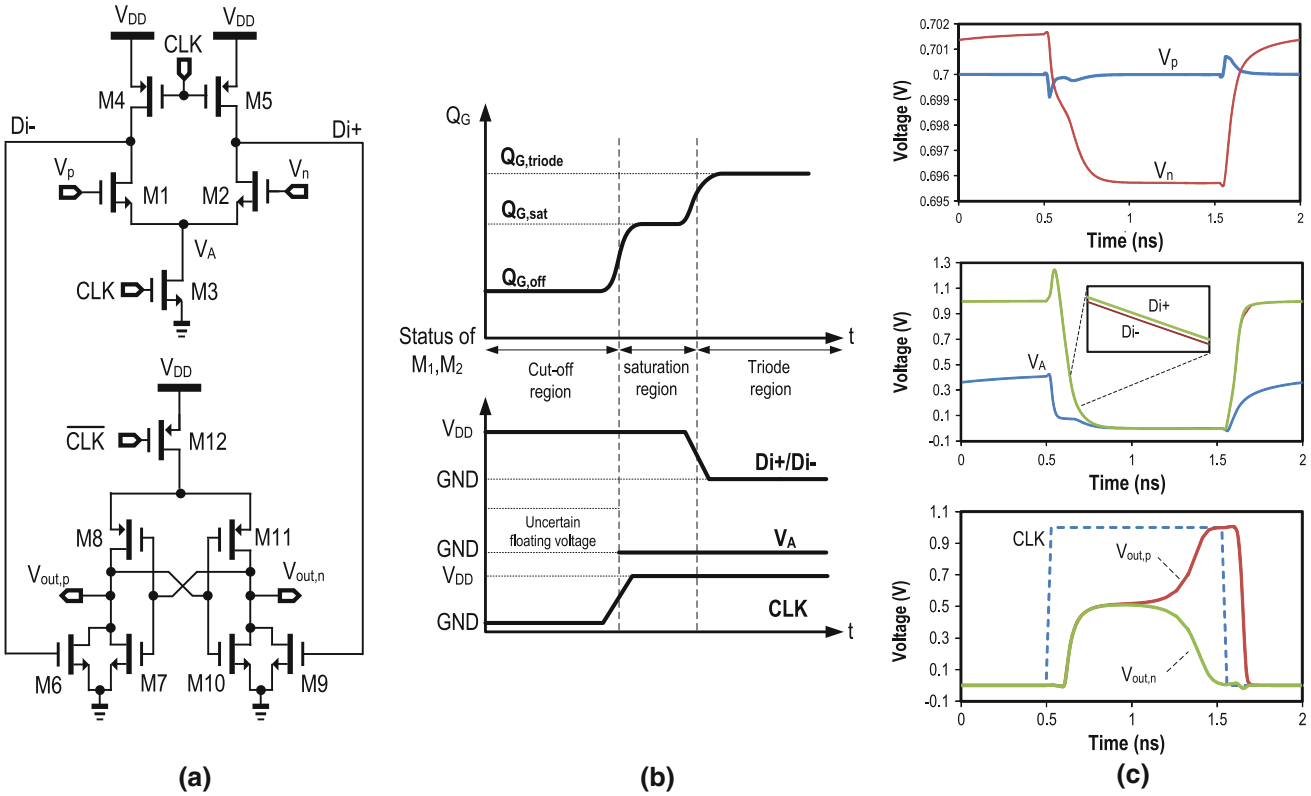

Fig. 2 **a** A conventional dynamic latched comparator. **b** The timing diagram shows the states and charge induced on the gate of M_1 (M_2). **c** The simulated operation voltages of critical nodes

1.1 Kickback noise in a dynamic latched comparator

Figure 2(a) shows a typical dynamic latched comparator from [8]. It has the properties of fast response time, low dynamic power and no static power. Assuming that both V_p and V_n are connected to V_{cm}, and when the clock signal (CLK) is low, both $Di+$ and $Di-$ will be pulled-up to V_{DD}, grounding $V_{out,p}$ and $V_{out,n}$. During this time interval the comparator will be in the reset mode. Node A is floating and therefore V_{GS} is uncertain. The input MOS pair

(M_1 and M_2) has already been turned off since no current can flow from $Di+$ to $Di-$ to node A. The charge induced at the gate of M_1 and M_2 is given by,

$$Q_{G,off} = V_{cm}C_{GB} + V_{GS}C_{GSO} + (V_{cm} - V_{DD})C_{GDO} \quad (1)$$

where C_{GB} is the equivalent capacitance between the gate and substrate. C_{GSO} and C_{GDO} are the gate-source and gate-drain overlap capacitances, respectively. V_{GD} is below 0 V in this region. C_{GB} can be modeled as the series combination of the gate oxide capacitance, WLC_{ox} and the depletion region capacitance, $WL\sqrt{(q\varepsilon_{si}N_{sub}/4\Phi_F)}$, where W and L are the width and length of the transistor, q is electron charge, ε_{si} is the silicon dielectric constant, N_{sub} is the doping concentration of the substrate, and Φ_F is the Fermi potential in the semiconductor [4, 9]. The approximate value of the capacitance can be obtained by performing DC simulation. However, this is just a simplified model since the actual charge calculation is far more complicated [10]. For simplicity and getting design insights, this model will be used to study the mechanism of kickback noise generation.

When the rising edge of CLK happens, M_4 and M_5 are turned off while M_3 becomes on. Node A is grounded first, driving M_1 and M_2 into the saturation region ($V_{GS} > V_t$, and $V_{GD} < V_t$, where V_t is the threshold voltage). At this point, the charges induced throughout the channel can be denoted by $Q_{ch,sat}$ [10], which is given by

$$Q_{ch,sat}(t) = -\frac{2}{3}WLC_{OX}(V_{cm} - V_A(t) - V_t) \quad (2)$$

The minus sign in Eq. (2) indicates that the charges induced in the channel are constituted by electrons (NMOS). In this operating region the channel acts as a shield between the gate and substrate. The induced charge caused by variation of V_G will be provided from the source and drain of the transistor. Thus, C_{GB} is negligibly small when the transistor is turned on and is negligible. The charge induced to the gate is thus given by,

$$\begin{aligned} Q_{G,sat}(t) = &- Q_{ch,sat}(t) + (V_{cm} - V_A(t))C_{GSO} \\ &+ (V_{cm} - Di_+(t))C_{GDO} \end{aligned} \quad (3)$$

From Eqs. (2) and (3), it can be observed that the induced charge depends on V_A that can be time-varying. This is one of the main sources of the dynamic kickback noise.

When M_1 and M_2 are turned on, nodes $Di+$ and $Di-$ start to discharge through them. The rate of discharge depends on the input voltage. The node ($Di+/Di-$) on the side which input voltage (V_p/V_n) is larger will discharge faster. The comparator generates the result depending on the discharging rate of $Di+$ and $Di-$ by triggering the positive feedback formed by the two cross-coupled inverters composed by M_7, M_8, M_{10} and M_{11}. The result is stored at the output until CLK is low again. Then, the comparator continues with the next comparison. As $Di+$ and $Di-$ are small enough in this time interval, M_1 and M_2 will be driven into the triode region and the amount of charge induced on the channel is given by,

$$Q_{ch,Triode}(t) = -WLC_{OX}(V_{cm} - V_A(t) - V_t) \quad (4)$$

Similar to the case in saturation region, C_{GB} is shielded out by the induced channel and thus it can be neglected. The total charge induced at the gate is hence given by,

$$\begin{aligned} Q_{G,triode}(t) = &- Q_{ch,triode}(t) + (V_{cm} - V_A(t))C_{GSO} \\ &+ (V_{cm} - Di_+(t))C_{GDO} \end{aligned} \quad (5)$$

Since both $Di+$ and $Di-$ and V_A will vary over time, the voltage variation will couple back to the gate producing the kickback noise. In this time region, V_{GS} and V_{GD} are both greater than zero and will cause a difference of induced charge on the gate.

Referring to Eqs. (1), (3), and (5) it is obvious that the charges induced at the gate of the input MOS pair are dynamic during the entire comparison and latch operations. Figure 2(b) shows the charge induced on the gate at different instants and operating regions of M_1 and M_2.

The operation can be further illustrated via transistor-level simulations. The comparator shown in Fig. 2(a) is simulated with the gate of M_1 connected to V_{cm} (0.7 V) and with a series internal resistance of 10 Ω (reasonable value for the internal resistance of a voltage source). The gate of M_2 is connected to a capacitor array with total capacitance equal to 1 pF and voltage equal to V_{cm} + 2 mV = 0.702 V. V_{DD} is set to 1 V and the frequency of CLK is set at 500 MHz. In addition, two capacitors of 5fF representing the loads of the subsequent stage are added to the outputs. Figure 2(c) shows the simulated results. It can be observed that V_n keeps on changing even when CLK is low since V_A is still increasing over time. The voltage variation of V_A will couple back to V_n through C_{GSO}. When the rising edge of CLK happens, there are some glitches in both V_p and V_n. They are due to the kickback noise of the input transistors M_1 and M_2. In addition, differing from V_p where the steady voltage will come back to the normal level of 0.7 V, V_n suffers from a permanent voltage drift of about −6 mV until M_2 is re-turned off. This is caused by the charges attracted to the gate of M_2. For the voltage waveform of V_A, $Di+$ and $Di-$, there are glitches at both $Di+$ and $Di-$ caused by the charge injection from M_4 and M_5, respectively. Since M_1 and M_2 had not been turned on yet, the positive charge from their channels will cause $Di+$ and $Di-$ to rise up. This will further increase the kickback noise as the glitch will couple back to the gates of M_1 and M_2 through the gate-drain overlap capacitance. In addition, $Di-$ is discharged faster than $Di+$ due to the kickback noise and voltage shift at the inputs, resulting in an erroneous decision. For the comparison result ($V_{out,p}$ and $V_{out,n}$), since the kickback noises affect the

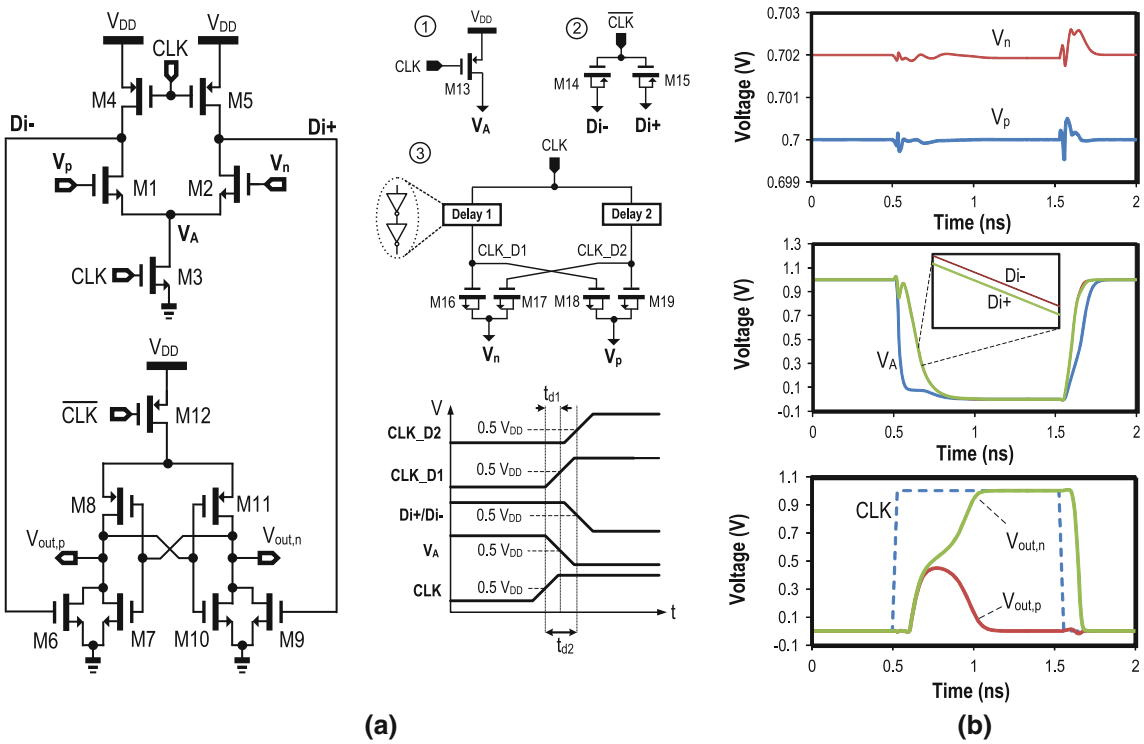

Fig. 3 **a** Proposed dynamic latched comparator with kickback-noise compensation. The extra elements are three sets of clocked NMOS-PMOS capacitors. **b** The simulated operation voltages of critical nodes

voltage at V_p and V_n, the comparator cannot decide the voltage difference correctly. These results show that the kickback noise not only causes glitch at the input and increases the settling time, but also affects the decision making.

From Eqs. (1), (3) and (5), the insight for providing a solution is if the induced charges can be compensated dedicatedly with the proper charge and time during the different operating regions, the kickback noise can be minimized synchronously. The next section proposes a solution under this concept.

1.2 Clocked NMOS-PMOS capacitors for kickback-noise cancellation

Figure 3(a) shows the proposed dynamic latched comparator with three improvements for reducing the kickback noise. The operating principle is basically identical with that in Fig. 2(a). For the first change, M_{13} is added to pull up the node A voltage to V_{DD} when CLK is low. This act removes the uncertain voltage at node A and thus the voltage of the sampling capacitor will not be drifted. The expense of this change is slightly slowing down the recovery time at V_A as is pulled up to V_{DD} in the reset mode.

The second change is by adding two clocked PMOS capacitors M_{14} and M_{15} to node $Di+$ and $Di-$, respectively. The voltages at these two nodes, right after the rising edge of the CLK, are raised rapidly because of the charges injected from the channels of M_4 and M_5. M_{14} and M_{15} can absorb the holes released from them by creating a p-channel at the same time. The sizes of these are approximately half of M_4 (M_5) since roughly half of the charge from the channel is injected to $Di+$ and $Di-$ when the transistors are turned off.

The third change is by adding four more NMOS capacitors M_{16}–M_{19} to the input of the comparator. It can be showed that the charge induced at the gate of M_1 and M_2 is a function of time and depends on their operating regions. It can be modeled as a two-step function with different amplitudes at different time intervals. Thus, in order to cancel the charge loss due to this phenomenon, M_{16}–M_{19} are chosen as NMOS because they can absorb electrons to form a channel when CLK goes high, compensating the electrons repelled from the gate of M_1 and M_2. M_{16} and M_{18} compensate the loss of charge due to switching of the transistors from the off-region to saturation region, whereas M_{17} and M_{19} compensate the loss of charge due to the switching of transistors from saturation to triode regions. There are two delay blocks to synchronize the switching times of the different sets of MOS capacitors to accurately neutralize the charges induced. The delay cells are obtained by cascading two inverters. The first can provide the necessary delay while the second one can control the slope of *CLK_D1* (or *CLK_D2*).

The time diagrams of those MOS capacitors are depicted in Fig. 3(a) as well. When CLK goes high, M_3 is turned on first and V_A will discharge through it gradually. When V_A becomes smaller than $V_{cm} - V_t$, M_1 and M_2 will enter the saturation region and a number of charges will be induced at their gates. The delay block 1 should have a delay time t_{d1} leading *CLK_D1* to increase to V_{DD}, switching on M_{16} and M_{18} simultaneously. As a result, the positive charge induced on the gates of M_1 and M_2 will be compensated by the negative charges induced in the channel of M_{16} and M_{18}, respectively. After that, $Di+$ ($Di-$) will start to discharge through M_1 (M_2) as it has been turned on. When their voltages are smaller than $V_{cm} - V_t$, M_1 and M_2 will be driven into the triode region. Again, the delay block 2 should have a delay time t_{d2} leading *CLK_D2* to be raised to V_{DD} and causing M_{17} and M_{19} to be switched on, compensating the induced charges.

The added NMOS capacitors (M_{16}–M_{19}) will lead to larger input capacitance of the comparator (C_{IN}). Nonetheless, it will not affect the comparison results as it is determined by the polarity of the voltage difference between the input nodes, which is independent on C_{in}.

The performance of the proposed comparator is extensively simulated and assessed using the ST 65-nm CMOS technology. The size of those MOS capacitors is optimized computationally as it depends on the common mode voltage V_{cm}, the gate-drain and gate-source overlap capacitances and the threshold voltage as well as the operation point, thus it is unmanageable to get a handy formulae to pinpoint the device sizes. A suitable delay time for *CLK_D1* and *CLK_D2* can be obtained by tuning the width and length of the PMOS and NMOS transistors of the inverters. The simulation results are shown in Fig. 3(b) under the same conditions of Section II. It can be seen that V_p and V_n will no longer be crossing each other. Thus the comparator can deliver a proper result ($V_p < V_n$). The voltage variation on the capacitor side V_n is suppressed to ± 0.15 mV during the comparison, which is much smaller than the noise of the comparator itself (1.5 mV) [8]. The glitch on V_p is also reduced to ± 0.3 mV, which is also lower than that without compensation (1 mV). Another improvement is that the glitches at $Di+$ and $Di-$ have been reduced and this can lower the kickback noise. The settling time for V_p and V_n after comparison and turned back to reset phase is improved. The settling time of V_p of the conventional comparator is around 1 ns whereas it is just 0.3 ns of the proposed one, extending the workable maximum frequency.

Figure 4(a), (b) show the effectiveness of the proposed comparator versus the conventional one as a function of the input-voltage difference. For a 10-bit ADC with 1-V_{pp} full scale, the LSB is ~ 1 mV. In both $V_n > V_p$ and $V_n < V_p$ cases, the kickback noise reduction is around 48×, from 6.27 to 0.13 LSB. On the other hand, when the input voltage is sufficient large to make the correct decision, the kickback noise will be tolerable for both.

The robustness of the results has been confirmed by Monte–Carlo simulations with process variations and mismatch. Figure 5(a), (b) show the V_p and V_n variations for 30 runs under 50- and 500-MHz clocks, respectively. The ripples on V_p and V_n are both around ± 0.3 mV. The noise margin is adequate and thus the kickback noise will not affect the comparison. The results also showed that the technique is highly insensitive to the CLK rate as the clocked NMOS-PMOS capacitors are *synchronized* with the operation of the comparator. In addition to the Monte–Carlo simulations, the comparator was assessed under different process corners (TT, FF, FS, FS, SS) and temperature (−40 to 125 °C), and the result was plot in Fig. 6. It can be seen that the voltage error can be kept below 1 mV even at extreme temperature (−40 and 125 °C) except for the case of FS corner. The voltage deviation for the conventional comparator is around 6.0–6.9 mV at different corners and temperatures, dominated by the NMOS process corner as the input pairs of the comparator are formed by NMOS and is quite irrelevant to the temperature during the simulations. The sensitivity of the voltage error to the supply voltage variation is quite high as since the charge attracted by M_{16}–M_{19} is directly related to the supply voltage. This can be a limitation but should be solvable by applying a low dropout regulator as the voltage source.

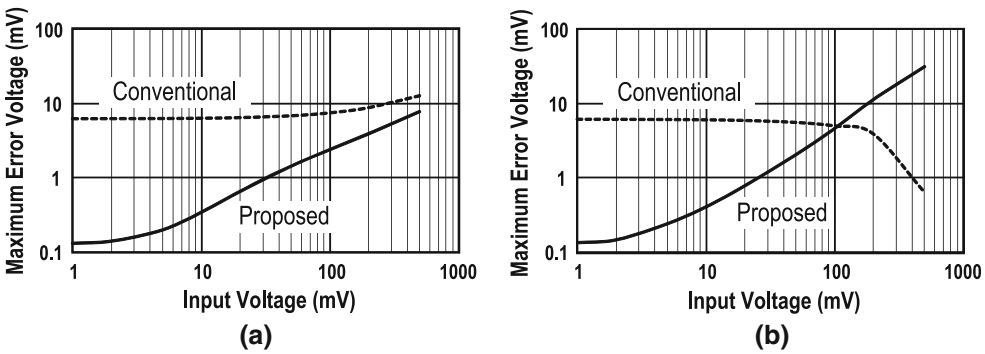

Fig. 4 Maximum input voltage variation due to kickback noise versus input voltage difference **a** $V_n > V_p$, **b** $V_n < V_p$

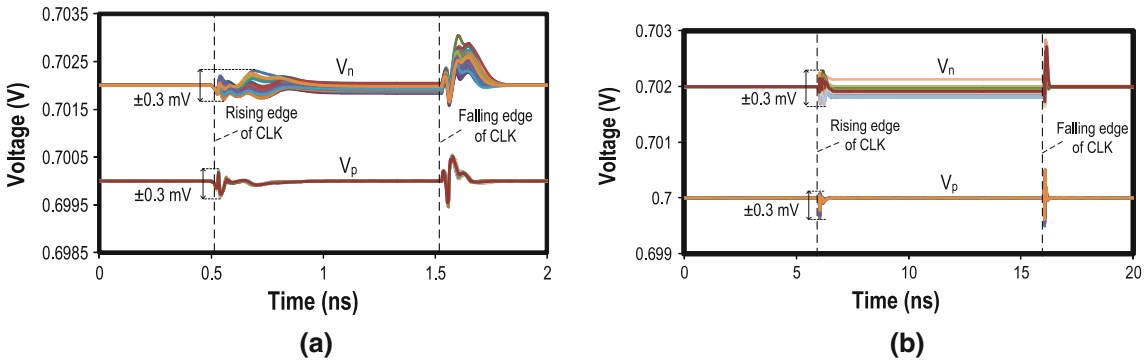

Fig. 5 Waveforms of proposed comparator's V_n and V_p in 30× Monte–Carlo simulations. **a** $f_{CLK} = 500$ MHz, **b** $f_{CLK} = 50$ MHz

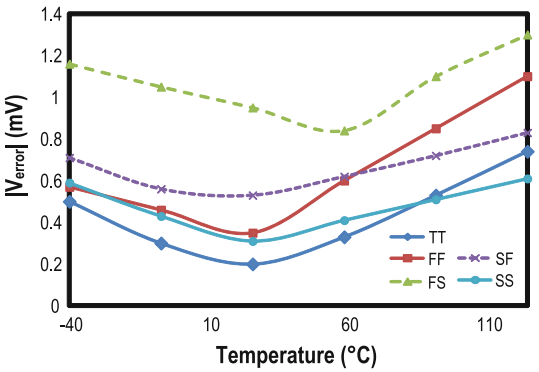

Fig. 6 Maximum deviation of the voltage on the capacitor at different temperature and process corners

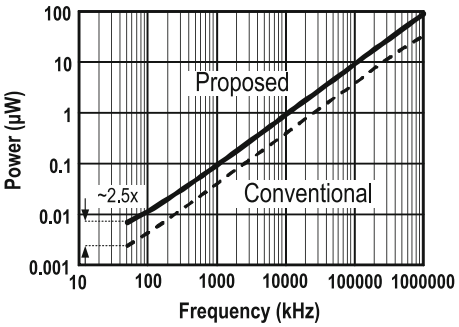

Fig. 8 Dynamic power versus the CLK frequency of the conventional and proposed comparators

The delays of conventional and proposed comparators are plotted in Fig. 7(a, b) with respect to the input voltages. The delay is measured between the times of CLK $= V_{DD}/2$ and $|V_{out,p} - V_{out,n}| = V_{DD}/2$. It can be observed that when $V_n > V_p$ the conventional comparator not only features more delay time when the input difference is small, but also gives a wrong decision. When $V_n < V_p$, the proposed comparator suffers from ∼130 ps longer delay when the input difference is 1 mV. It is due to the fact that node A is charged to V_{DD} when CLK is low, entailing a longer time to discharge it back to $V_{cm} - V_t$.

The dynamic power with CLK frequency is plotted in Fig. 8. The proposed comparator draws constantly 2.5× high power than the conventional one regardless of the CLK rate. For instance, the dynamic power of the conventional comparator is 16 μW at a CLK rate of 500 MHz whereas the proposed one is 41 μW, caused by the two added delay cells which need to drive the dummy cells M_{16}–M_{19}. There is no static power. The die sizes when counting only the width and length of transistor are 2.676 μm^2 (conventional) and 11.87 μm^2 (proposed). Although the power and area of the proposed comparator are increased by 2.5 and 4.4×, respectively, it can be considered a good trade-off for SAR-type ADCs, as there is only one comparator. Some of the charges may be leaked to the substrate during the formation and destruction of the channels in the transistors M_{16} and M_{17}. However, it has been tested that the voltage error due to this phenomena is just around 50 μV and it much less than the noise of the

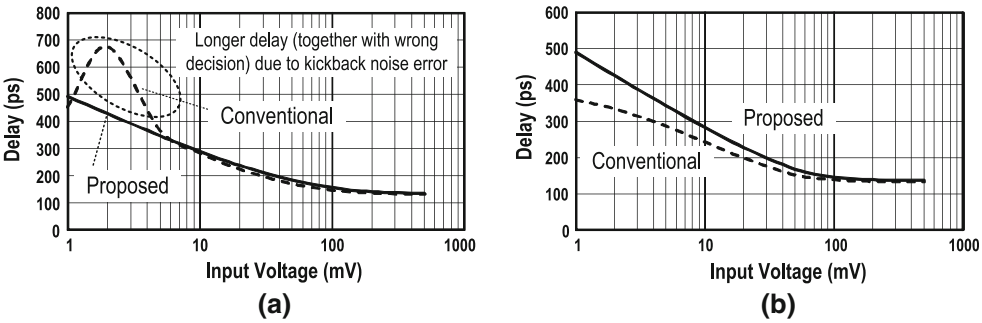

Fig. 7 Delay of the comparators versus input voltage difference in **a** $V_n > V_p$ and **b** $V_n < V_p$ cases

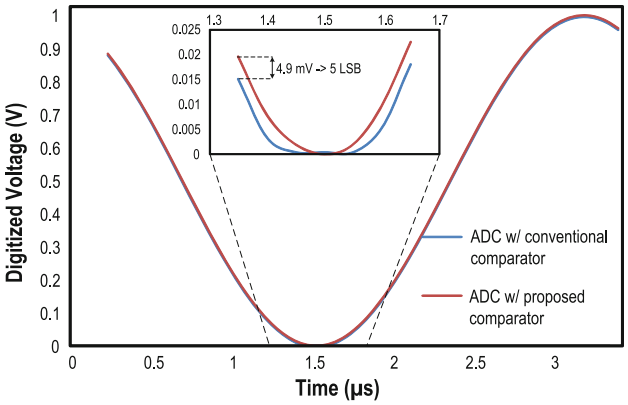

Fig. 9 Digitized waveform of a $1V_{p-p}$ sinusoidal signal by two ADCs with conventional and proposed comparator

comparator. Thus, it will not affect significantly the performance of the system.

The effectiveness of the comparator was also simulated with a 1-V single-ended 20-MS/s 10-bit SAR ADC with a unit capacitance of 1 fF. The structure is similar to Fig. 1. With a full range input sine wave of 312.5 kHz, the total harmonic distortion (THD) of the output digital code of the ADC with original comparator is −52.27 dB while the THD of ADC employed the proposed comparator is −60.15 dB, which is improved due to the improved decision accuracy of the proposed comparator. This can be seen from Fig. 9, which shows the digitized output of two identical ADCs but with different comparators (conventional and proposed). The ADC with the conventional comparator will suffer an offset around 4.9 mV (5 bits) at the enlarged region due to improper decision of the comparator, as illustrated in Figs. 2 and 3(b), which imposed harmonic distortion on the digitized output.

2 Conclusions

The mechanism of kickback noise generation in a dynamic latched comparator has been analyzed, and a robust kickback noise cancellation technique has been proposed. By adding the comparator well-positioned clocked NMOS-PMOS capacitors, those unwanted charges at different dynamic nodes can be cancelled effectively, restraining the voltage variation at the inputs due to different operation regions of the MOS devices. The comparator is particularly suitable for the SAR-type ADC as the charge stored in the capacitor array will not be affected. Simulated in 65-nm CMOS with different clock rates of 50 and 500 MHz, the kickback noise is $<\pm$ 0.3 mV in 30× Monte–Carlo simulations with both mismatch and process variations taken into account. For 10-bit resolution in a full scale of 1 V_{pp}, the kickback noise of the proposed comparator is improved by 48×, from 6.27 to 0.13 LSB, comparing with the conventional one. A 1-V single-ended 20-MS/s 10-bit SAR ADC employing the proposed comparator yields 8-dB THD improvement over the conventional one.

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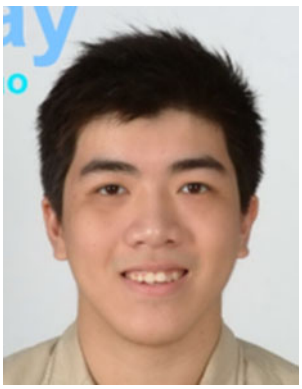

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Rui P. Martins (M'88-SM'99-F'08) received the Bachelor (5-years), Masters, and Ph.D. degrees as well as the *Habilitation* for Full- Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon, Portugal, in 1980, 1985, 1992 and 2001, respectively. He has been with the Department of Electrical and Computer Engineering/IST, TU of Lisbon, since October 1980. Since 1992, he has been on leave from IST, TU of Lisbon, and is also with the Department of Electrical and Electronics Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he is a Full-Professor since 1998. In FST he was the Dean of the Faculty from 1994 to 1997 and he has been Vice-Rector of the University of Macau since 1997. From September 2008, after the reform of the UM Charter, he was nominated after open international recruitment as Vice-Rector (Research) until August 31, 2013. Within the scope of his teaching and research activity he has taught 20 bachelor and master courses and has supervised 22 theses, Ph.D. (9) and Masters (13). He has published: 15 books, co-authoring (4) and co-editing (11), plus 5 book chapters; 185 refereed papers, in scientific journals (36) and in conference proceedings (149); as well as other 70 academic works, in a total of 275 publications, in the areas of microelectronics, electrical and electronics engineering, engineering and university education. He has co-authored also 7 submitted US Patents (1 approved and issued in 2009, 1 classified as "patent pending" and 5 still in the process of application). He has founded the *Analog and Mixed-Signal VLSI Research Laboratory of UM*: http://www.fst.umac.mo/en/lab/ans_vlsi/. Prof. Rui Martins was elevated to IEEE Fellow *for his leadership in engineering education*. He was the Founding Chairman of the IEEE Macau Section from 2003 to 2005, and of the IEEE Macau Joint-Chapter on Circuits And Systems (CAS)/Communications (COM) from 2005 to 2008 [*World Chapter of the Year 2009* of the *IEEECircuits And Systems Society (CASS)*]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on Circuits And Systems—*APCCAS'2008*, and was elected Vice-President for the Region 10 (Asia, Australia, the Pacific) of the *IEEE Circuits And Systems Society (CASS)*, for the period of 2009 to 2010. He is Associate Editor of the *IEEE TransactionsonCircuitsandSystemsII—ExpressBriefs*, for the period of 2010 to 2011. He was the recipient of 2 government decorations: the *Medal of Professional Merit* from Macao Government (Portuguese Administration) in 1999, and the *Honorary Title of Value* from Macao SAR Government (Chinese Administration) in 2001. In July 2010 he was elected as Corresponding Member of the Academy of Sciences of Lisbon, Portugal.